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Design and Characterization of the Readout ASIC for the BESIII CGEM Detector

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TIGER (Turin Integrated Gem Electronics for Readout) is a mixed-mode ASIC for the readout of signals from CGEM (Cylindrical Gas Electron Multiplier) detector in the upgraded inner tracker of the BESIII experiment, carried out at BEPCII in Beijing. The ASIC includes 64 channels, each of which features a dual-branch architecture optimized for timing and energy measurement. The input signal time-of-arrival and charge measurement is provided by low-power TDCs, based on analog interpolation techniques, and Wilkinson ADCs, with a fully-digital output. The design and test results of TIGER first prototype are presented showing its full functionality.

Summary

The ASIC presented is developed for the readout of signals coming from the CGEM detector of the BESIII experiment. The detector is scheduled to be installed during the 2018 upgrade and features an innovative, lightweight three-layer triple-CGEM tracker with analog readout. This type of readout employs a charge centroid method to improve the spatial resolution while keeping the front-end channels to a relatively small number of about 10000.

In order to meet the requirements set by the experiment, the readout ASIC has been designed to operate with an input capacitance of about 100 pF, input dynamic range 1-50 fC, power consumption <10 mW/channel and event rate of 60 kHz/channel. Additionally, a time resolution better than 10 ns is required in order to time-tag each hit and operate the detector in the so-called "micro-TPC"mode thus improving the spatial resolution of angled tracks.

Designed in a 110 nm CMOS technology, the ASIC consists of 64 channels, references and bias generators, a digital global controller and an internal test pulse calibration circuitry. Each channel comprises an analogue front-end for signal amplification and shaping and a mixed-mode back-end to digitize the information.

The front-end is composed of a charge sensitive amplifier coupled to two shapers, each of which is connected to a discriminator with a programmable threshold. The time-branch shaper generates a fast signal, optimized for timing measurements with a leading-edge threshold, while the energy-branch shaper provides a slower signal, allowing for better signal integration and equivalent noise charge (ENC) optimization.

The time measurement is performed by two low-power TDCs, each of which is composed by four time-to-amplitude converters and a 10-bit Wilkinson ADC. A quad-buffered Sample&Hold (S/H) circuit is connected at the output of the energy-branch shaper, operating as a digitally controlled peak detector. The signal peak amplitude is digitized by the same Wilkinson ADC used by the TDC, so the charge information is obtained either from the time-over-threshold (ToT) or the S/H circuit. The event data are sent to a digital block, running at 160 MHz, that controls the chip operations, handles the global and channel registers configuration and manages the off-chip data transmission through 2 LVDS output links.

The ASIC has been electrically characterized and all the specified requirements are met within the limited power budget of 10 mW per channel. The S/H linearity is very good (less than 0.2%) for an input charge in the 5-40 fC range. The TDC resolution is better than 50 ps r.m.s., such that its contribution to the intrinsic time resolution becomes negligible. The equivalent noise charge (ENC) with 100 pF input capacitance is about 2500 electrons. Despite the fact that the measured noise performance is already adequate for our application,

PSRR, interference and grounding conditions are currently under study. First results of tests with the CGEM prototype using cosmic rays and a 90Sr source will be presented.
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