Contribution ID: **153** Type: **Oral**

A high-Precision Timing ASIC for TOF-PET Applications

Wednesday 13 September 2017 12:20 (25 minutes)

Detectors with precise time-of-flight measurement capabilities are a very active area of research in particle physics and imaging, due to their improved accuracy and background rejection. In this contribution we present a monolithic readout ASIC, developed for a novel PET scanner, featuring a 30 ps time resolution for 511 keV photons using a SiGE HBT based front-end, capable of driving large input capacitances (up to 1 pF) while using less than 150 μW/channel. A fully-functional prototype has been submitted to IHP and a full version is in an advanced stage of design.

Summary

Time-of-flight (TOF) measurement in PET scanners allows a more accurate image reconstruction and/or a lower delivered radiation dose. In conventional PET, coincidence detectors are used to determine along which line of response an annihilation has occurred. The information added by the TOF measurement allows a more accurate determination of the position of the annihilation by reducing the line of response to a short segment. In order to extract valuable information on the position of the annihilation point, a high TOF precision is required (at least < 200 ps, but higher resolutions lead to more accurate results).
To achieve a good timing performance, front-ends need to have a low equivalent noise and a fast rise time (to reduce the jitter as much as possible). SiGe BiCMOS technology is a good candidate for this application.
We are developing a fully custom ASIC to take advantage of the characteristics of the SiGe Bi-CMOS process for timing measurements, integrating a fully-depleted pixel matrix with a low-power BJT-based front-end per channel, integrated on the same 100 μm thick die. All the pixels are multiplexed to a single TDC to extract timing information. Each front-end includes a BJT preamplifier with active feedback, a CMOS discriminator and a calibration DAC. A triggered readout logic is included to reduce the data to be read out of the system.
The target timing resolution is 30 ps for a 511 keV photon with a 1 pF input capacitance. The front-end has a gain of ˜90 mV/fC and a rise time of ˜1ns. Its low power consumption of ˜135 μW, makes it possible to stack multiple ASICs on top of each other, in order to increase the detection efficiency. A total of more than 1 million channels will form the complete scanner.
A full-featured prototype with a small 10-by-3 pixel matrix has been submitted in March 2017, after a number of smaller prototypes to validate each block. A full-size chip is currently being designed.

Authors: VALERIO, Pierpaolo (CERN); PAOLOZZI, Lorenzo (Universite de Geneve (CH)); CARDARELLI, Roberto (Universita e INFN Roma Tor Vergata (IT)); IACOBUCCI, Giuseppe (Universite de Geneve (CH))

Co-authors: RIPICCINI, Emanuele (UNIGE); HAYAKAWA, Daiki (Universite de Geneve (CH)); Mr CALTABIANO, Alessandro (Università di Roma Tor Vergata); Mr BRUNO, Salvatore (Università di Roma Tor Vergata); BENOIT, Mathieu (UNIGE)

Presenter: VALERIO, Pierpaolo (CERN)

Session Classification: ASIC

Track Classification: ASIC