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An 8-Channel ASD in 130 nm CMOS with Superior Performance of Rise Time, Noise and Threshold Uniformity for ATLAS Drift Tube Readout at the HL-LHC

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ATLAS Muon-Drift-Tubes spatial resolution-&-efficiency depend on drift-time resolution, noise levels, and accurate threshold setting. A new 130nm read-out device is developed and optimized, for the required time resolution, to guarantee rise-times below 10ns, with acceptable time-slewing effects. Moreover, the large chain-amplification results in increased sensitivity to any disturbance (mainly from supply). To avoid additional costs to clean up the set-up from such disturbs, the read-out chain adopts innovative techniques (at system, circuit, and design levels) minimizing read-out chain disturb sensitivity. This paper details the design strategy, compares post-layout simulation with measurements and presents resolution studies in CERN high-energy testbeam.

Summary

ATLAS MDT of HL-LHC (High-Luminosity Large-Hadron-Collider) interface with 8xASD (Amplifier-Shaper-Discriminator) ASIC. The new electronics in IBM 130nm CMOS 8RF-DM technology must be able to detect charged particles in 5fC –100fC range with <15ns rising time in challenging operative conditions. These arise out peak luminosity increment of a factor 5 –7.5 beyond the nominal value of 1034 cm-2 s-1.
The 8xASD includes eight channels designed to comply with rising time, signal-to-noise and threshold uniformity specifications. Each channel includes an input stage (a Charge Sensitive Preamplifier, CSPreamp) able to convert the input charge signal into a voltage one. This analog signal provides information about charge arrival time and charge amount. The 8xASD can also operate in ToT (Time-over-Threshold) mode.
This paper presents the second ASD ASIC prototype for ATLAS MDT (the first ASIC was presented in [1]. It occupies an area of 7.64mm2 performing about 14mV/fC of sensitivity and 12ns of rising time at discriminator input with 10mA/channel current consumption and 3.3V supply voltage.
The first front-end element of previous ASD chain[1] is the CSPreamp. It is built-up by a single-ended (i.e. a common source) analog gain stage with a feedback capacitor (and a resistor for operating point). Unfortunately, this solution is very sensitive to voltage supply and ground references. These situations are further stressed by the large amplification gain in ASD chain (after the CSPreamp) and by common substrate layout, featuring very poor noise/disturbs rejection. This definitively degrades whole analog chain PSRR.
The main consequences are higher false positive events rate (scanning along the threshold voltage codes, i.e. about three orders of magnitude higher than specifications) and inaccurate Time-over-Threshold for low input charge (i.e. 5fC –25fC).
In previous design, the noise signal coming from supply and ground references reaches the CSPreamp output with 6.5dB (2.11 factor) gain and, then, it is further amplified by three amplification stages causing false detections.
In this scenario, the 8xASD has been modified in terms of CSPreamp circuital topology, preferring a fully differential structure.
Post-layout simulations validate this choice demonstrating that the unwanted supply noise signal is attenuated of -7dB (0.44 factor) at first stage output. The reduction of 13.5dB (4.7factor) of this parameter makes it

a valid choice without analog performance degradation like rising time, sensitivity, etc. The channel power consumption is the same whereas there is a total area increment of about 14%. This is due to the better isolation of analog parts from digital ones creating regions of high resistive path (named BFMOAT and provided by foundry) and Guard Rings. Area increment from 6.73mm2 to 7.64mm2 has been allowed to divide different supplies and to manage them externally by user.
An improved version of 8xASD chip for ATLAS MDT Chamber has been designed and integrated with the final target to replace the actual mounted ASICs [1].
[1] DE MATTEIS, M., et al. Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC. JINST 2016.
[2] POSCH, C., et al. Mdt-asd, cmos front-end for atlas mdt. 2007.

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