



Development of depleted monolithic pixel sensors in 150 nm CMOS technology for the ATLAS Inner Tracker upgrade

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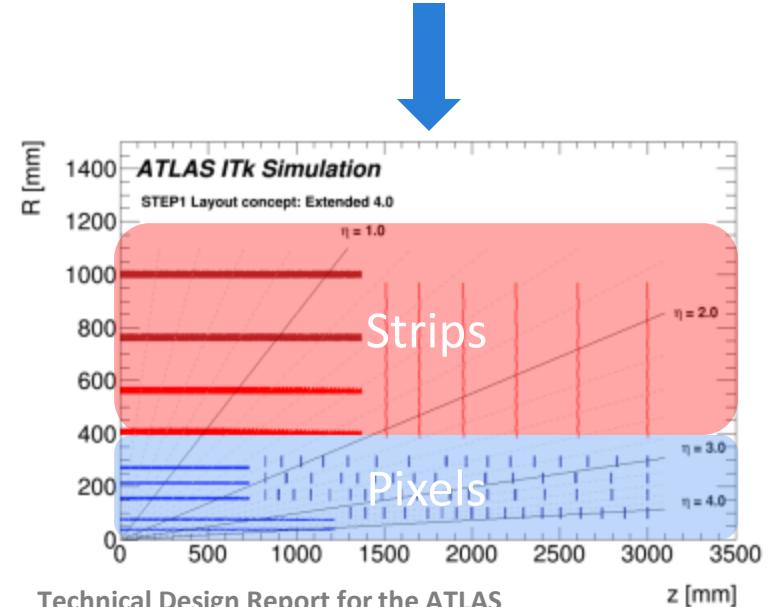
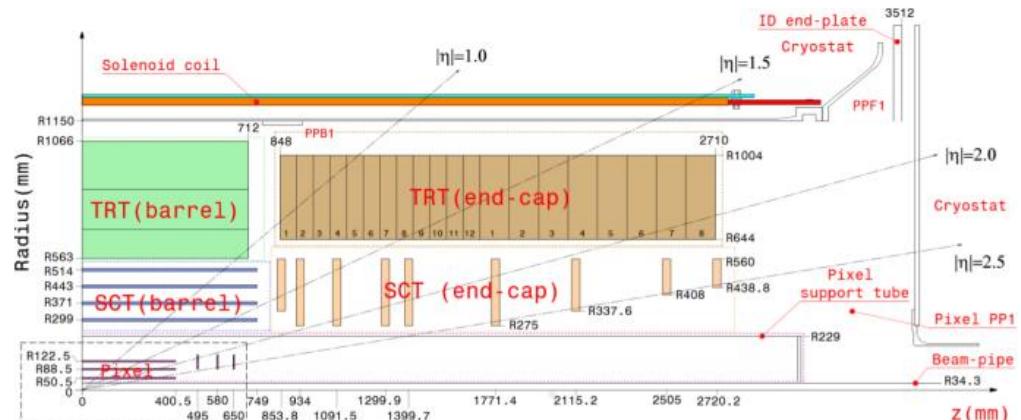


Outline

- Introduction
- Description of the design
- Measurement results
- Summary

ATLAS Phase II Upgrade: Inner Tracker (ITk)

- LHC phase II upgrade in ~2025
- More stringent requirements for Inner Detector
 - Rad. level up to: $10^{16} \frac{n_{eq}}{cm^2}$ & 1 Grad TID
 - High particle rate: occupancy, bandwidth, ...
- A new all-silicon inner tracker will replace the current detector
- New pixel detector baseline – hybrid pixels (fast readout and radiation hard)
- CMOS Demonstrator collaboration is evaluating suitability of CMOS pixels for the outer pixel layers



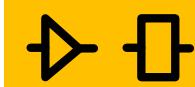
Technical Design Report for the ATLAS
Inner Tracker Strip Detector
CERN-LHCC-2017-004. ATLAS-TDR-025, April 2017

CMOS Demonstrator Program

- Several possibilities were investigated and prototypes in different technologies have been designed



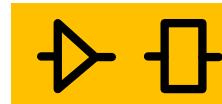
Sensor



R/O chip



Diode +
preamp



R/O chip



Diode + Amp +
Digital

Passive CMOS sensor + R/O chip

Active CMOS sensor + R/O chip

Monolithic device

- Currently most focus is given to monolithic devices

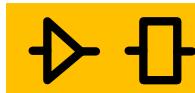
- Aiming for radiation hardness up to $10^{15} \frac{n_{eq}}{cm^2}$ & 80 Mrad TID
- Fast R/O with 25ns precision required
- Possible gains: lower sensor manufacturing cost , cheaper and simpler module assembly

CMOS Demonstrator Program

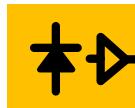
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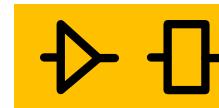
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- Aiming for radiation hardness up to $10^{15} \frac{n_{eq}}{cm^2}$ & 80 Mrad TID

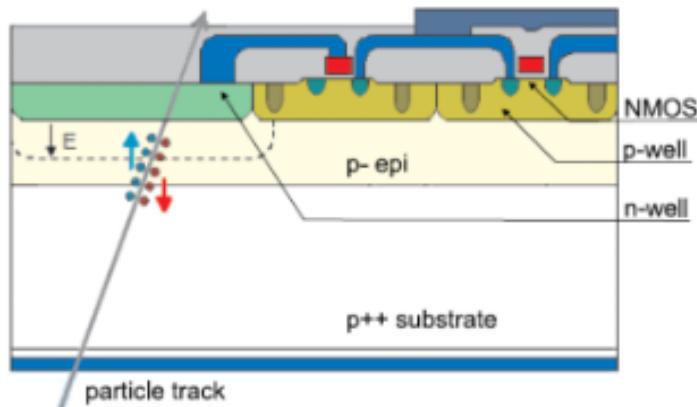
- Fast R/O with 25ns precision required

- Possible gains: lower sensor manufacturing cost , cheaper and simpler module assembly

Chip name	Technology	Fill factor	Pixel size [μm^2]	R/O architecture	Staus
aH18	Fab A (180nm)	Large	56 × 56	Asynchronous	Measurements
H35DEMO	Fab A (350nm)	Large	50 × 250	Synchronous	
Malta	Fab B (180nm)	Small	36 × 36	Asynchronous	Ready for submission
TJ Monopix		Small	36 × 40	Synchronous	
Coolpix		Large	50 × 250	Synchronous	
LF Monopix	Fab C (150nm)	Large	50 × 250	Synchronous	Measurements
LF2		Large	50 × 50	Synchronous	

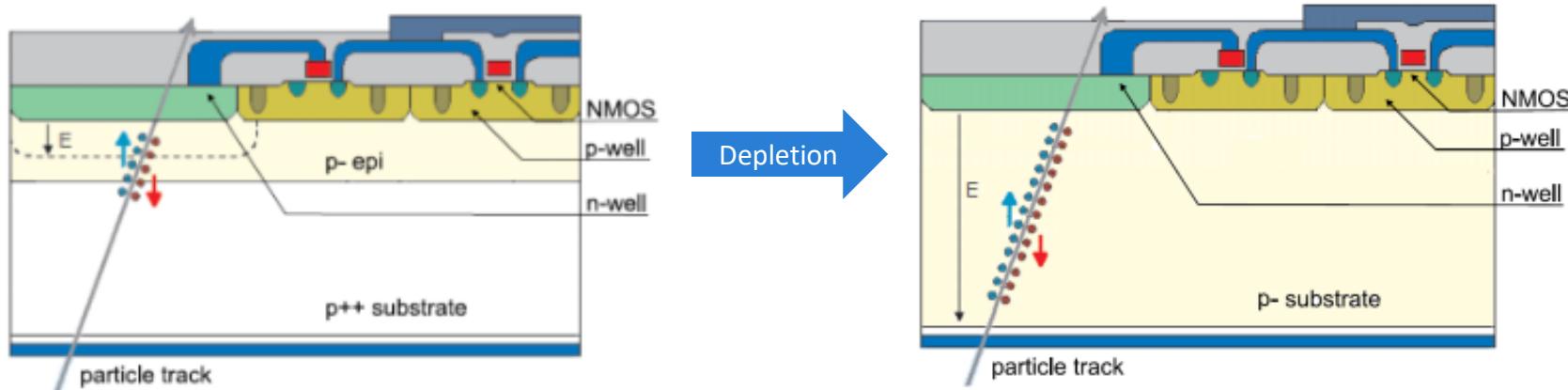
- Monolithic pixels are not new idea

	STAR	ALICE-LHC	ILC	ATLAS-HL-LHC	
				Outer	Inner
BX-time [ns]	110	20 000	350		25
Particle Rate [kHz/mm ²]	4	10	250	1000	10 000
Fluence [n _{eq} /cm ²]	> 10 ¹²	>10 ¹³	10 ¹²	10 ¹⁵	2x10 ¹⁶
Ion. Dose [Mrad]	0.2	0.7	0.4	50	> 1000



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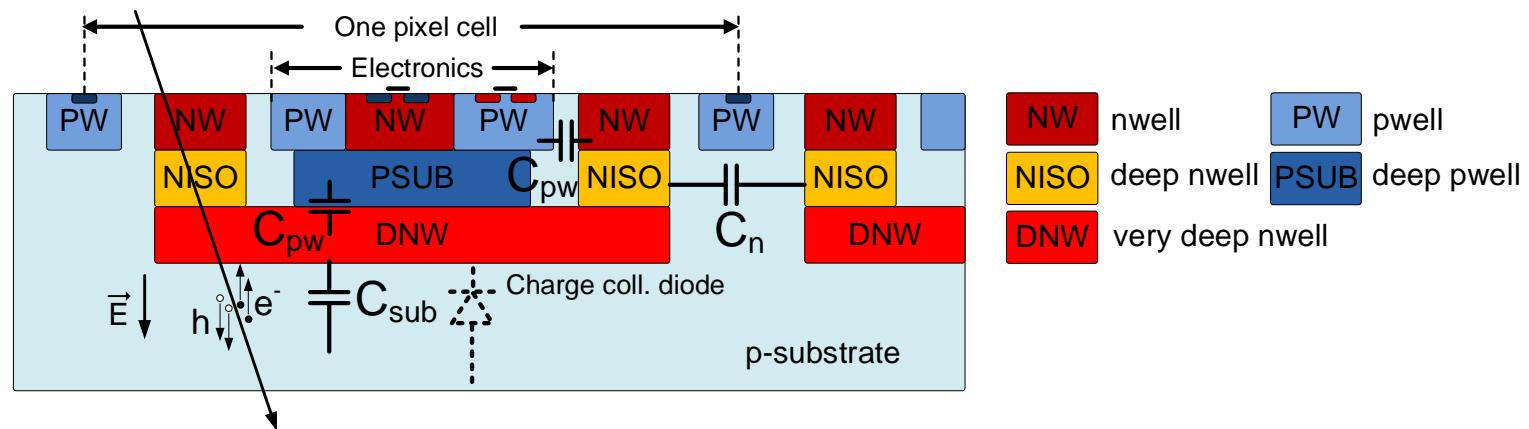


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- Measurement results
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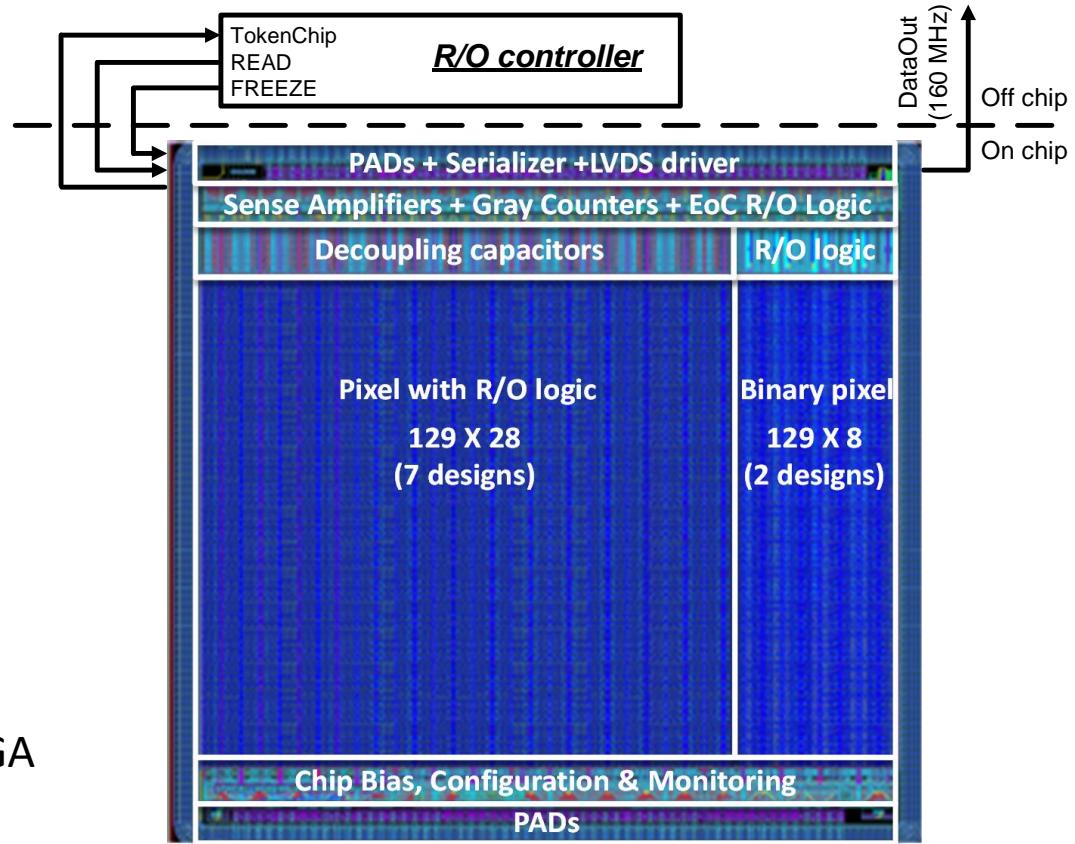
Technology

- 150nm CMOS
- Multiple nested wells available
- Manufactured on high resistivity ($>2\text{k}\Omega\text{cm}$) p-type bulk (depletion width $d \propto \sqrt{U_{bias} \cdot \rho_{sub}}$)
- Thinning and back size processing possible



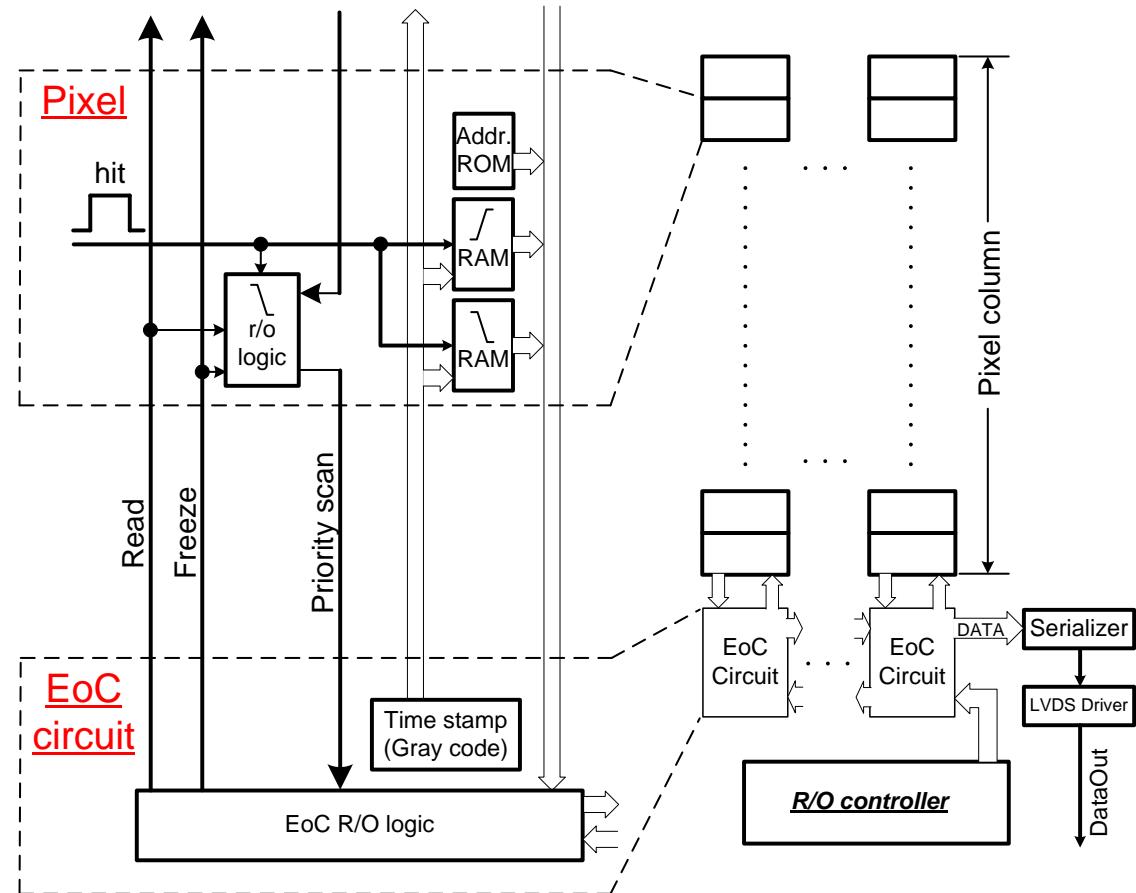
LF Monopix chip overview

- Chip size ~ 10mm × 9.5 mm
- 50 μ m × 250 μ m pixel size
- Matrix of 129 × 36 pixels
- 9 pixel flavours – each 4 column
(8bit ToT with 25ns time stamp resolution)
- Column drain R/O scheme
- No trigger memory on chip
- 160 MHz LVDS serial output
- R/O controller implemented off chip by FPGA
- Silicon arrived in March 2017
- Now under characterization



Column drain R/O architecture

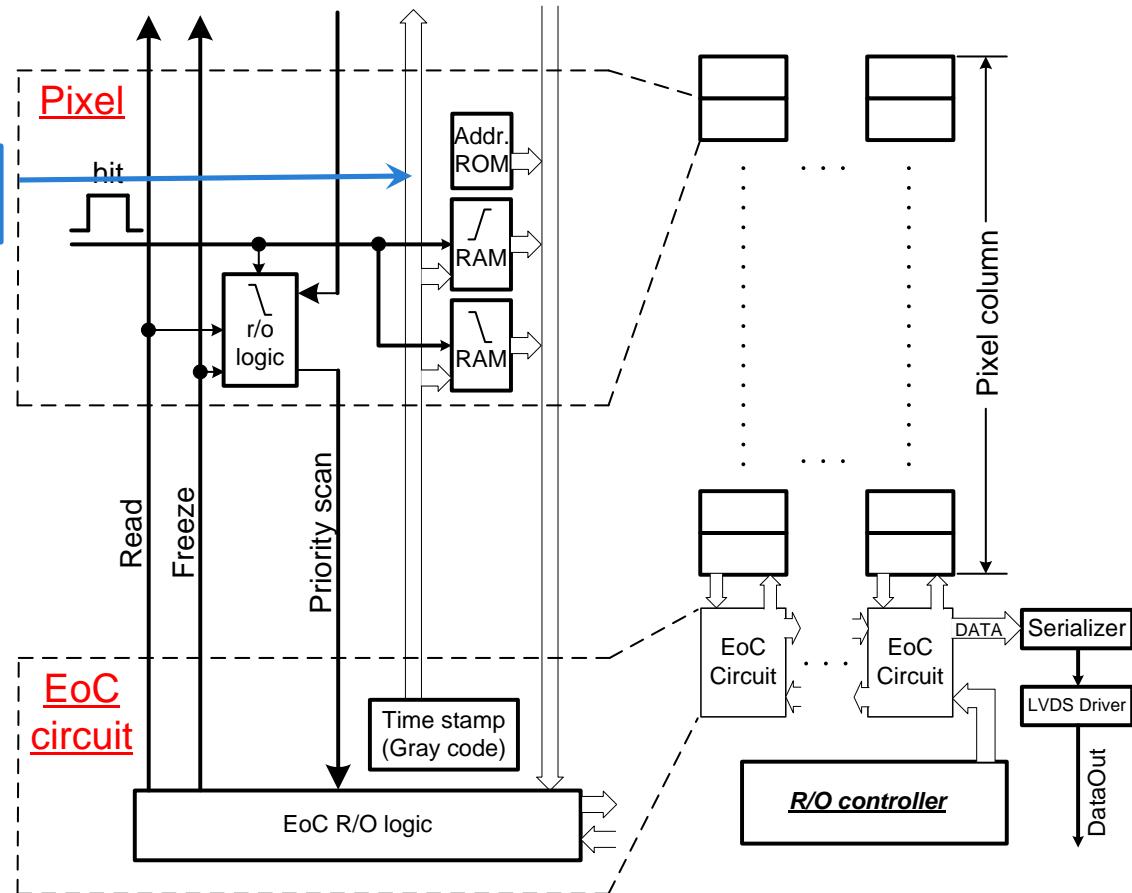
- Already used in ATLAS (FE-I3)
- Relatively simple in-pixel digital logic
 - Preferable for DMAPS



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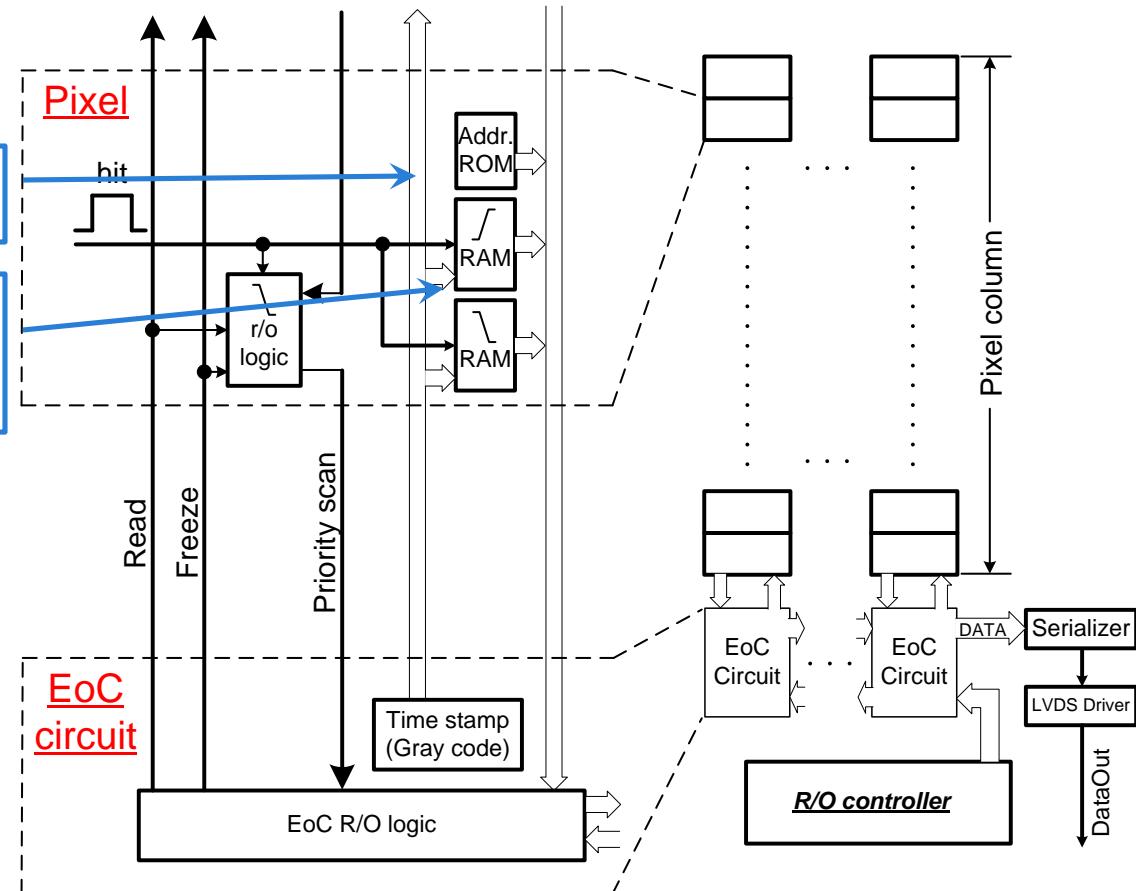
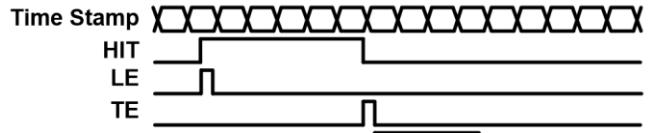
Time Stamp XooooooooooooooX



Column drain R/O architecture

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- Time stamp distributed in pixel array
- Hit information stored in the pixel
- Coarse analog measurement by ToT



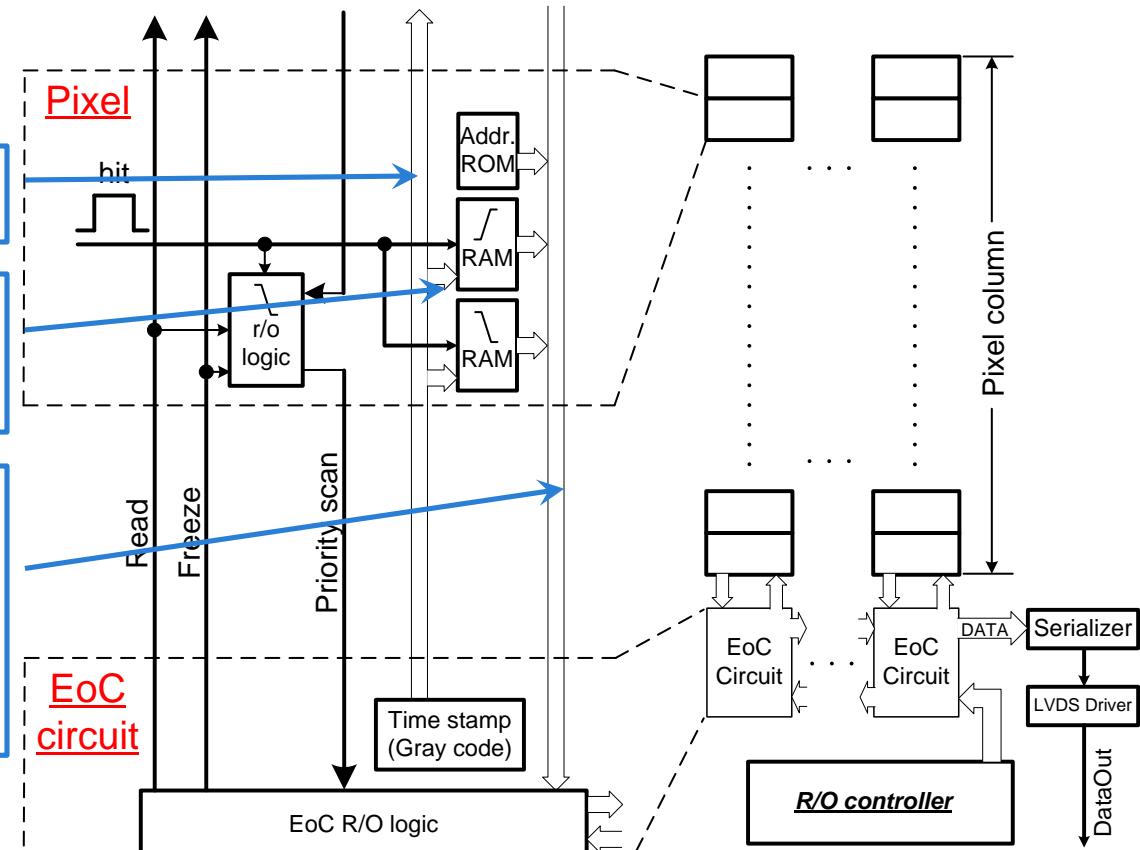
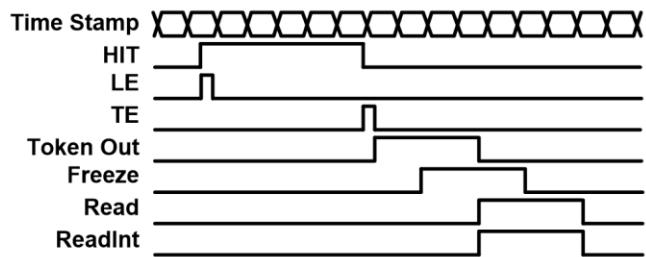
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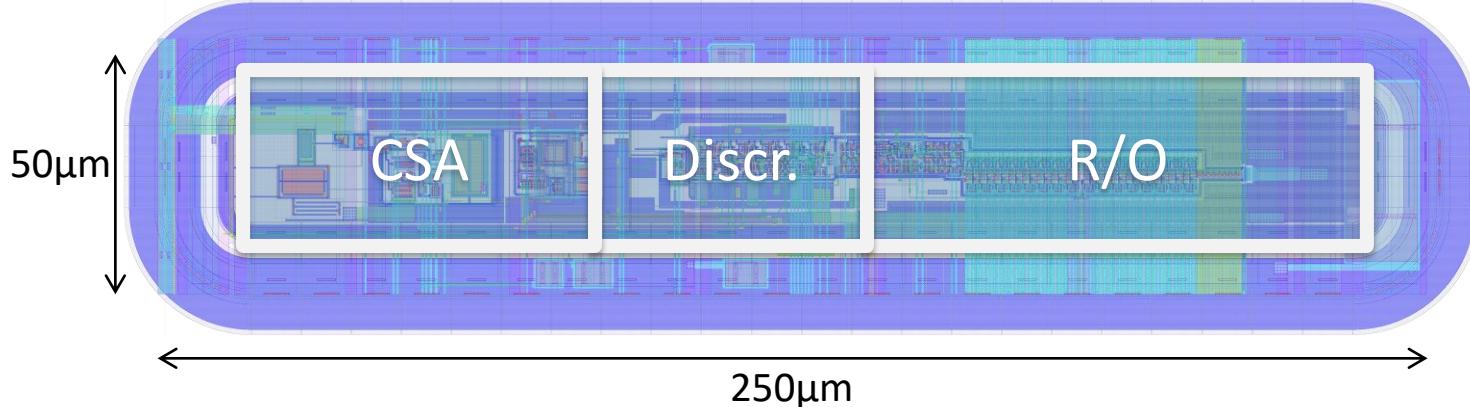
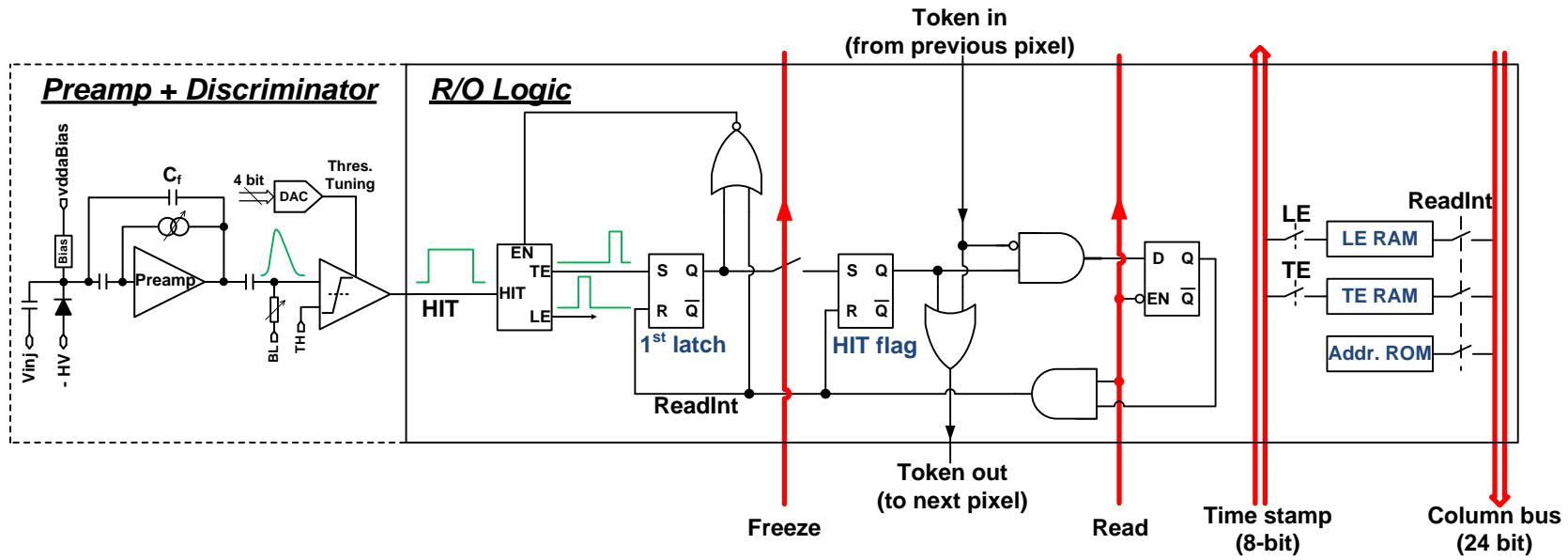
- Time stamp distributed in pixel array

- Hit information stored in the pixel
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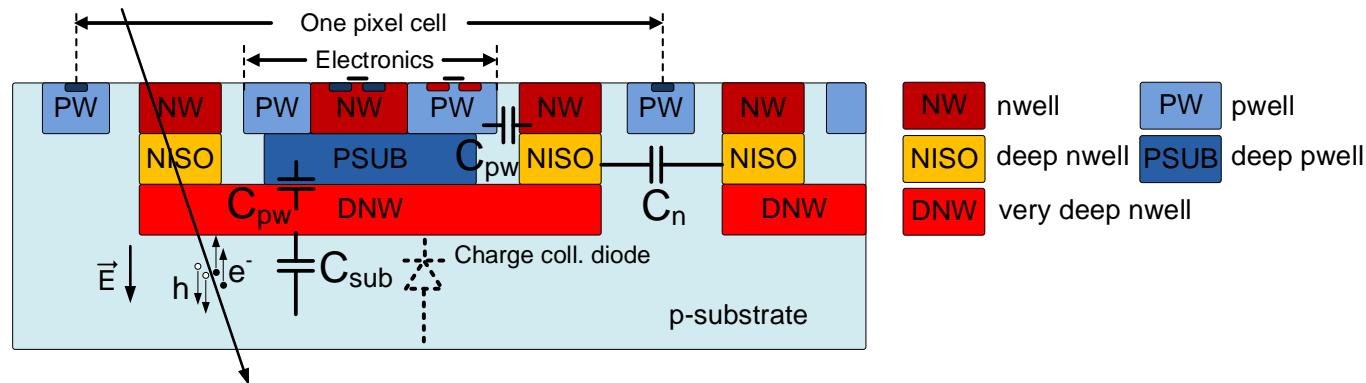
- TE initiates R/O process arbitrated by EoC logic
- Data bus shared by one column
- Topmost hit has the highest R/O priority



Pixel design

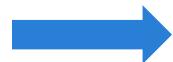


Design challenges for LF-MonoPix01



- Large detector capacitance $C_D = C_{sub} + C_n + C_{pw}$

$$\tau_{CSA} \sim \frac{1}{g_m} \cdot \frac{C_D}{C_f}$$

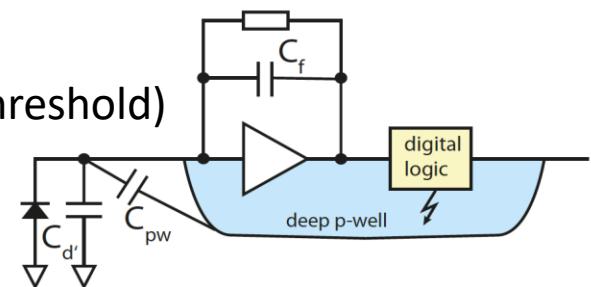


Power required to compensate ($g_m \sim I_D$)

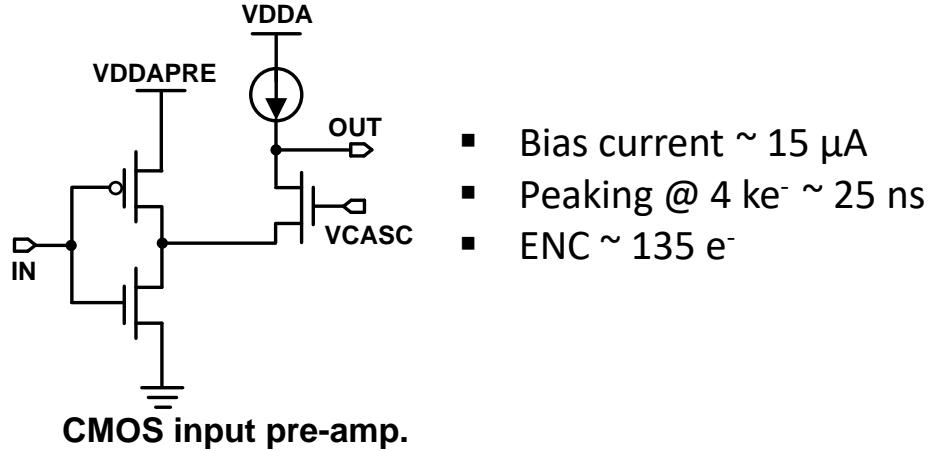
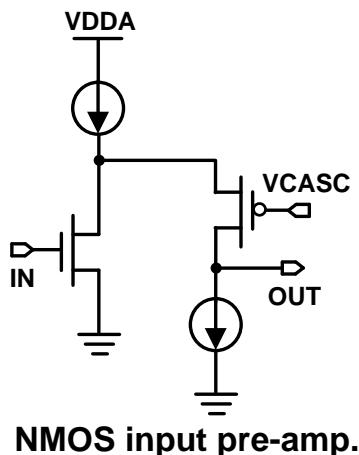
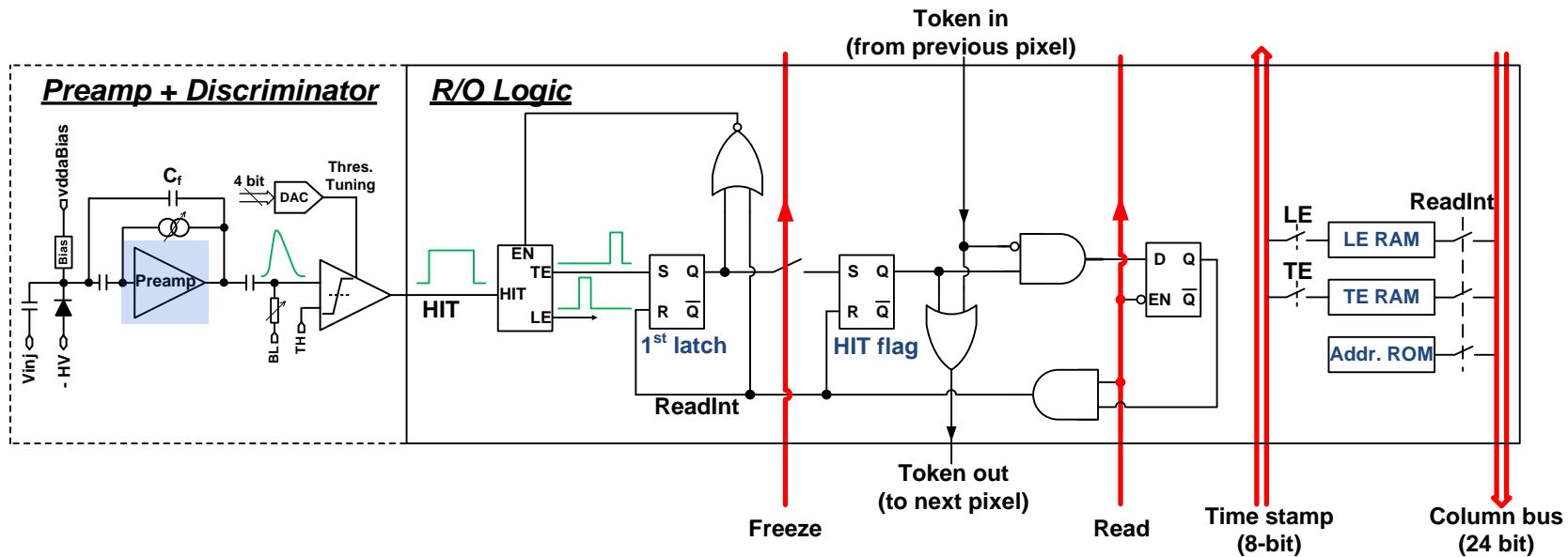
$$ENC_{thermal}^2 \sim \frac{4}{3} \cdot \frac{kT}{g_m} \cdot \frac{C_D^2}{\tau}$$

- C_{pw} couples substrate noise into the sensor (e.g. limits minimum threshold)

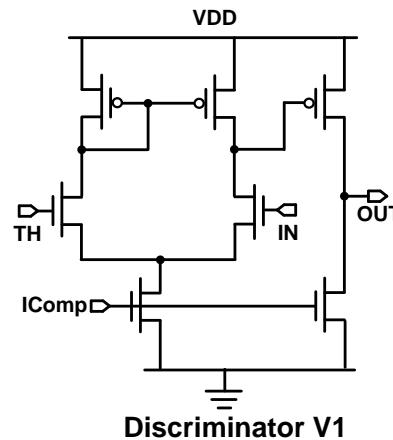
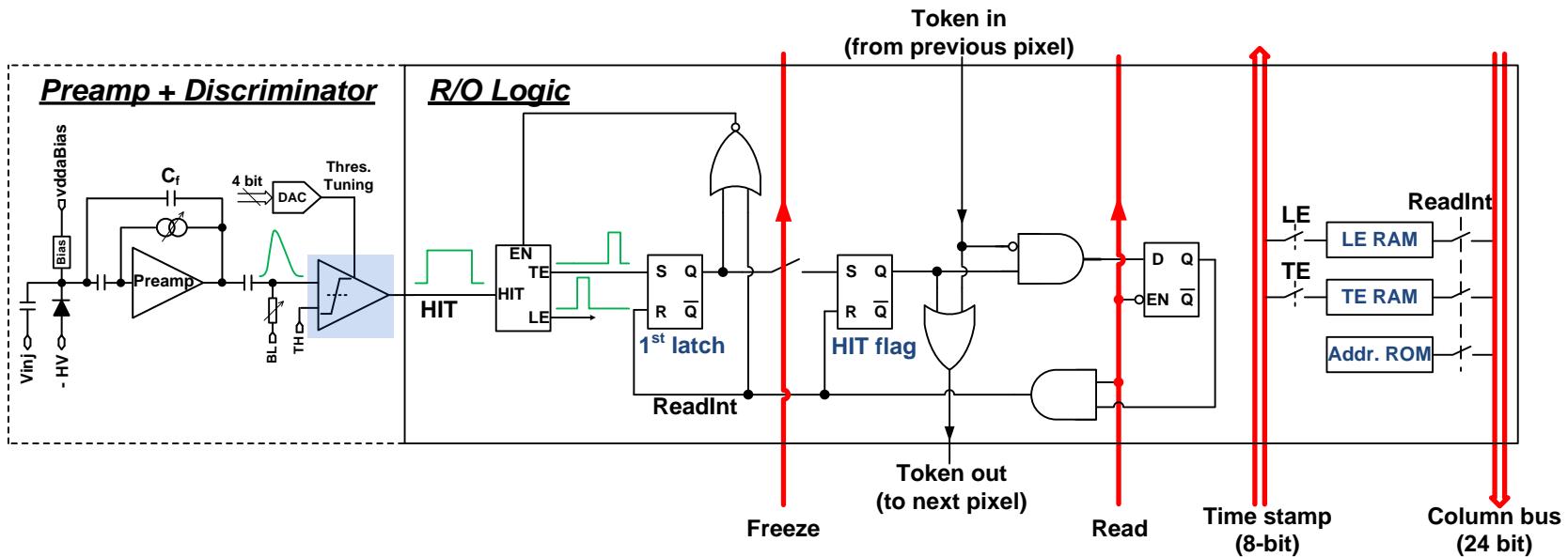
example: $C_{pw} = 100 \text{ fF}$, $\Delta V_{pw} = 1 \text{ mV} \rightarrow Q_{x\text{-talk}} = 625 \text{ e}^-$



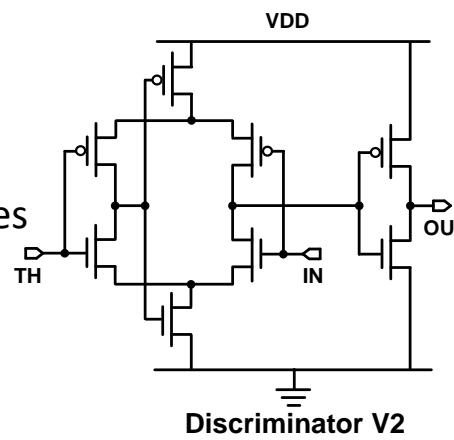
Pre-amplifier



Discriminator

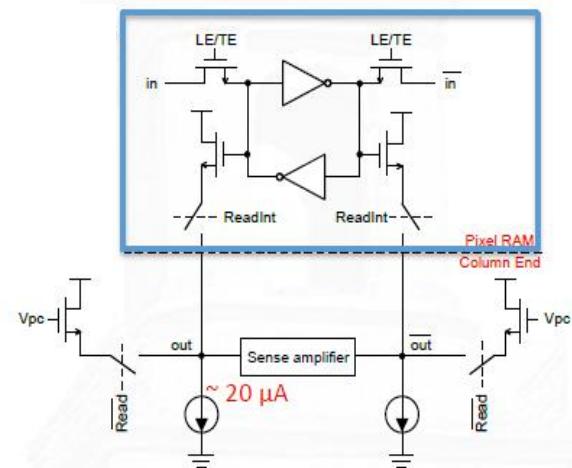
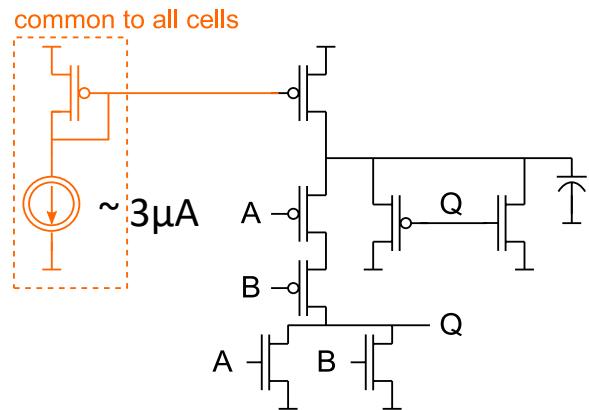
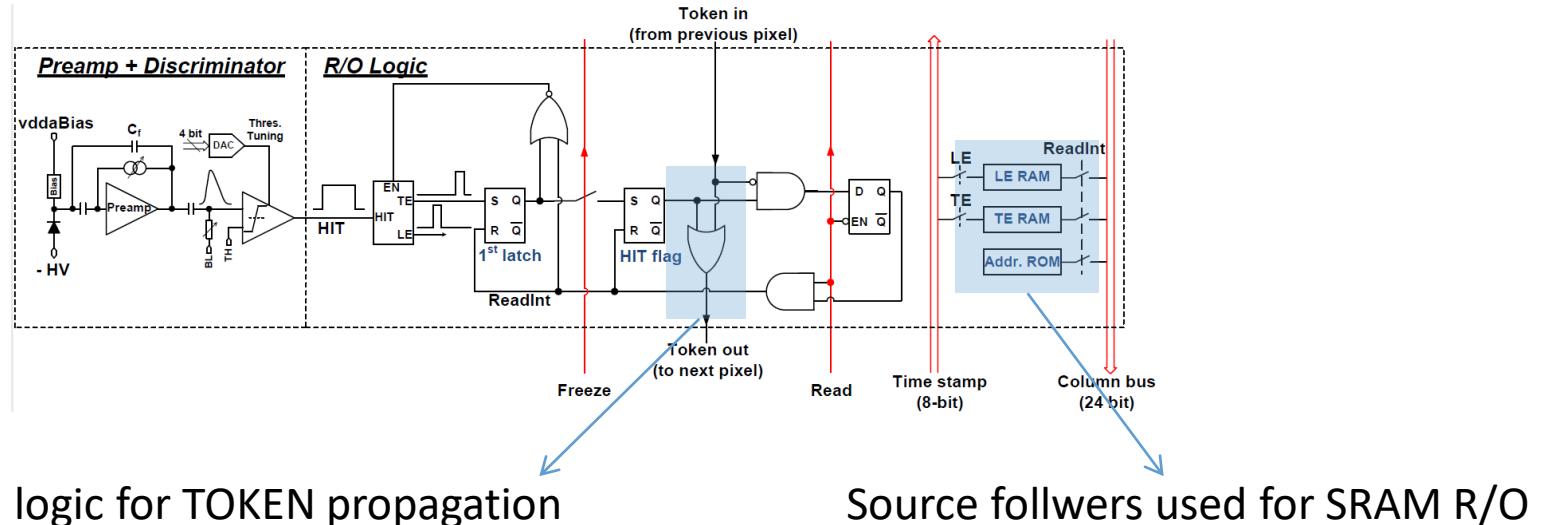


- 2-stage amplifier
- Bias current: $4.5 \mu A$
- Used in previous prototypes

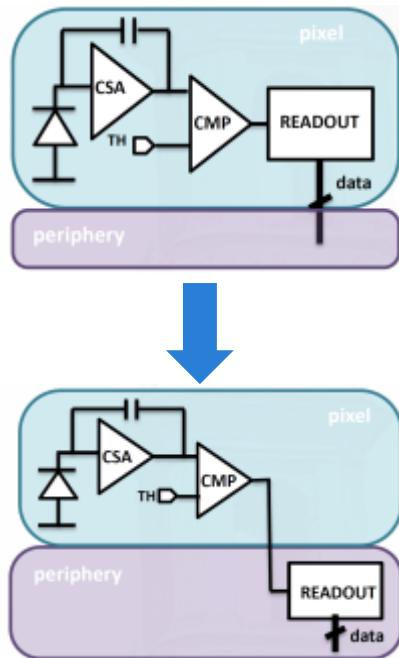
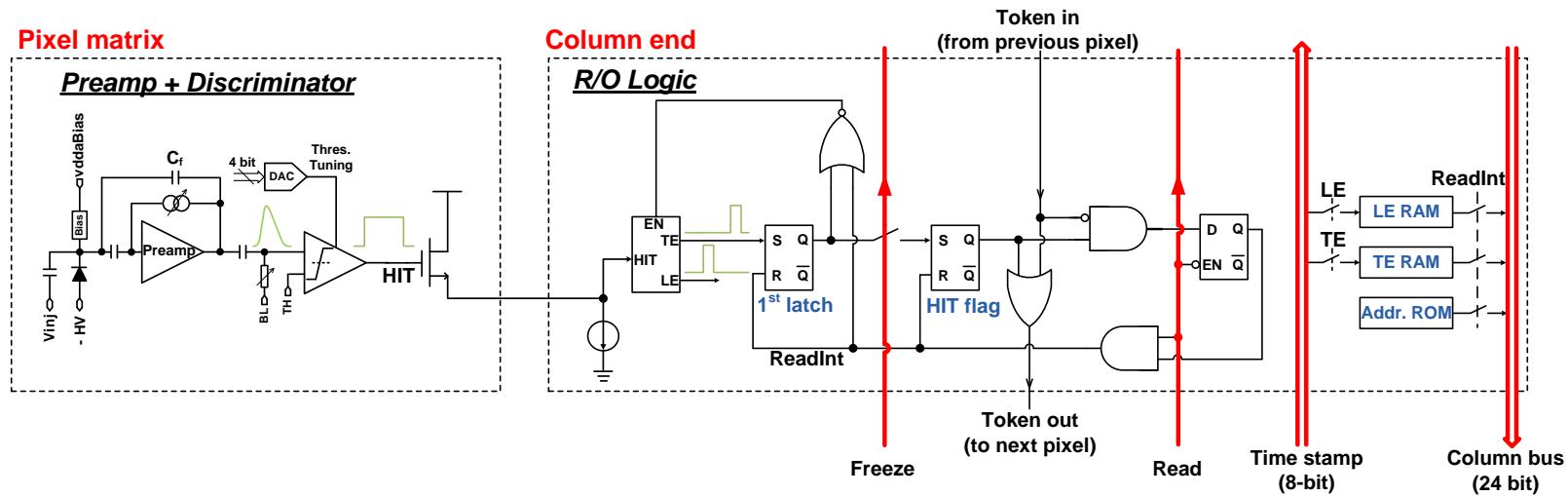


- Push-pull amplifier
- Self biased: $< 4 \mu A$
- CMOS inverter as 2nd stage
- New design in LF-MonoPix (expected to have lower time walk)

Cross talk minimization efforts in LF-MONOPIX01



Binary pixel + R/O logic at column end

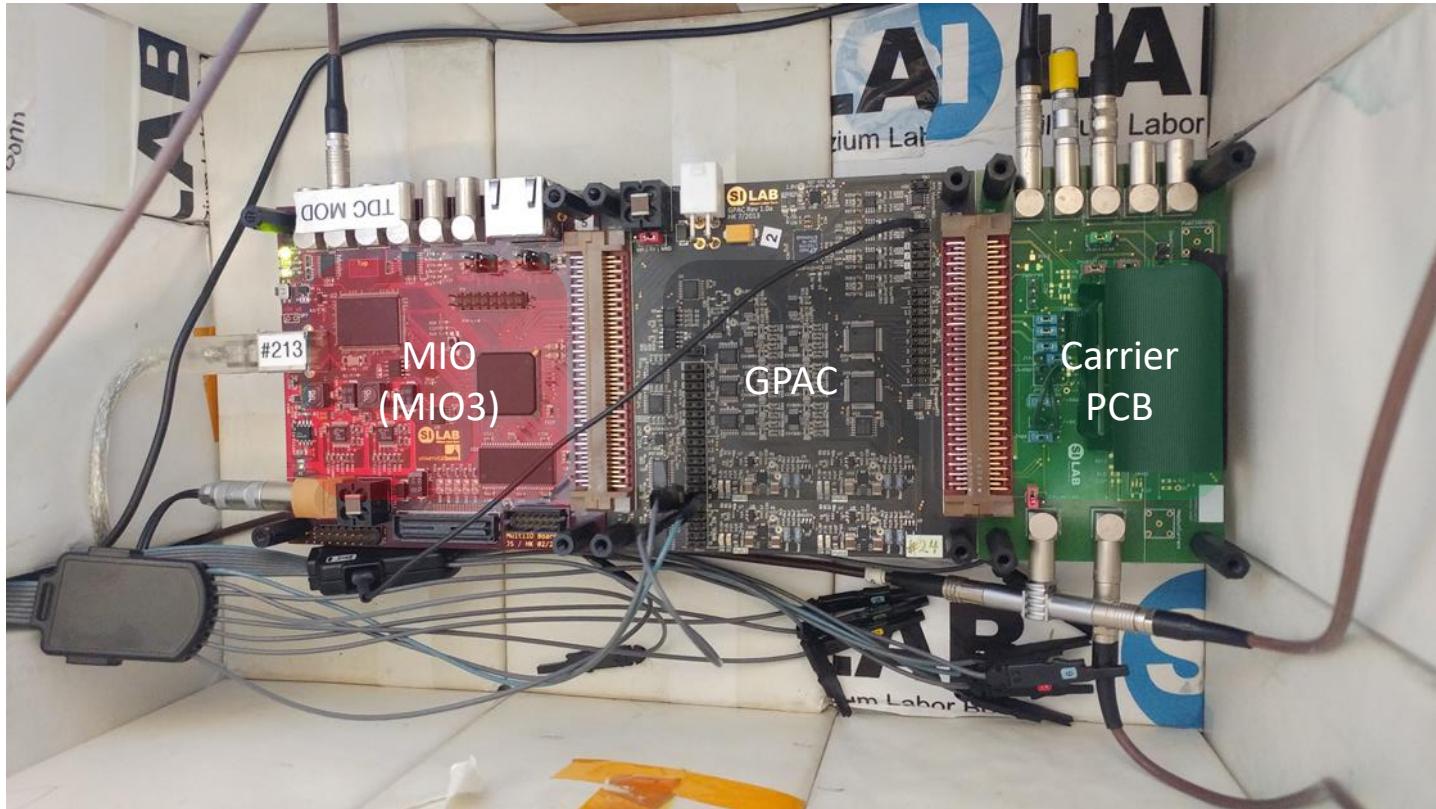


- Motivated by reducing C_D & cross talk
 - Less in-pixel electronic
 - Almost no CMOS signal distribution along the column
- One-to-one connection from pixel to R/O logic
 - HIT signal shape distorted by source follower
 - Complex routing
 - Layout design not easily scalable

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Measurement setup

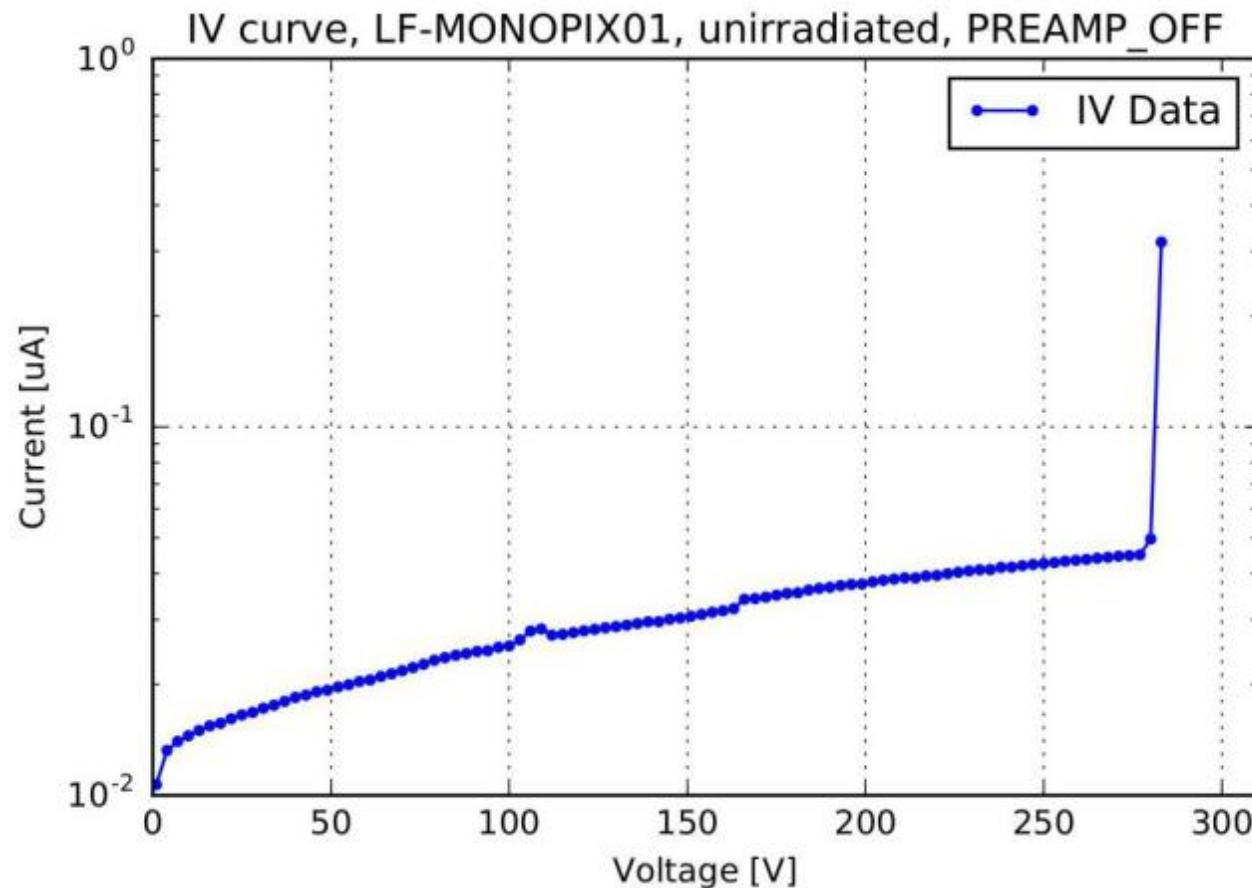


Full read-out firmware & software (under development) based on the BASIL framework:

https://github.com/SiLab-Bonn/monopix_daq

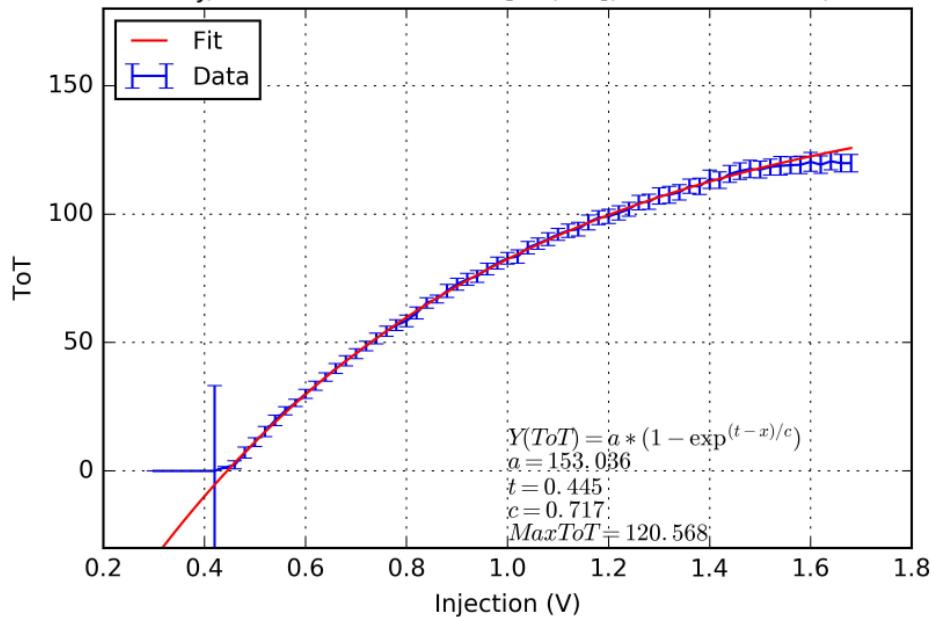
I-V curve

- Break down ≈ -280 V
- Tested on few chips, all show similar behaviour



Injection vs. ToT

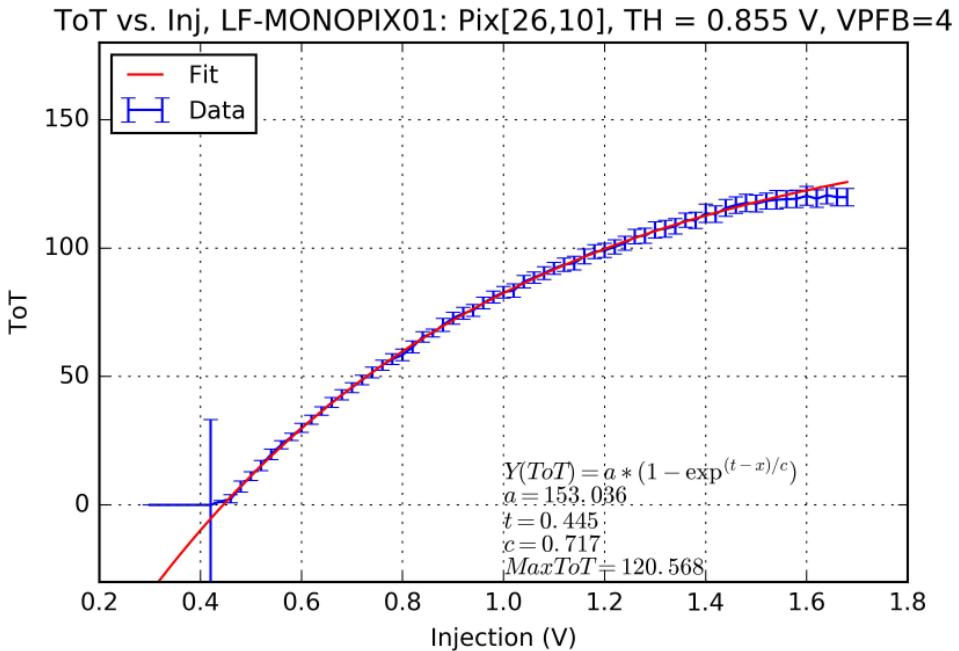
ToT vs. Inj, LF-MONOPIX01: Pix[26,10], TH = 0.855 V, VPFB=4



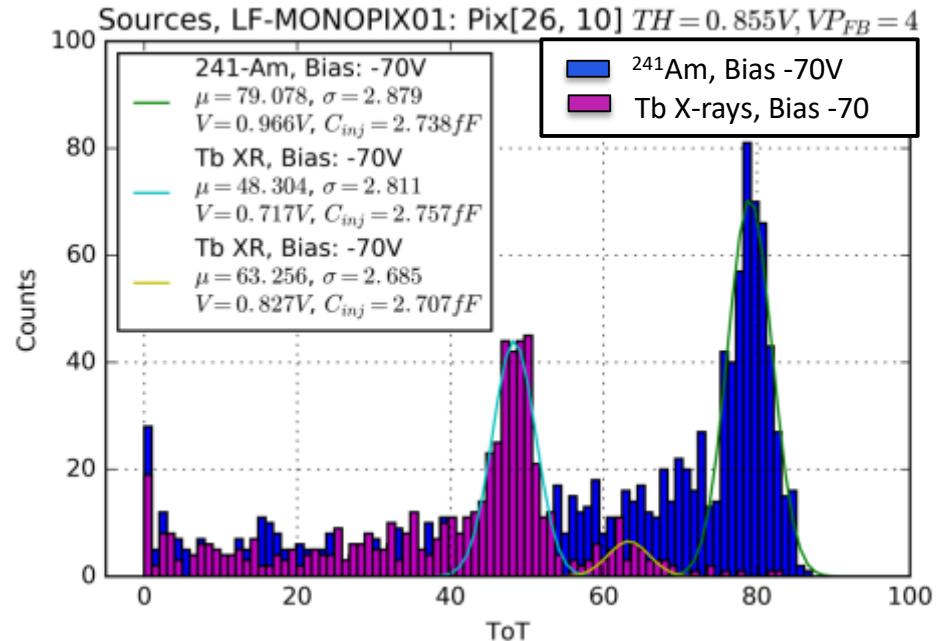
- Low feedback current for CSA to have wider analog pulse (not default shaping)
 - Larger ToT range to have better analog resolution for sensor characterization

ToT calibration & x-ray spectra

Injection vs. ToT



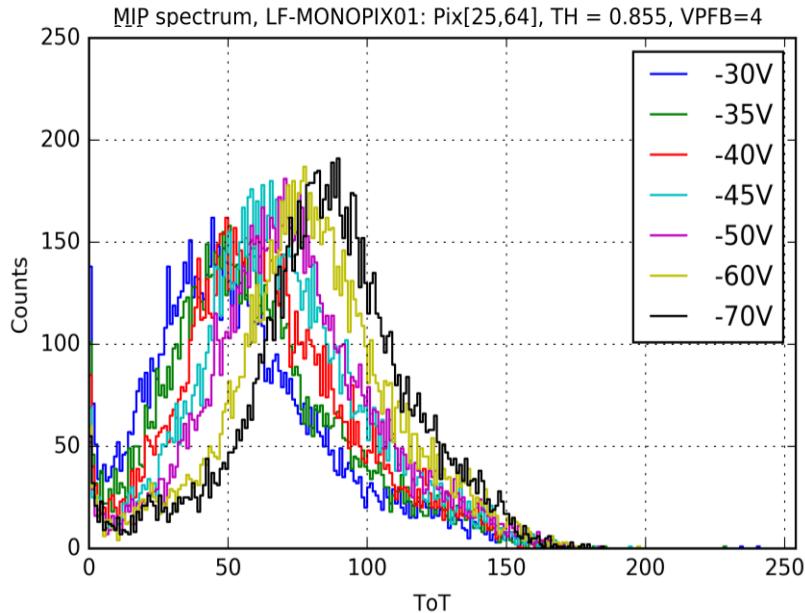
Source spectrum fit



- Low feedback current for CSA to have wider analog pulse (not default shaping)
 - Larger ToT range to have better analog resolution for sensor characterization
- Injection capacitance is measured $\left(C_{inj} = \frac{Q}{V_{inj}}\right)$ to be ≈ 2.75 fF

Depletion depth

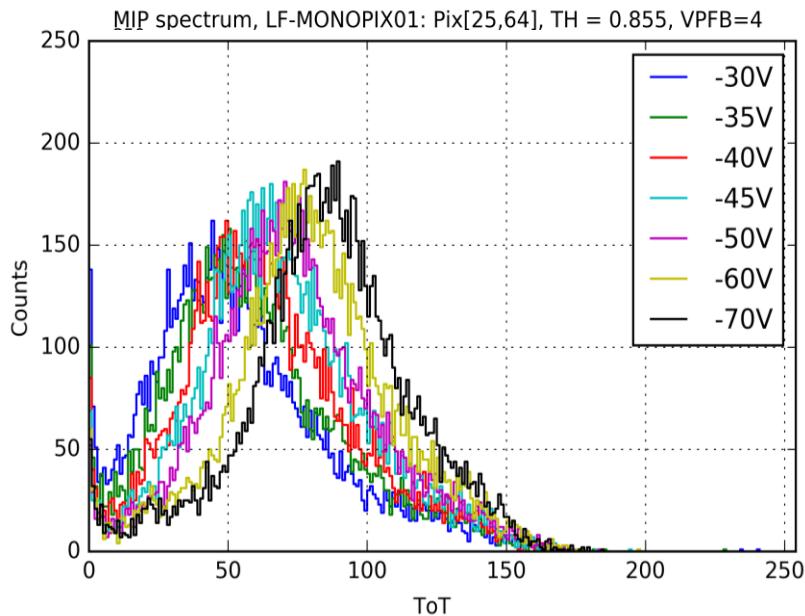
Spectrum vs bias voltage



- MIP spectra taken with 2.5 GeV electron beam at ELSA

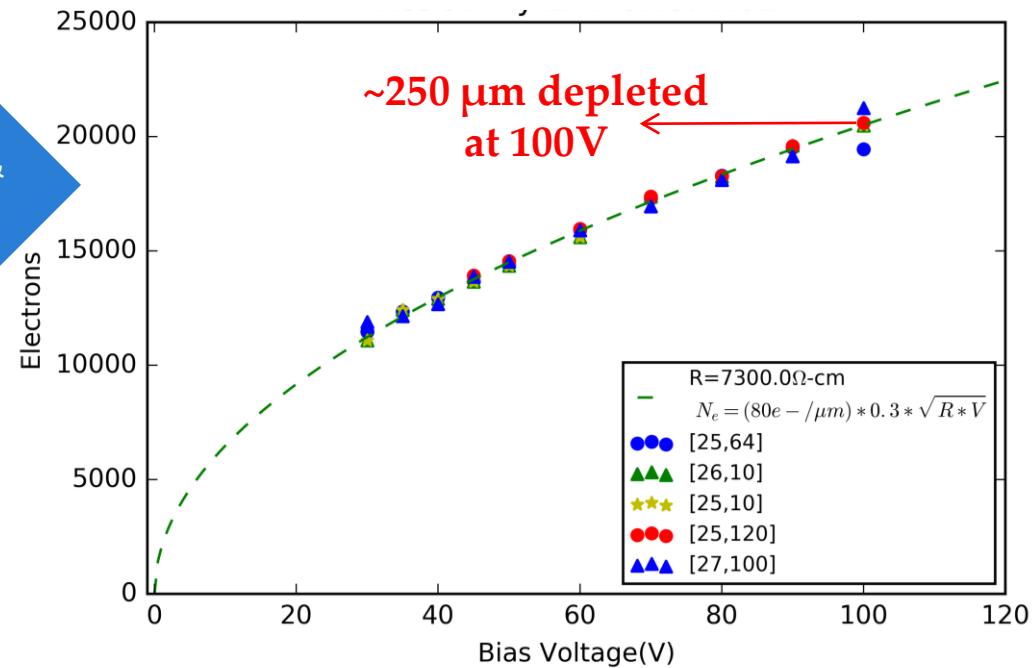
Depletion depth

Spectrum vs bias voltage



Calibrate & fit MPV

Resistivity fit

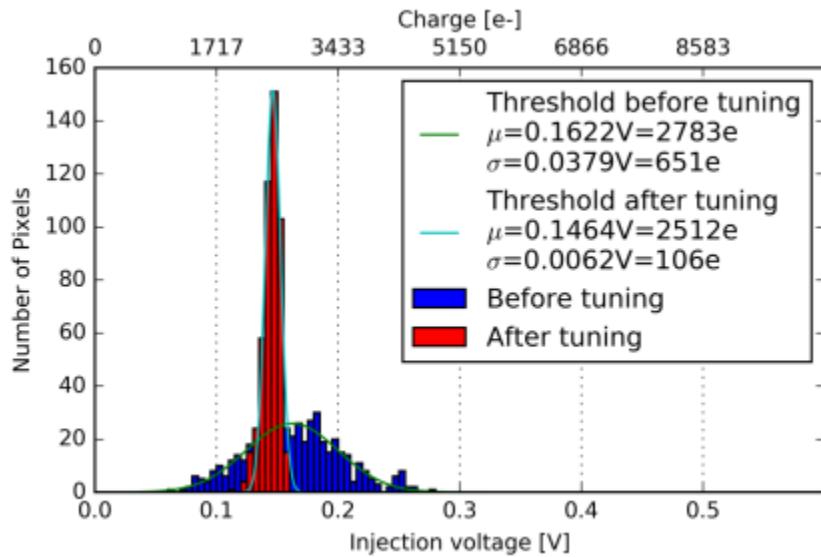


- MIP spectra taken with 2.5 GeV electron beam at ELSA
- Substrate resistivity $\approx 7.3 \text{ k}\Omega\text{cm}$ (higher than previous prototypes, but within specification)

Threshold tuning

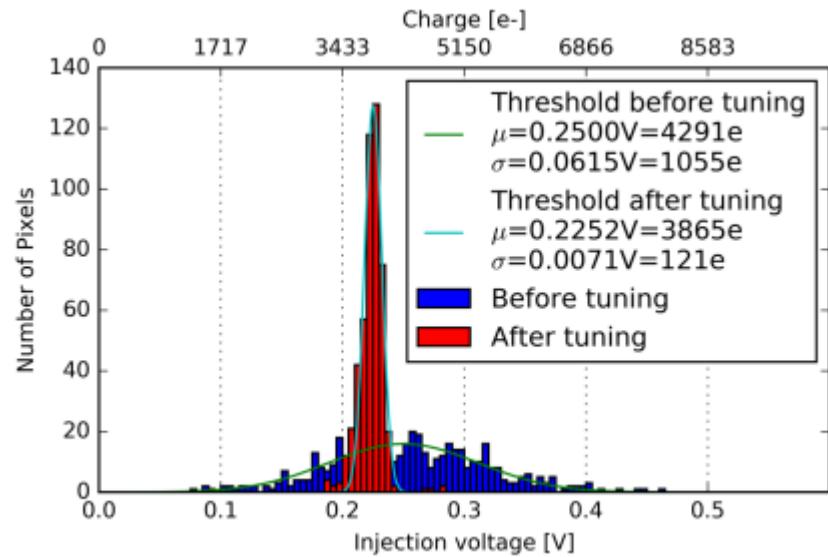
Column 24 -27

- CMOS input CSA
- Discriminator V1
- In-pixel RO logic



Column 20 -23

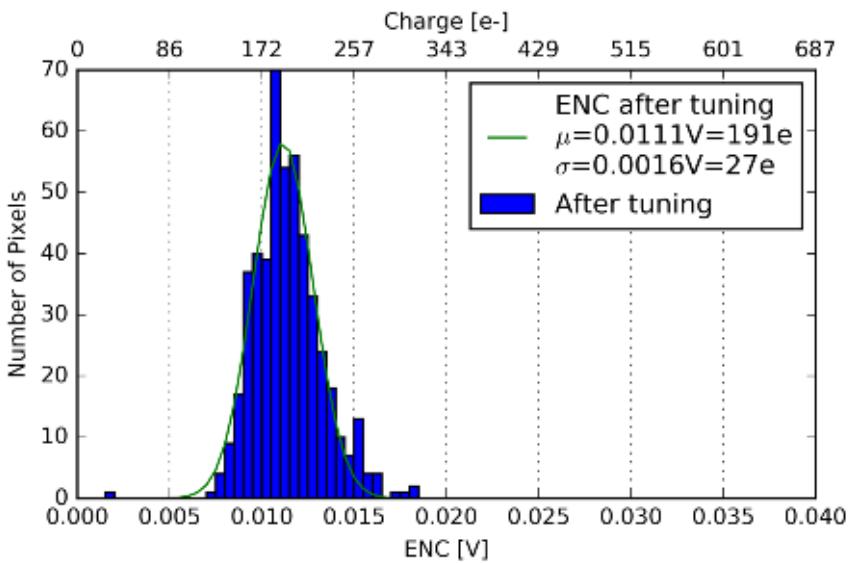
- CMOS input CSA
- Discriminator V2
- In-pixel RO logic



- The threshold can be tuned to ≈ 2500 e⁻ with dispersion of ≈ 100 e⁻
- Algorithm under improvement, a lower tuned threshold may be achievable

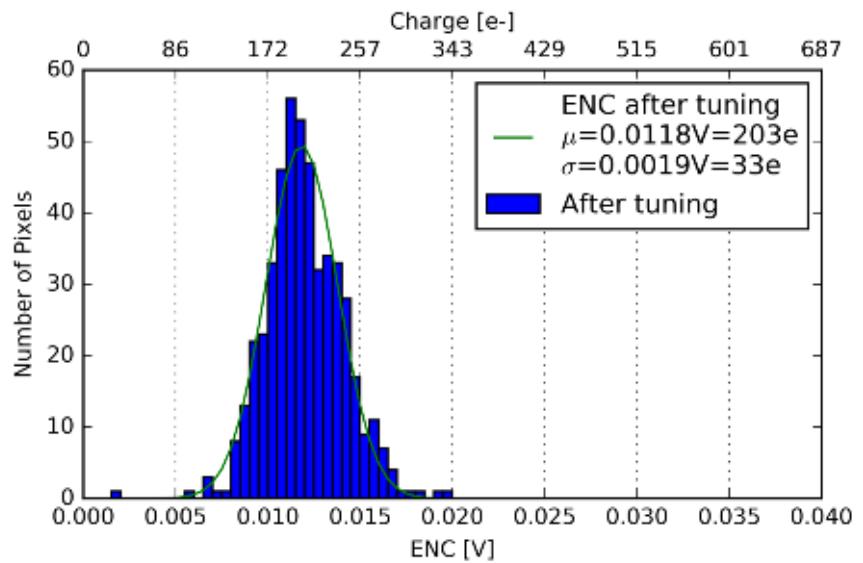
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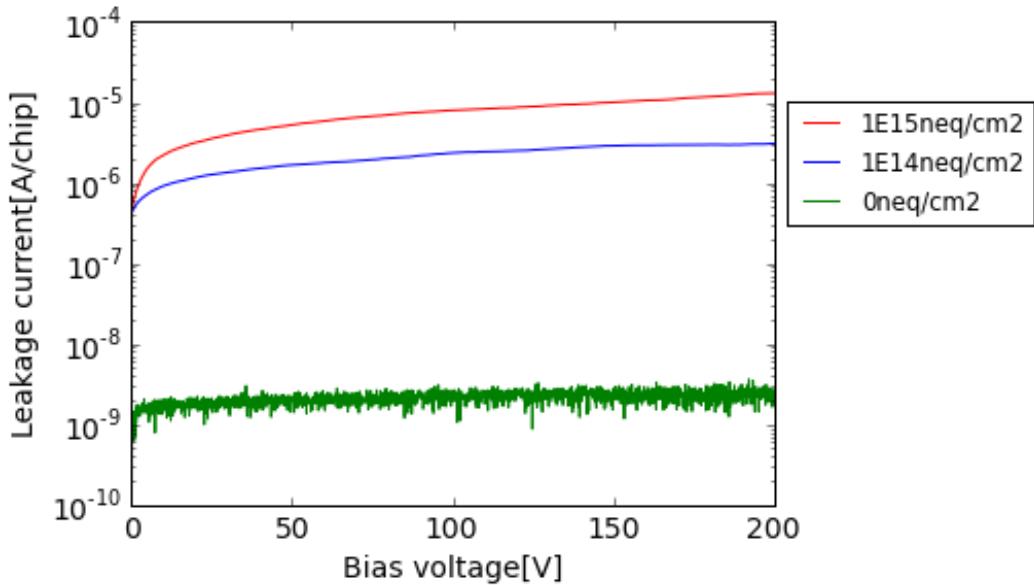
- CMOS input CSA
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- ENC ≈ 200 e⁻ with dispersion of ≈ 30 e⁻
- Other flavors under investigation

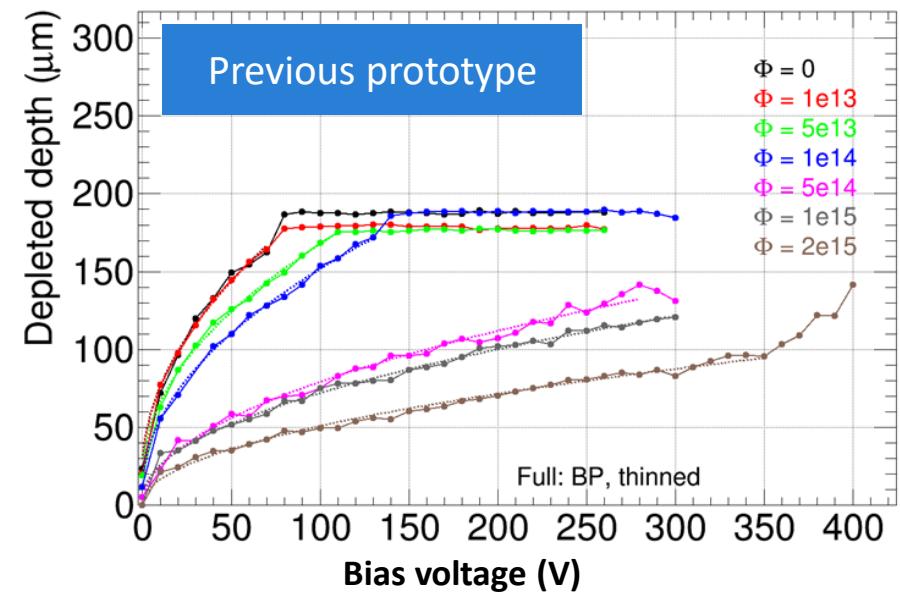
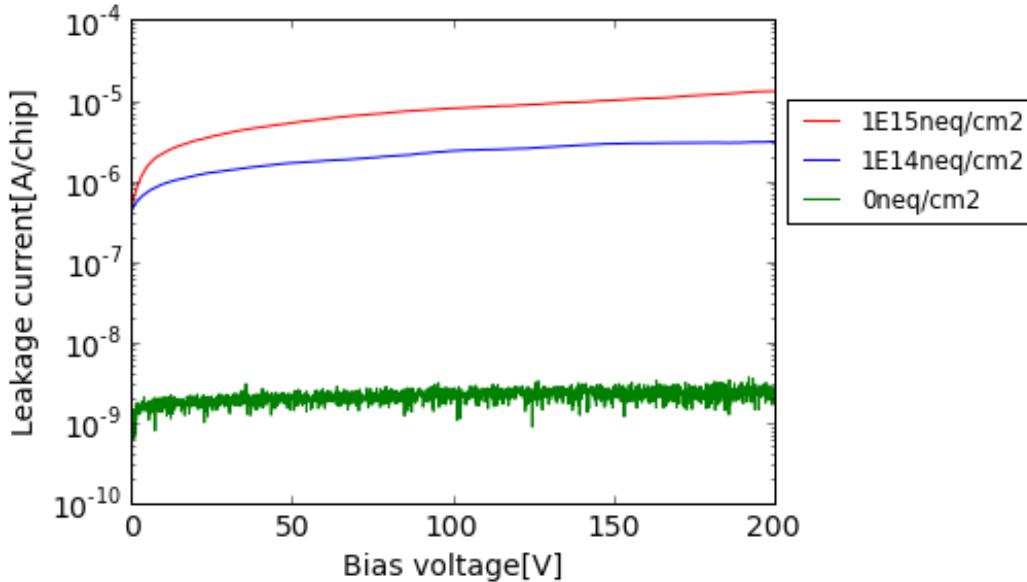
Irradiation

- Irradiation done by University of Ljubljana: 10^{14} , $5 \cdot 10^{14}$, 10^{15} , $5 \cdot 10^{15} \frac{n_{eq}}{cm^2}$
- IV curve measurement (at -25 °C) shows increased leakage, breakdown > 200 V
- At $10^{15} \frac{n_{eq}}{cm^2}$ chip is still fully functional, threshold dispersion slightly increased



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- Based on previous prototype >100μm depletion after $10^{15} \frac{n_{eq}}{cm^2}$ expected



E-TCT measurement on LF test structures thinned to 200μm
I. Mandić, RD50 workshop 2017

- Proton irradiation done by CPPM, data analysis ongoing

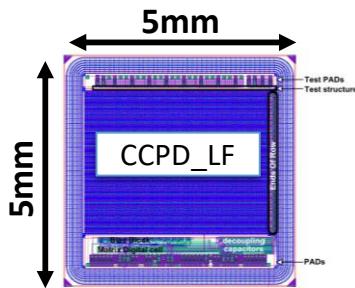
- A prototype monolithic sensor was designed in 150nm CMOS process and manufactured on a HR wafer
- Chip are being tested presently and measurement results are in agreement with simulation predictions
- Monolithic R/O works and threshold of $2500 e^-$ was achieved, lower value probably possible
- Backside processing and thinning to be done
- Efficiency measurements and radiation tolerance tests are starting now

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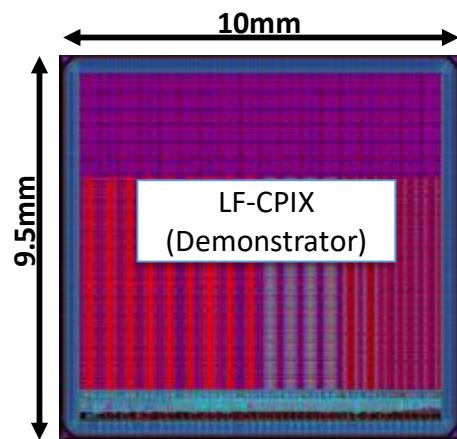
Backup

LF prototypes



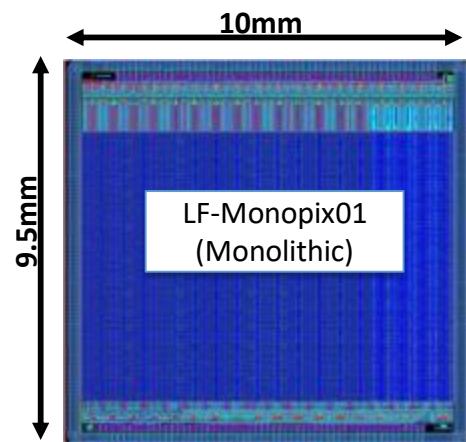
CCPD_LF

- *Subm. in Sep. 2014*
- $33 \times 125 \mu\text{m}^2$ pixels
- *Fast R/O coupled to R/O chip*
- *Standalone R/O for test*



LF-CPIX (DEMO)

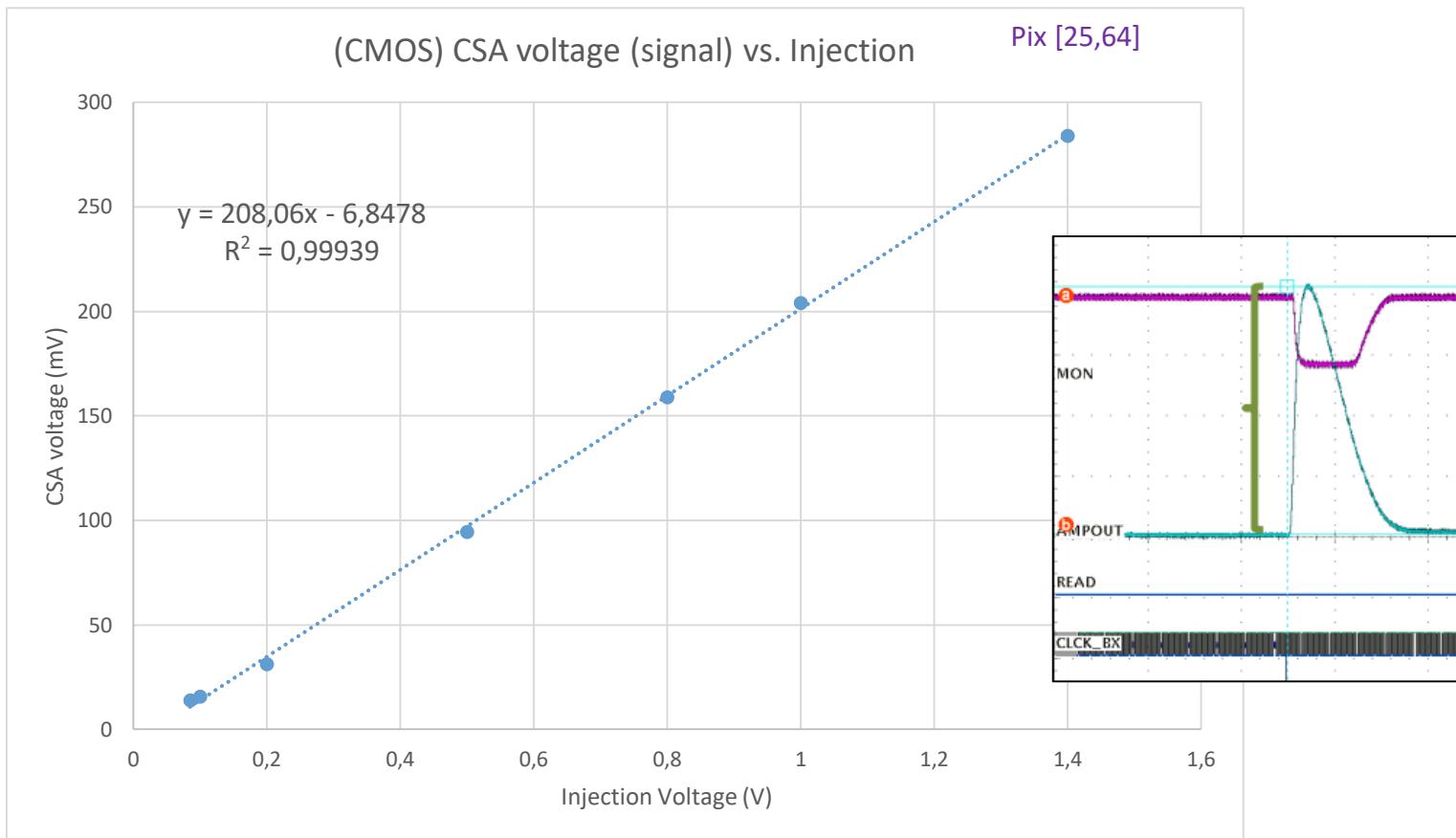
- *Subm. in Mar. 2016*
- $50 \times 250 \mu\text{m}^2$ pixels
- *Fast R/O coupled to R/O chip*
- *Standalone R/O for test*



LF-Monopix01

- *Subm. in Aug. 2016*
- $50 \times 250 \mu\text{m}^2$ pixels
- ***Fast standalone R/O***
- *Standalone R/O like LF-CPIX*

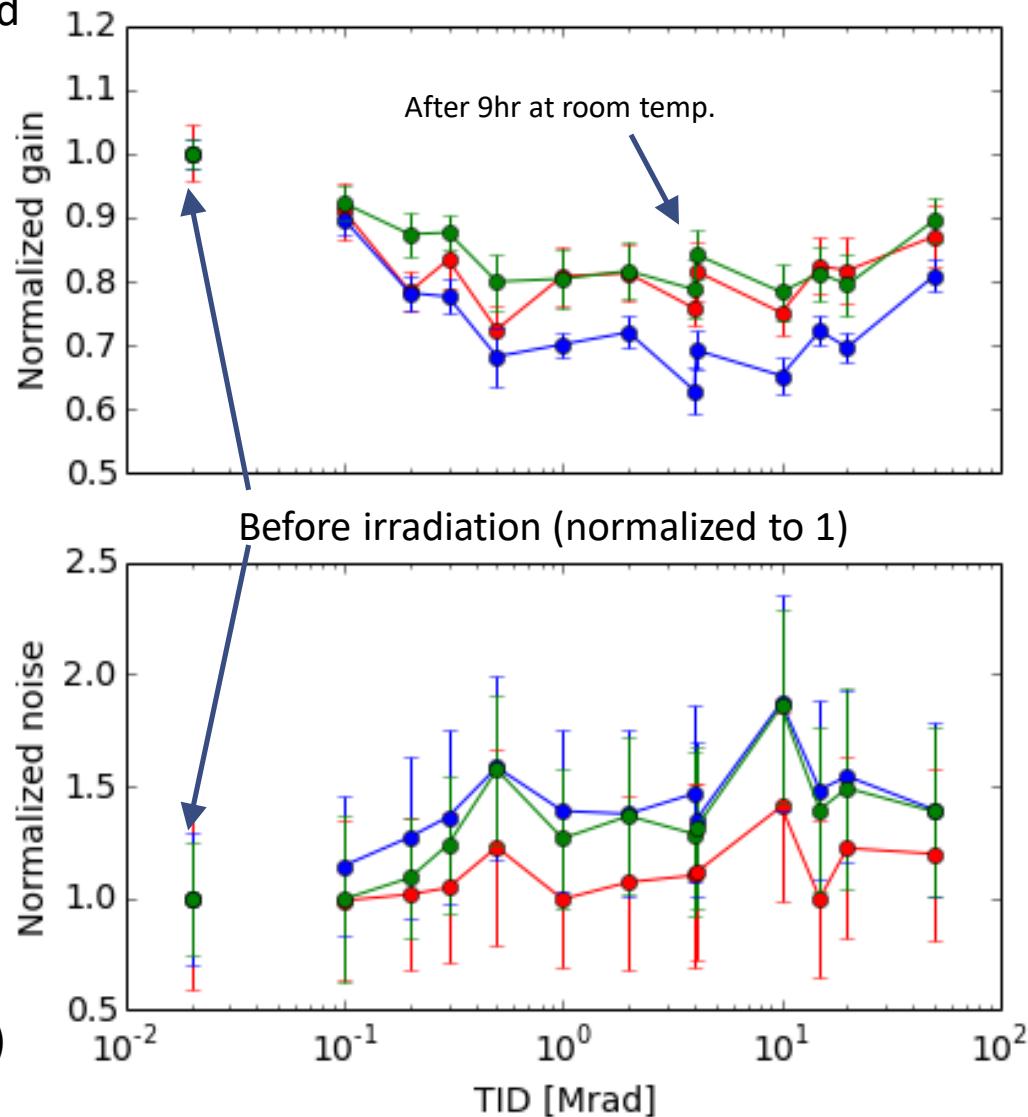
CMOS CSA linearity



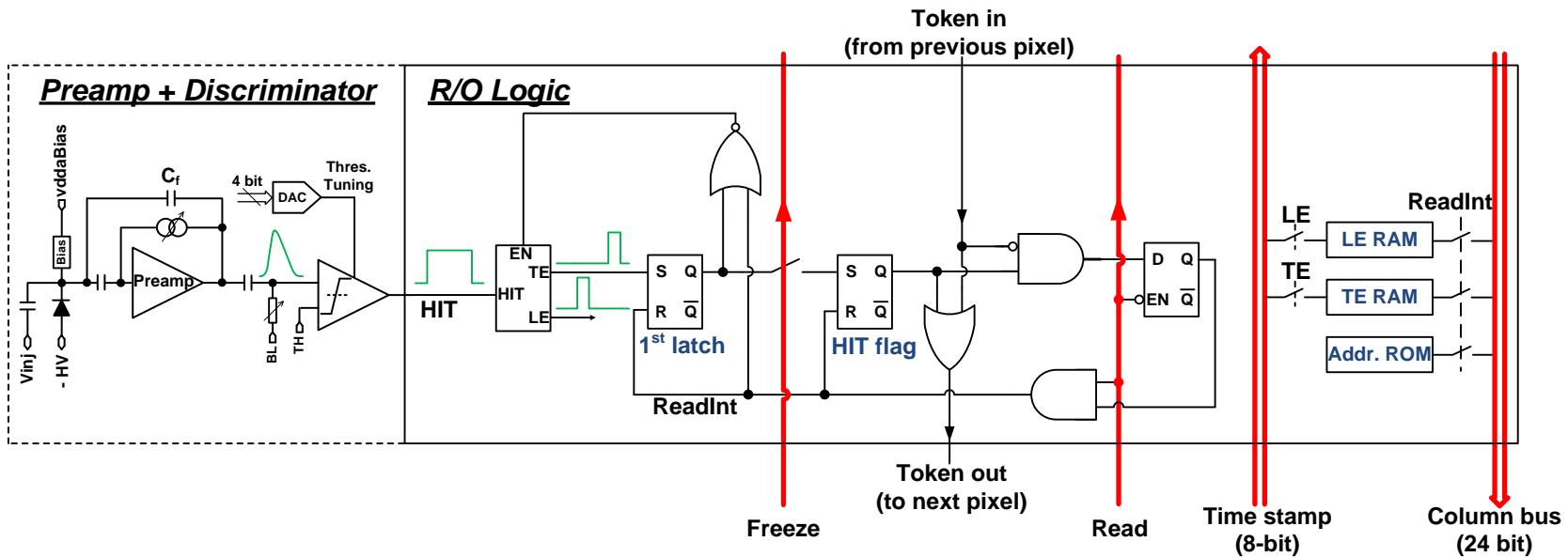
The CMOS CSA has a linear response to injected charge (ToT -as expected- not linear due to the fast return to baseline)

TID effects on CSA in ccpd-If

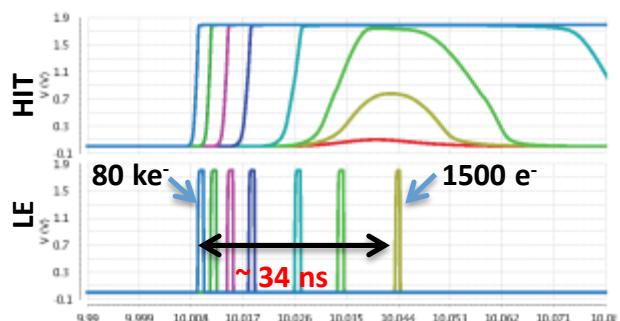
- Gain and noise of readout measured before and after X-ray ($\sim 60\text{keV}$) irradiation
- TID: 50Mrad (outer layer of ATLAS-HL-LHC)
- Flavors of CSA feedback (version A)
 - Normal ($L=0.9\mu\text{m}$)
 - Long ($L=1.5\mu\text{m}$)
 - ELT ($W\approx 2.4\mu\text{m}$, $L\approx 0.16\mu\text{m}$)
- Readout works after irradiation
 - Gain degraded to 70-80%
 - Approx. twice larger noise
- No significant differences between flavors
- More irradiation studies are coming (24GeV p $^+$)



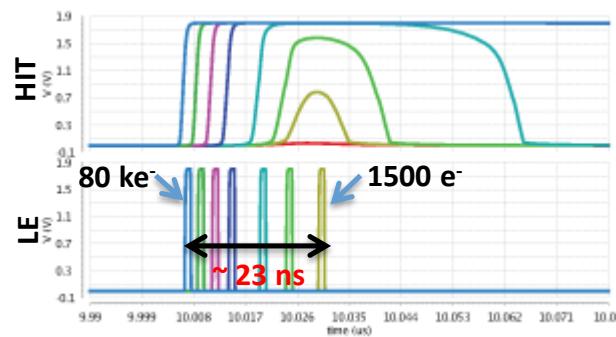
Time walk simulations



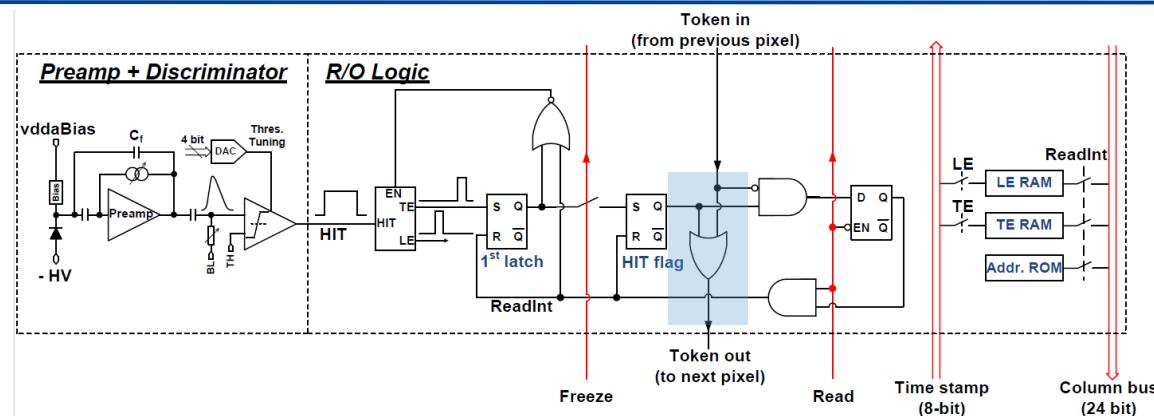
NMOS pre-amp. + Dis. V1, Threshold=1500e⁻



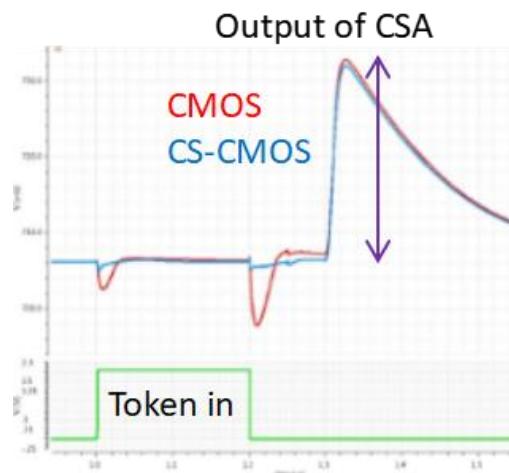
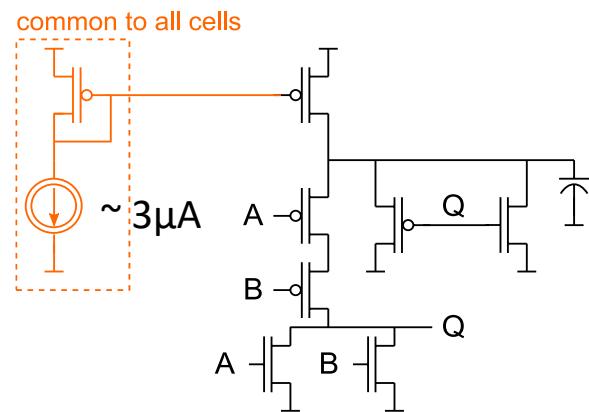
NMOS pre-amp. + Dis. V2, Threshold=1500e⁻



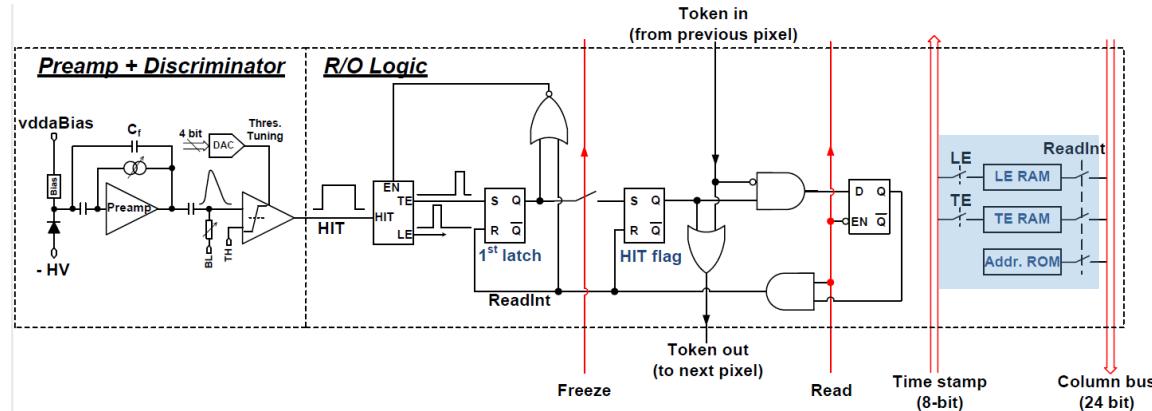
Cross talk minimization efforts in LF-MONOPIX01



Current steering logic for TOKEN propagation



Cross talk minimization efforts in LF-MONOPIX01



Source followers used for SRAM R/O

