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Development of Depleted Monolithic Pixel Sensors in 150 nm CMOS technology for the ATLAS Inner Tracker Upgrade

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This work presents a Depleted Monolithic Active Pixel Sensor (DMAPS) prototype manufactured in LFoundry 150 nm CMOS process. The described device, named LF-Monopix01, was designed as a proof of concept of a fully monolithic sensor capable of operating in the environment of outer layers of ATLAS Inner Tracker upgrade for High Luminosity LHC. Implementing such device in the detector will result in a lower production cost and lower material budget compared to presently used hybrid designs. In the presentation the chip architecture will be described, followed by simulation and measurement results.

Summary

There has recently been an increased interest within the high energy physics community in employing CMOS manufacturing processes to develop active silicon pixel sensors on depletable substrates. In order to better organize the design efforts an R&D collaboration called "CMOS demonstrator"was started within ATLAS with a goal of qualifying the available CMOS technologies to build depletable high performance and cost efficient CMOS detectors with low material budget for the ALTAS ITk upgrade. Within this collaboration several prototypes have been developed in few different technologies. Presented measurement results were encouraging, showing that CMOS sensors might be a feasible choice for ATLAS ITk, but vast majority of designs developed so far were either passive sensors or sensors with an integrated first stage of analog front-end, thus still requiring bump-bonding or gluing to a dedicated readout chip. A natural next step is an attempt to integrate sensor, analog front-end and readout circuit into one chip. This paper presents such a device – a DMAPS prototype baptized LF-Monopix01 designed in LFoundry 150 nm CMOS technology. The chosen process features quadruple wells and a charge collection node is formed by a very deep N-well embedding the in-pixel electronics. A deep P-type layer allows isolating transistor N-wells from the very deep N-well, so that full CMOS capability is achieved within the pixel. The readout of the pixel array follows the "column drain"architecture. In every pixel, the charge signal is first amplified by a Charge Sensitive Amplifier (CSA), and then compared to an adjustable threshold by a discriminator. Two 8-bit time stamps corresponding to the leading and trailing edge of the discriminator output, respectively, are stored in RAM cells. A hit in a pixel initiates token signal propagation to a readout controller, which initiates the priority scan, such that hit pixels are successively read out. The data is serialized and sent off-chip at a rate of 160 Mbps by a LVDS driver. For design simplicity, the readout controller is implemented off-chip in a FPGA.

The design contains a matrix of 129×36 pixels, with a pixel size of 250 µm × 50 µm. The matrix is composed of 9 pixel flavours, evenly distributed into four columns each. The flavours differ by designs of the CSA architecture (2 types), the discriminator architecture (2 main types) and the placement of pixel readout circuitry (in-pixel or at the periphery).

The design was fabricated on a high resistivity (> 2 kOhm•cm) P-type substrate. First measurement results show that readout circuitry is fully functional and sensor breakdown voltage is above 280 V. During the presentation the prototype will be described in detail, followed by simulation results and the latest measurements results.

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