KLauS4:
A Multi-Channel SiPM Charge Readout ASIC

K. Briggl, H. Chen, Y. Munwes, V. Stankova, Z. Yuan

W. Shen, H.C. Schultz-Coulon

KIP, Heidelberg University

Kirchhoff-Institute for Physics

UNIVERSITÄT HEIDELBERG
ZUKUNFT SEIT 1386

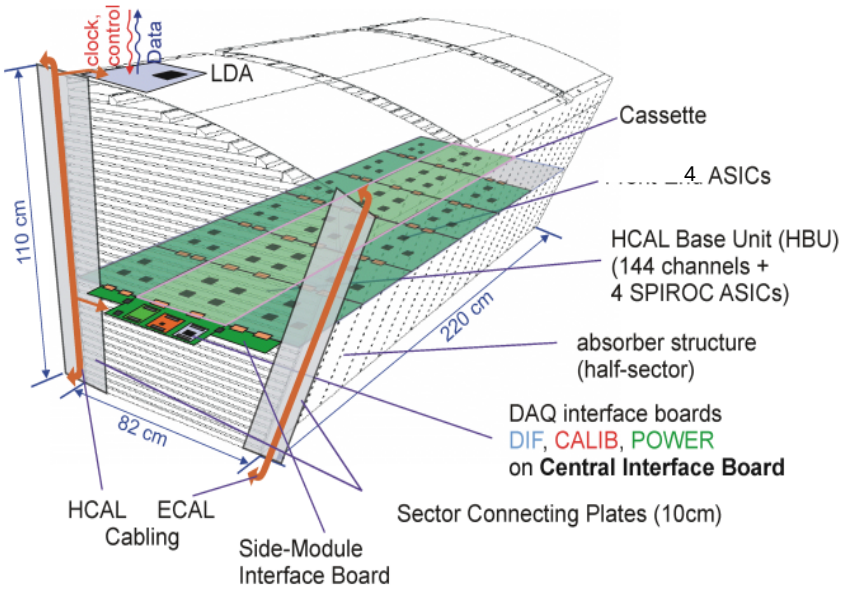
Applications

Analog Hadronic CALorimeter (AHCAL) for the Future Linear Collider

Design requirements:

Charge measurements for Silicon Photomultiplier signals

- ✔ Fully integrated: Front-end + Digitization
- ✔ **Low power consumption**
  - ✔ Severals million channels in the dense AHCAL
  - ✔ 25uW/ch with power-pulsing (> 0.5% duty cycle)
  - ✔ No active cooling
- ✔ **Low noise:** precise charge measurements
  - ✔ SiPM gain calibration
  - ✔ Single photon spectra for small gain devices
- ✔ **Large dynamic range**
  - ✔ Large number of SiPM pixels

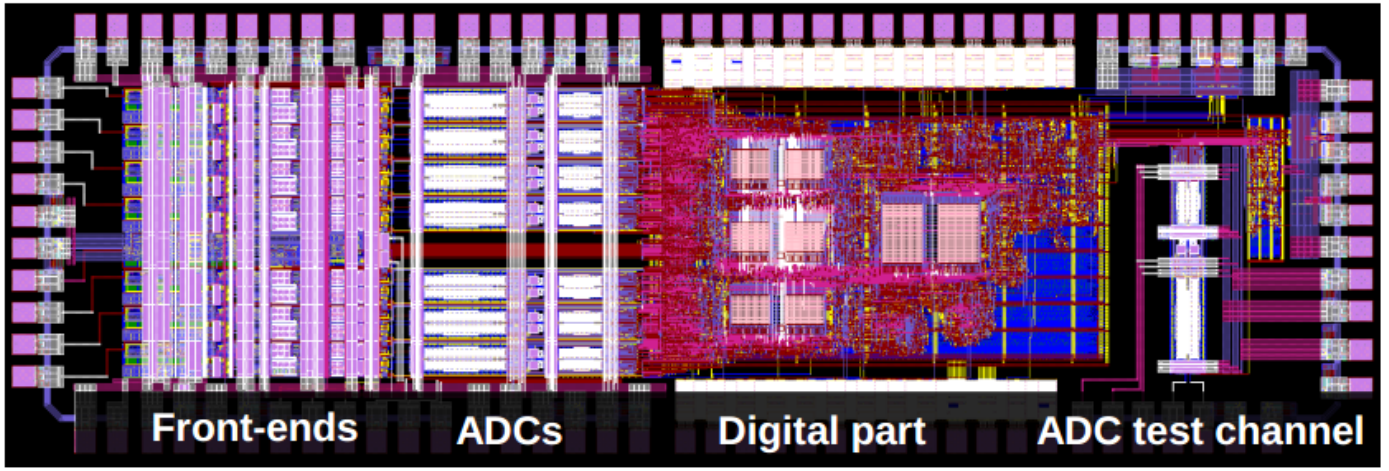


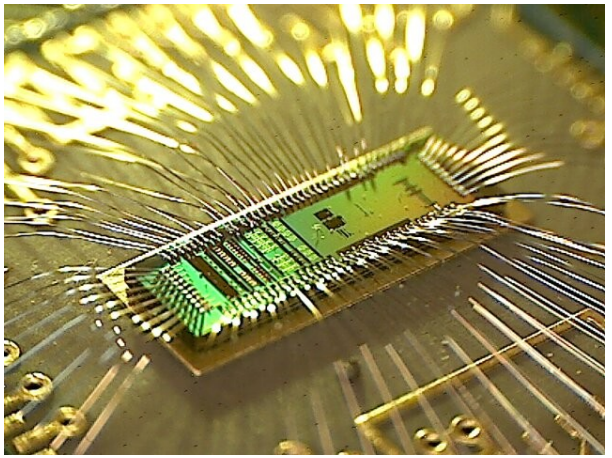
Overview

- KLauS4 : 7 channel prototype ASIC
  - ASIC structure
  - Characterization measurements
  - Test-beam results
- Summary

KLauS4: 7-channel prototype

KLauS - Kanäle zur Ladungsauslese für Silicon Photomultiplier

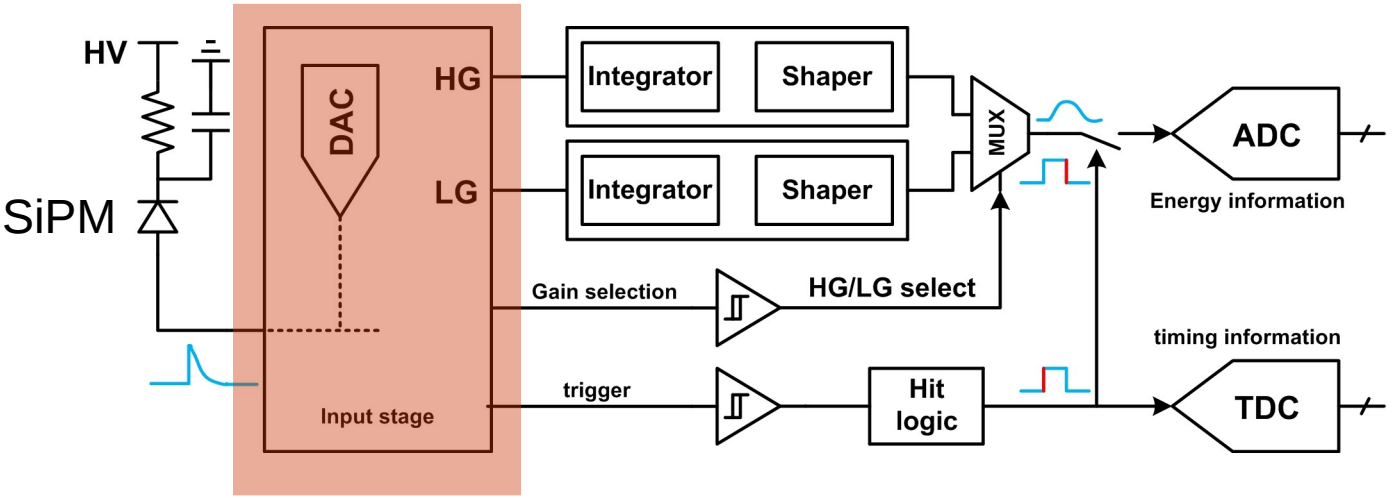




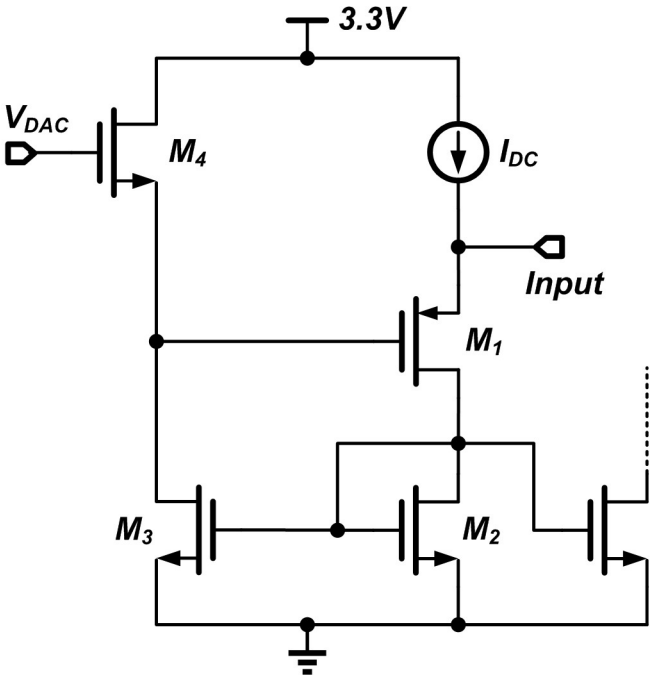
Submitted in May 2016

- **Mixed-mode** prototype
- UMC 180nm CMOS, 1.5 x 4.5 mm^2 mini-ASIC
- **7 channels** (Front-end + ADC + Digital control block)
- TDC with 25ns binning
- Fast LVDS (160 Mbit/s) or I2C link for data transfer
- SPI for slow control

Inside structure: Front-end

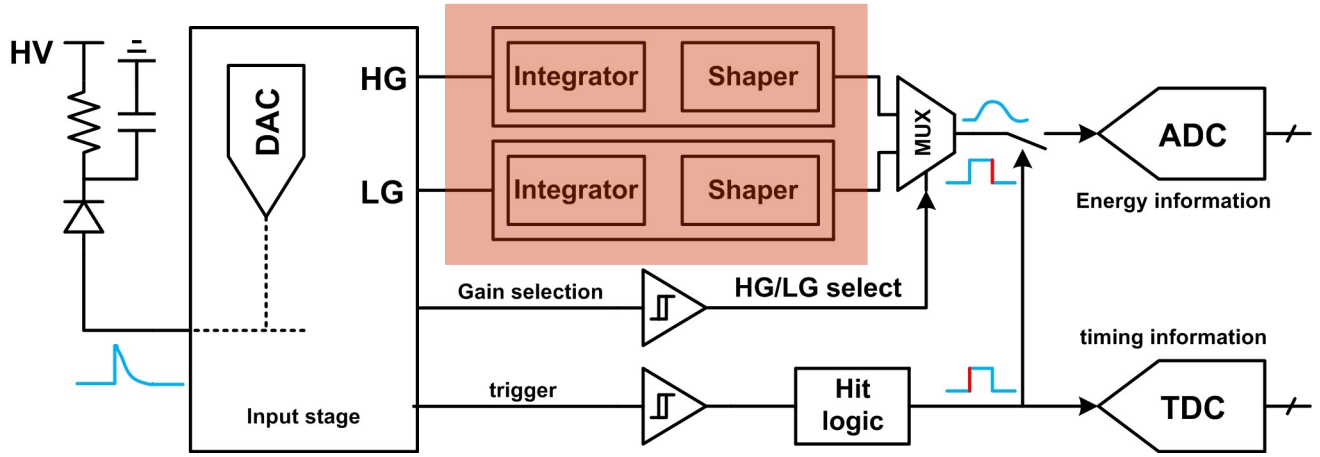


Channel block diagram

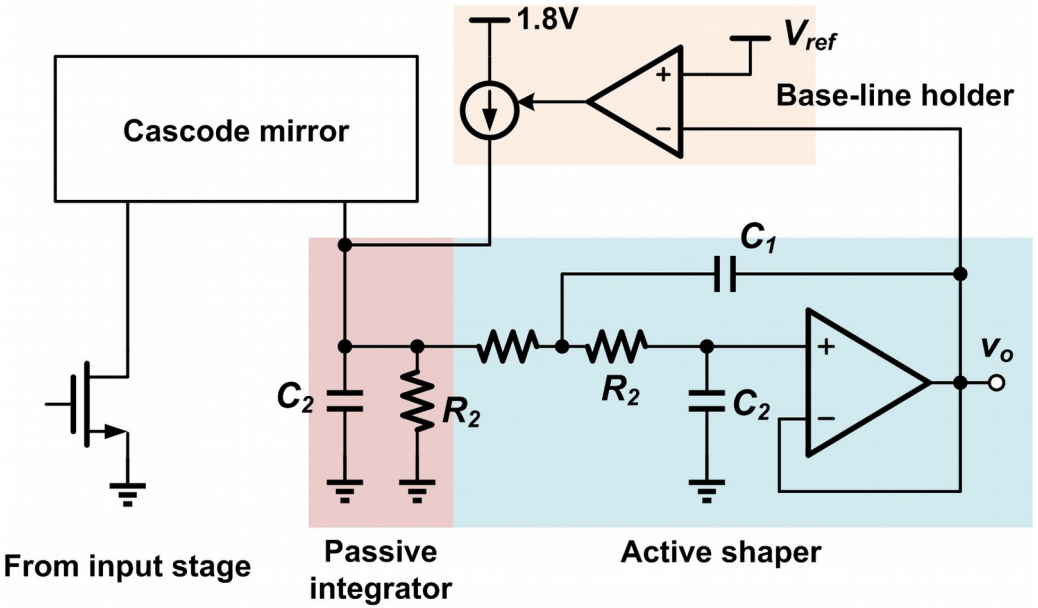


- **Front-end**: *Input stage, 2 integration branches, 2 comparator, ADC and TDC*
- **low input impedance:** *Common-gate structure + current feedback*
- **8b-DAC** - SiPM bias voltage tuning
- **Power-gating** functionality

Inside structure: Front-end

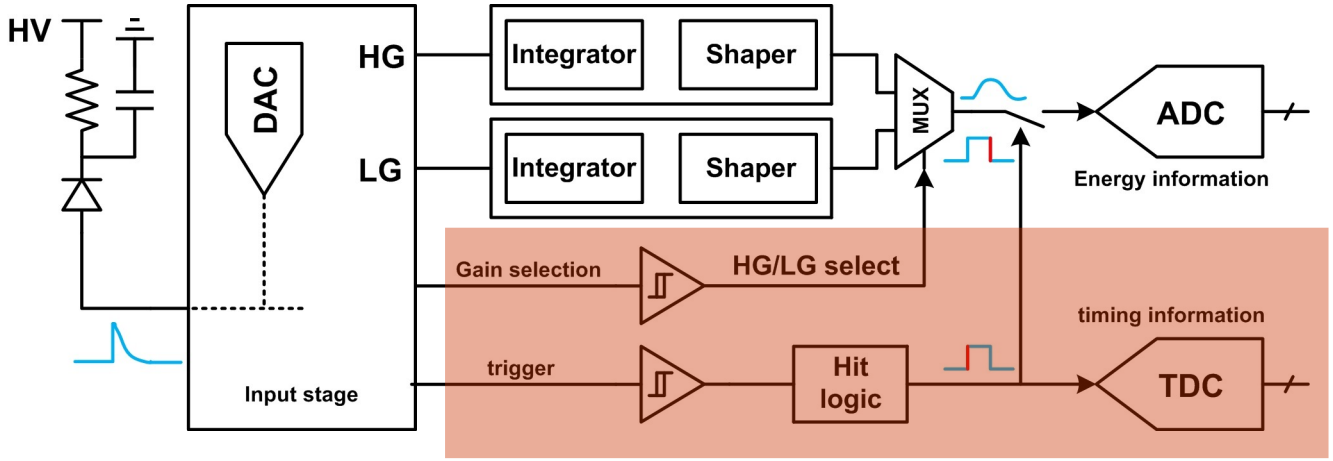


Channel block diagram



- **Two integration branches**
  - **High Gain** – *for calibration (single photon spectrum)*
  - **Low Gain** – *for large SiPM signals*
- **Charge integration stage**
  - Passive integrator
  - Active shaper
  - Sub-threshold region base- line holder *to stabilize the pedestal*

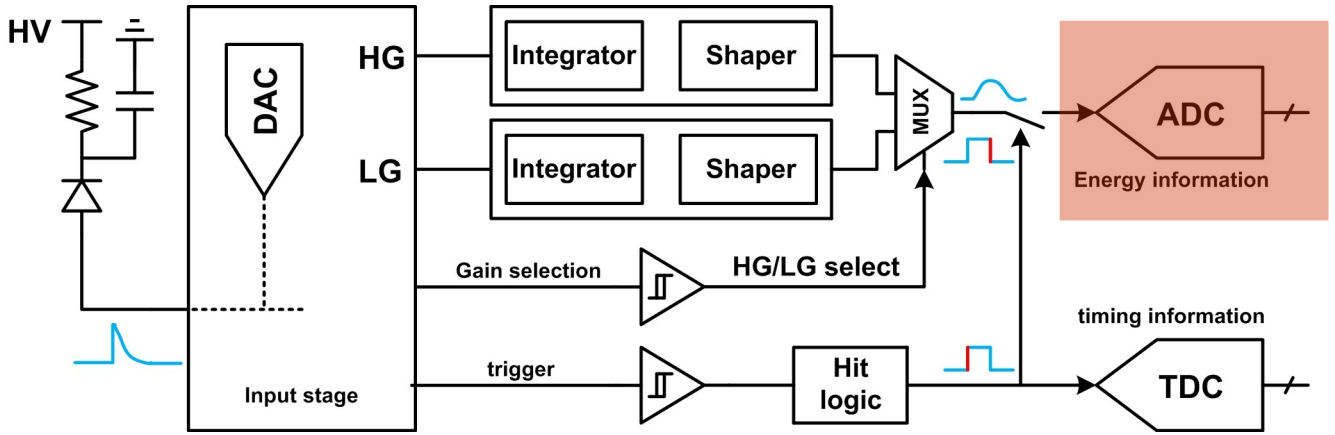
Inside structure: Front-end



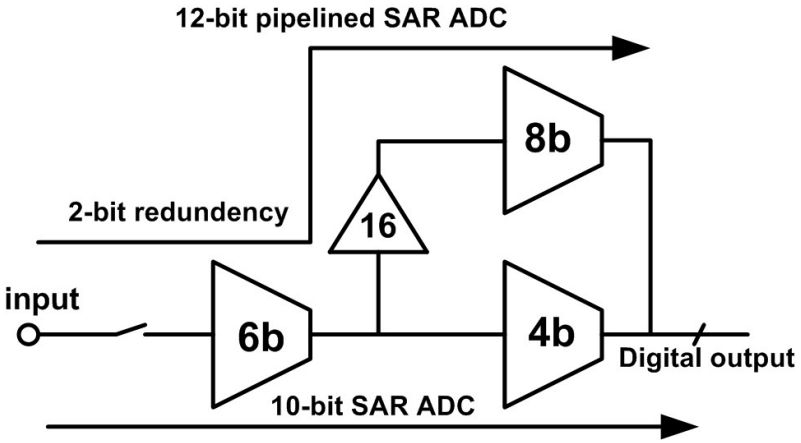
Channel block diagram

- **Gain selection comparator** → which branch to be digitized
  - Auto gain select is also possible
- **Time comparator**
  - **TDC** → time reference
  - **Hit logic** → delay the trigger signal *(hold delay)* initiate the ADC sampling.

Inside structure: ADC

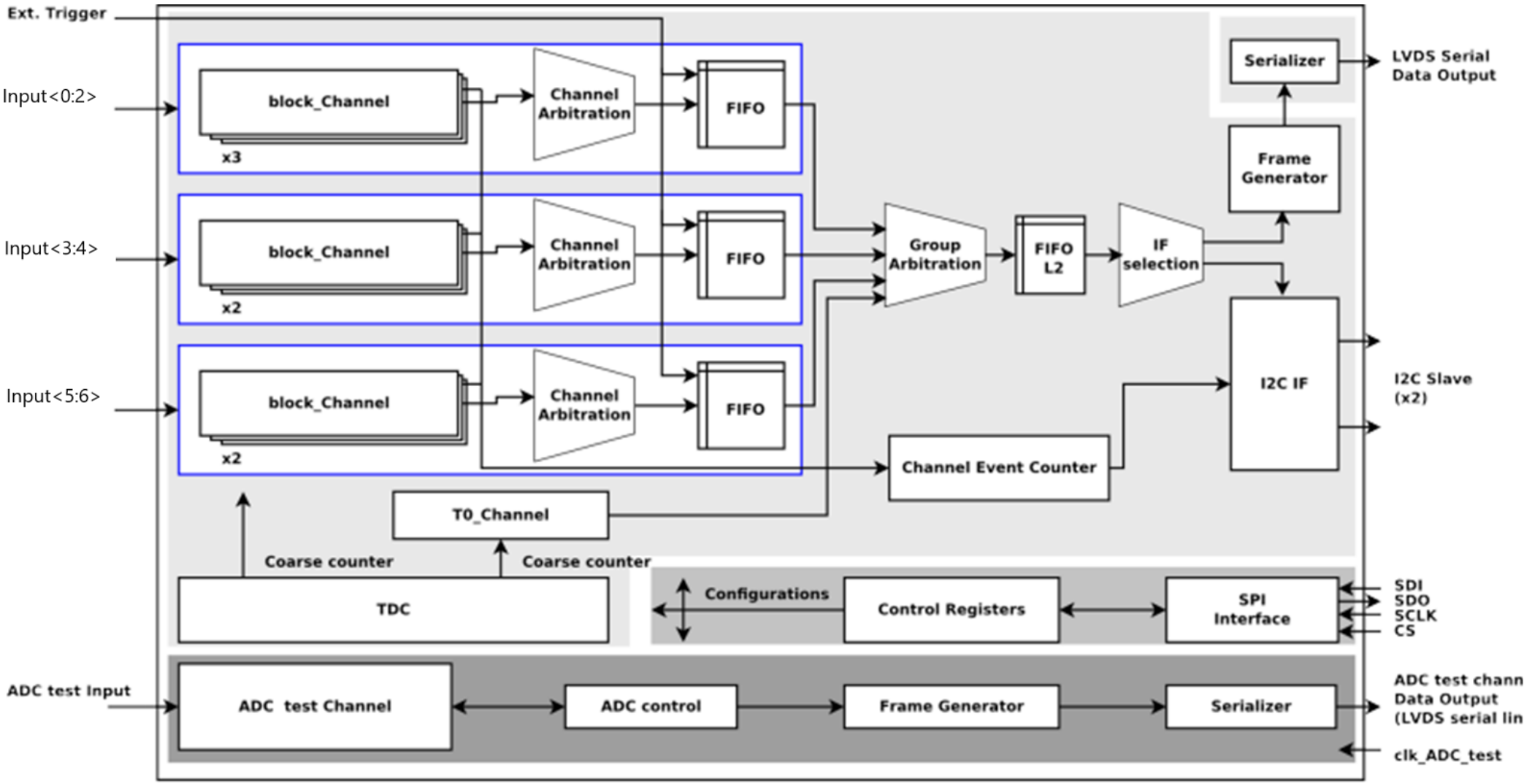


Channel block diagram



- Implemented – **SAR ADC** with structure type of Monotonic capacitor switching procedure (MCS) → to save power and area
- **Two configuration**:
  - 10-bit ADC – MIP quantization (SAR ADC)
  - 12-bit ADC – SiPM calibration (pipeline SAR)
- **Sampling rates** ~ 3Msps (10-bit ADC)

ASIC block diagram



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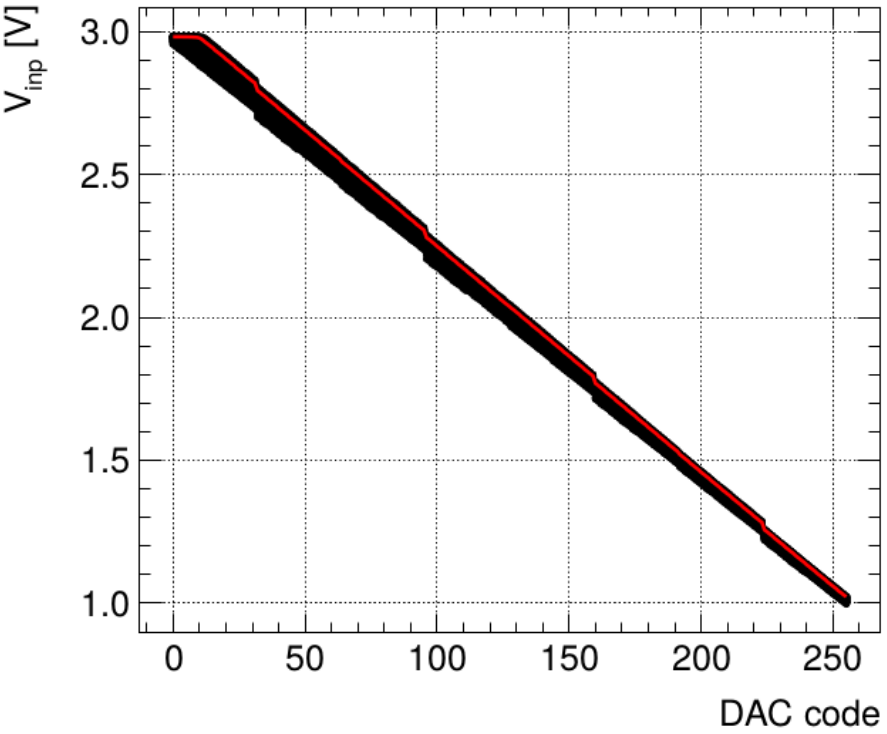
SiPM bias tuning

- **Linearity and range** of the 8-bit voltage input DAC
  - Always on: Low power (1-2nA/LSB)
  - For each configured DAC value the voltage at the input terminal has been measured.
  -
- **Measured 3 boards, 7 channels each**
  - Monotonic behavior
  - Tuning range of 2V as required
  - The differential non-linearity is due to mismatch in the current mirrors of the DACs.



ADC characterization

Linearity measurements:

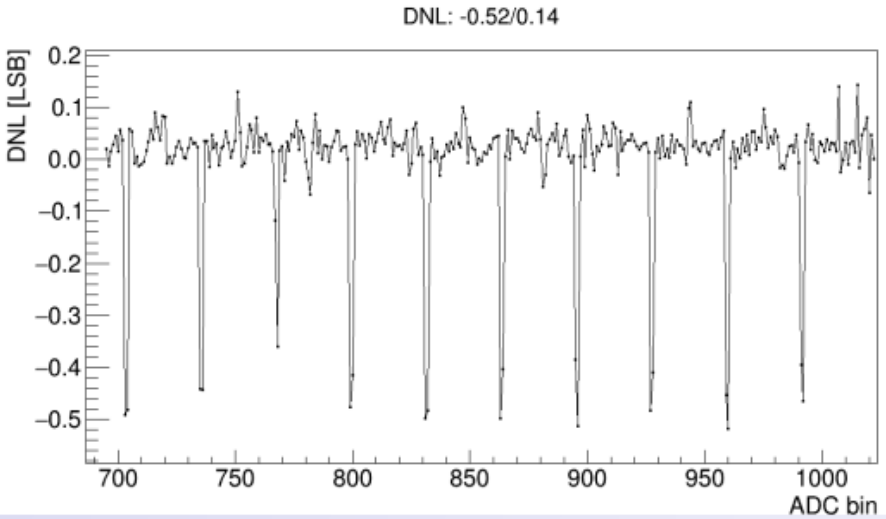
Used an external DC voltage source at the ADC input , voltage sweep (0.5~1.7V) – *front-end output voltage.*

- **10-bit ADC:**
  - Dynamic range: -1.62~1.62V → LSB~3.2mV

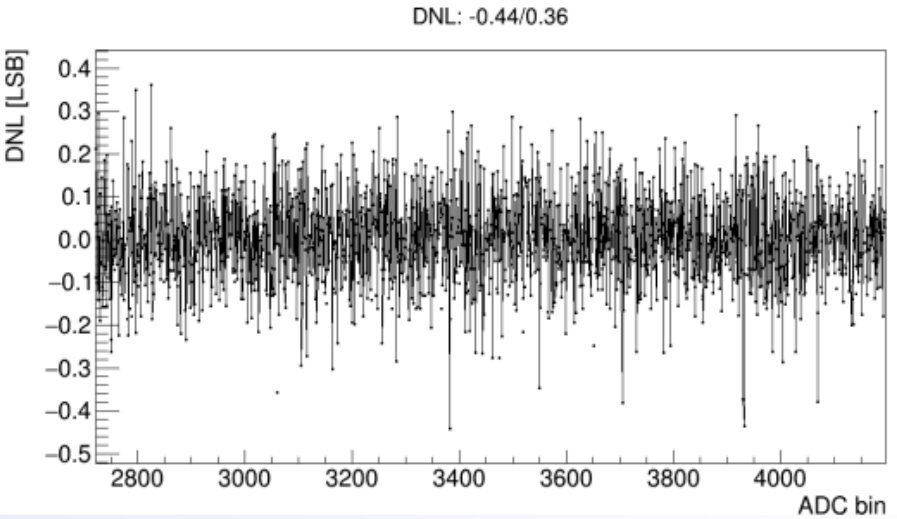
    Smaller than the reference voltage of 1.8V. Possible cause a parasitic capacitance from the MSB array to GND.
  - Nonlinearity every 32 bits from large bridge parasitics capacitor
  - Can be calibrated after ADC characterization
  - Corrected in the next version

- **12-bit ADC:** |DNL|<0.5

10bit ADC



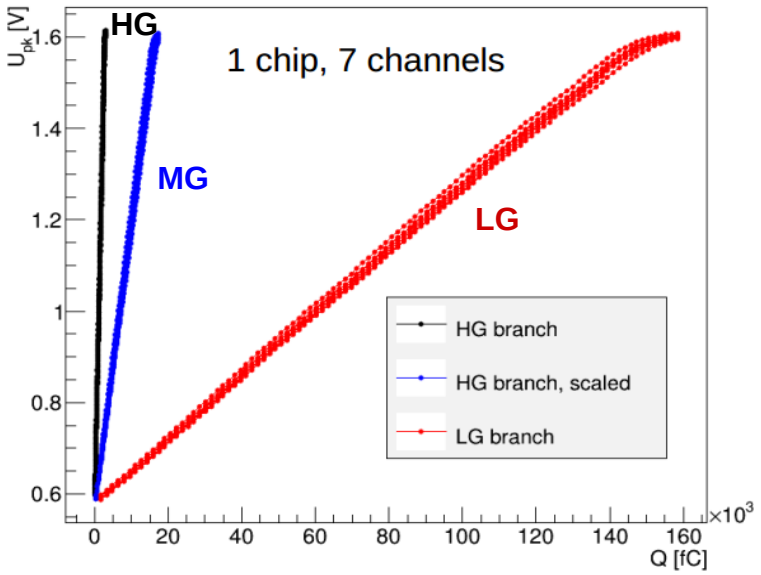
ADC in 12bit mode



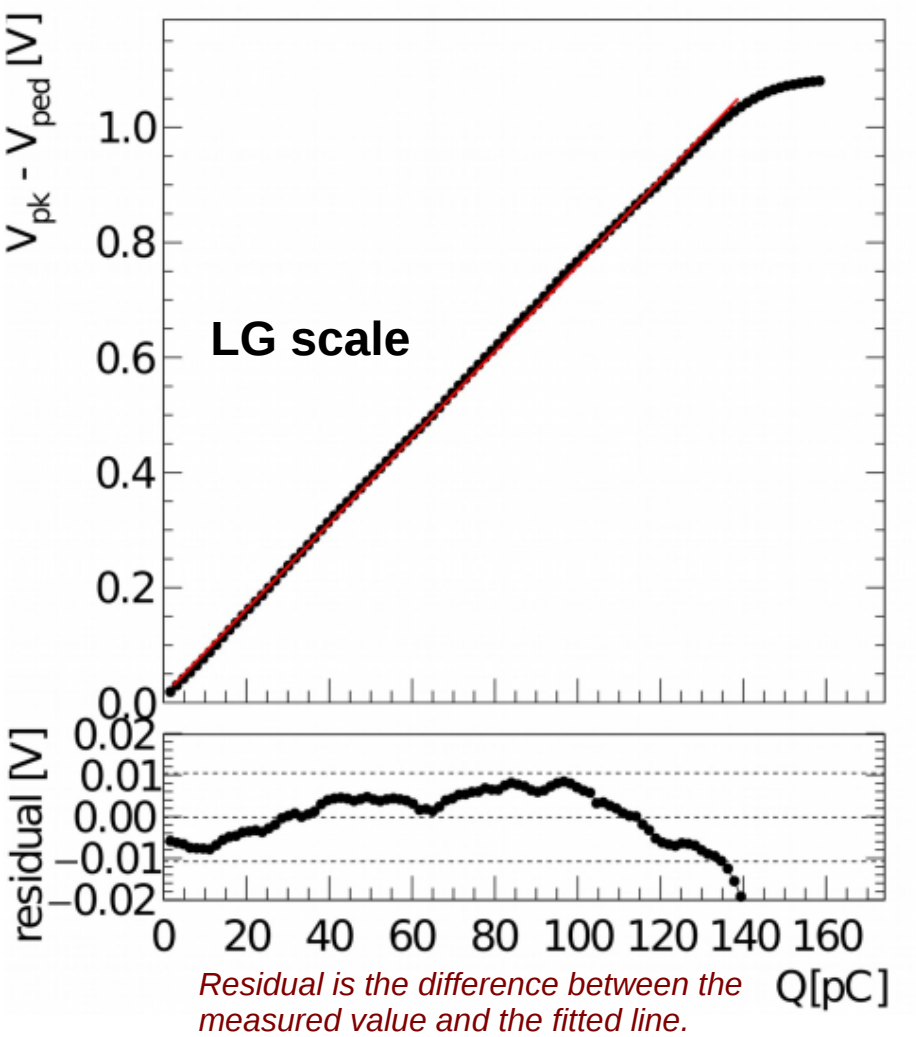
Front-end characterization

Charge injection pulse pass trough 33pF capacitor and is connected to the FE. The FE output is measured with scope.

- **3 possible gain scale setting**
  - HG branch → 1:1(HG) or 1:7(MG) exclusive
  - LG branch → 1:48
- **Dynamic range** (1% Full Scale Range):
  - High Gain scale → 2.7pC
  - Middle Gain scale → 16pC
  - Low Gain scale → 136pC

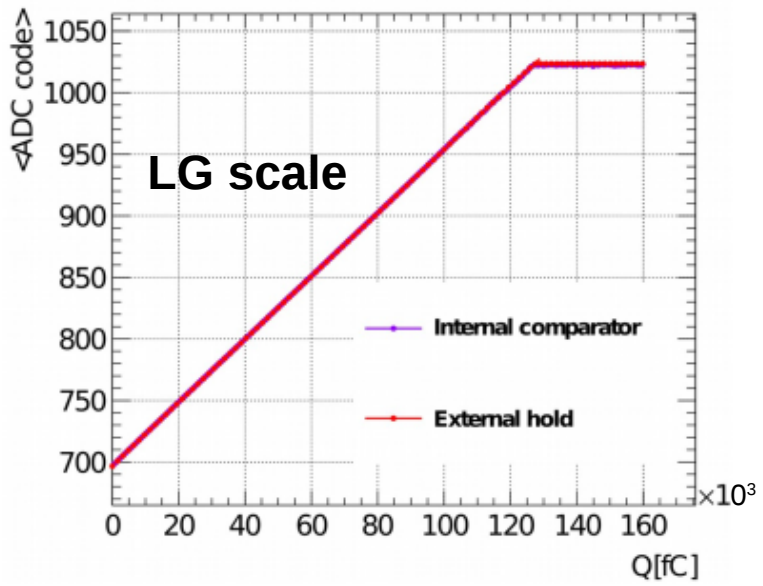


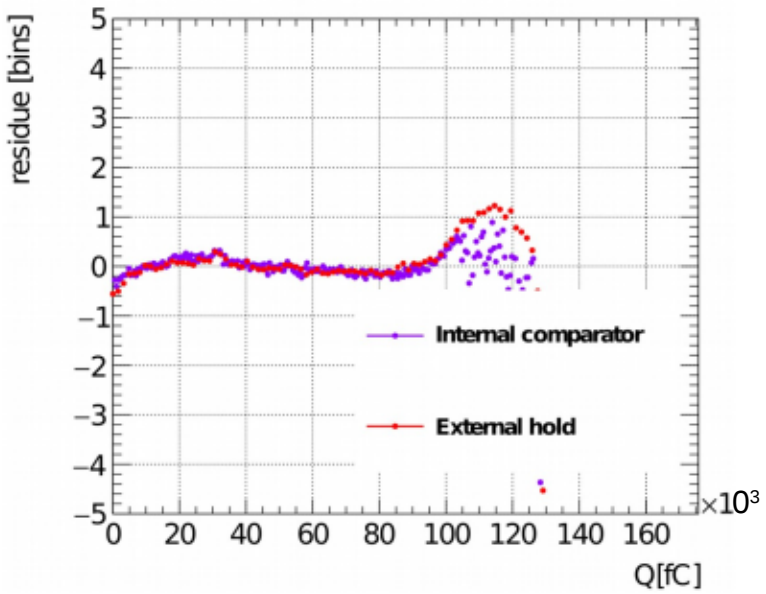
Voltage amplitude as a function of input charge



Residual is the difference between the measured value and the fitted line.

Full chain characterization





Charge injection pulse through 33pF capacitor.

- **Full chain measurement with 10-bit ADC**
- Measurements with **two type of hold**
  - Internal generated hold *(time walk)*
  - External generated hold

No time walk effect observed

- **Dynamic range**
  - HG scale → 2.3pC *(vs 2.7pC only FE)*
  - LG scale → 130pC *(vs 136pC only FE)*

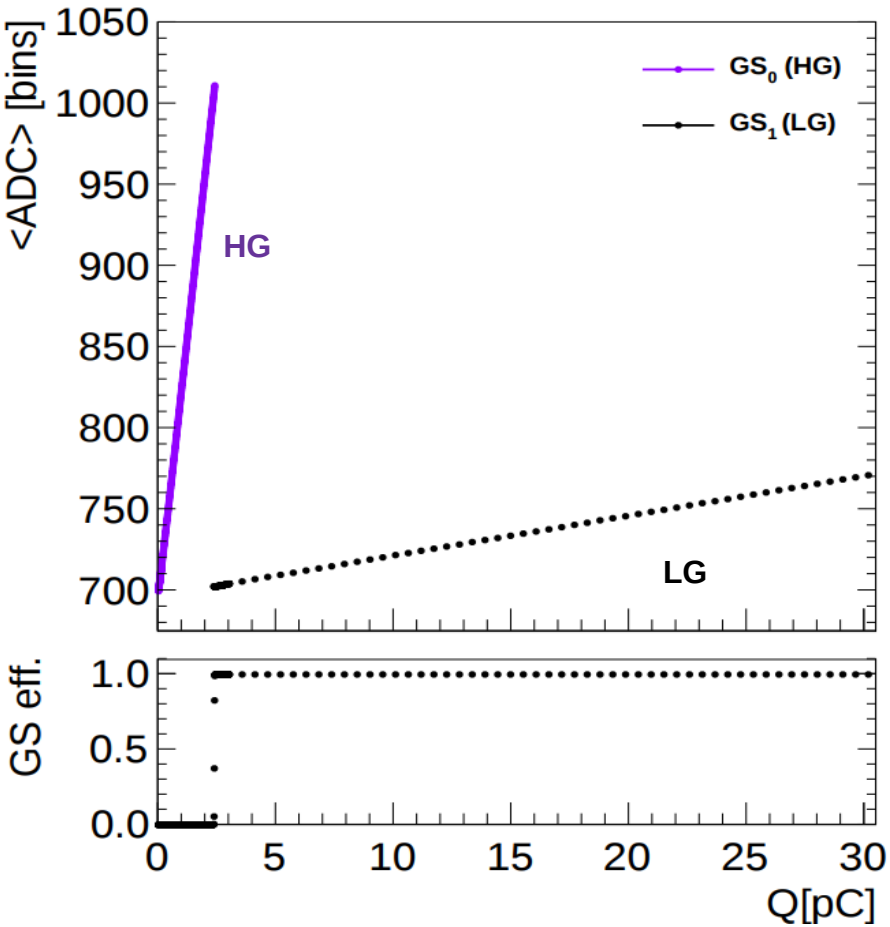
Dynamic range smaller than that of FE due to ADC limited dynamic range (1.6V)

- 1% Full Scale Range

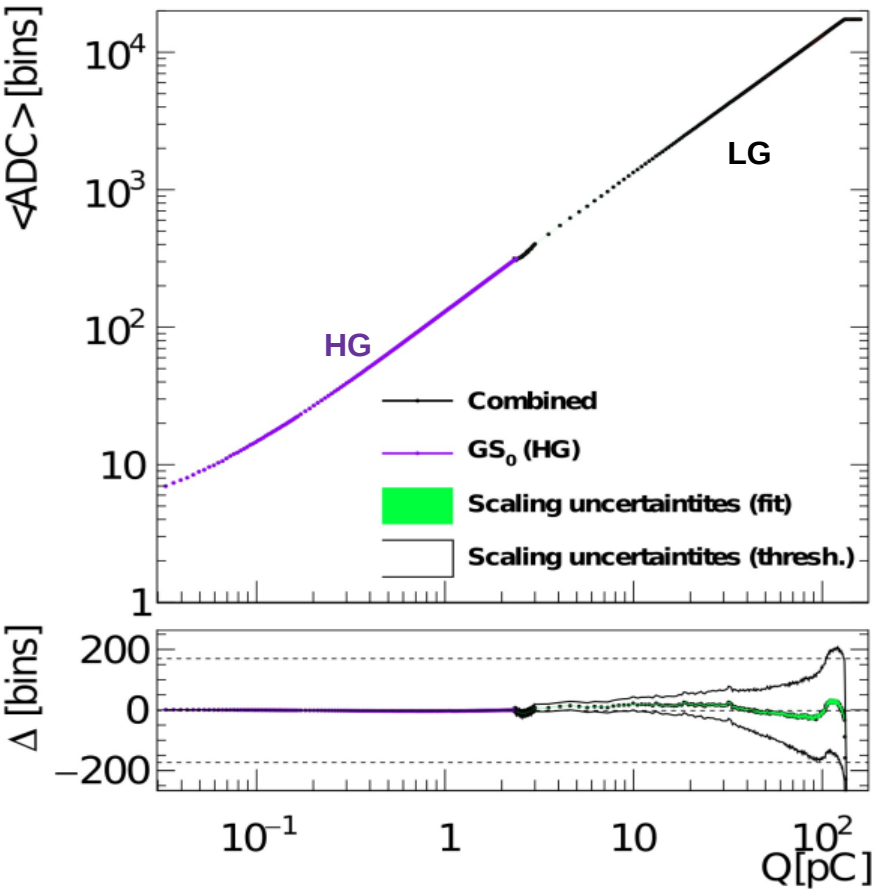
(The residue is the difference between the fitted data and the measured result)

Full chain: Auto-gain selection

Full chain linearity measurement using 10-bit ADC in auto-gain working mode



Combination of the LG and the HG plots



- **The auto gain selection works well**
- **Linearity is satisfactory**, for charge smaller than 130pC
- The **deviations < 1% (FSR)**

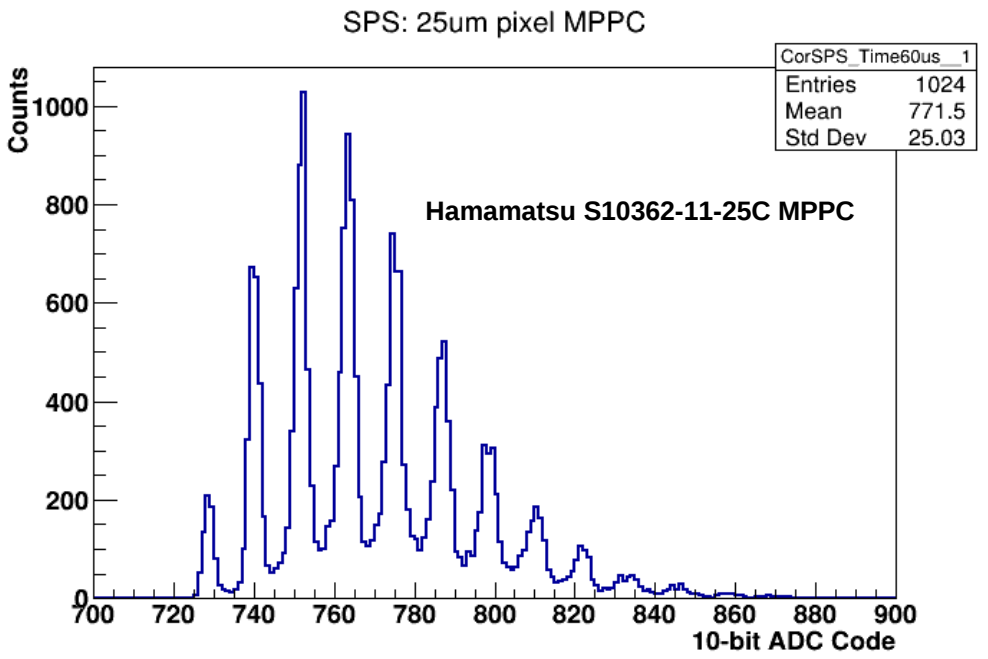
Measurements of the SPS

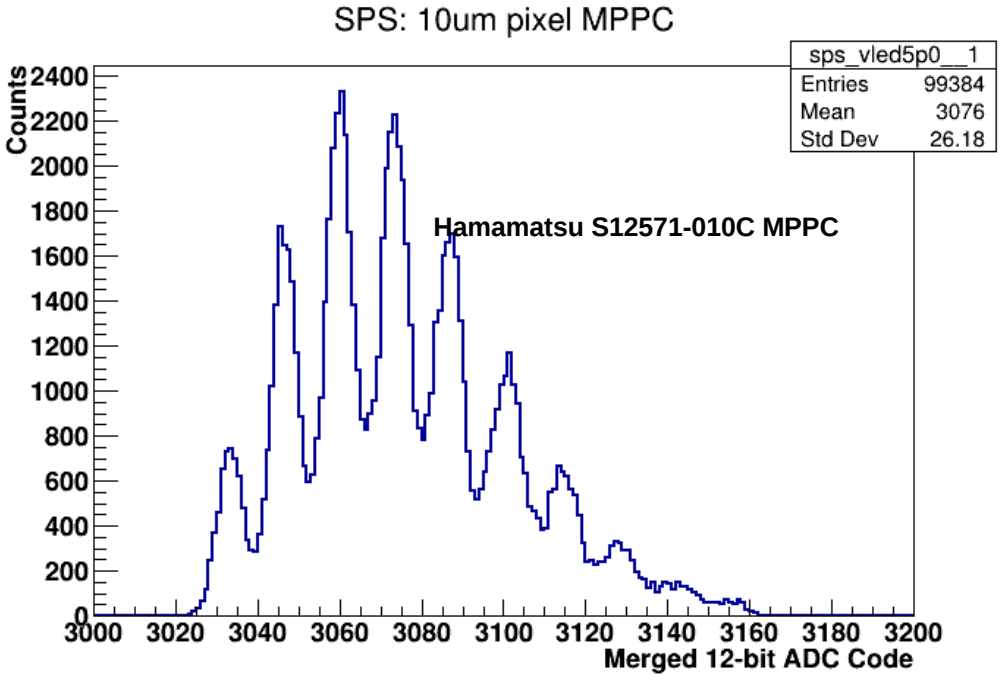
Single Photon Spectra (SPS): SiPM with different pixel sizes.
Sensor illuminated by a pulsed LED

- **SPS with 25µm MPPC**
  - Spectra recorded in self-triggered mode
  - Large gain: 10b ADC sufficient
  - ADC DNL correction performed

- **SPS with 10 µm MPPC**
  - External triggered mode
  - Small gain: 12b ADC used
  - SiPM operated at nominal bias voltage

Gain = 1.35e5 (data-sheet)





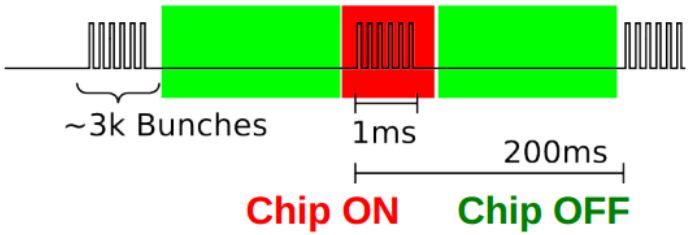
- For both cases a nice spectrum is obtained with clear peak separation.

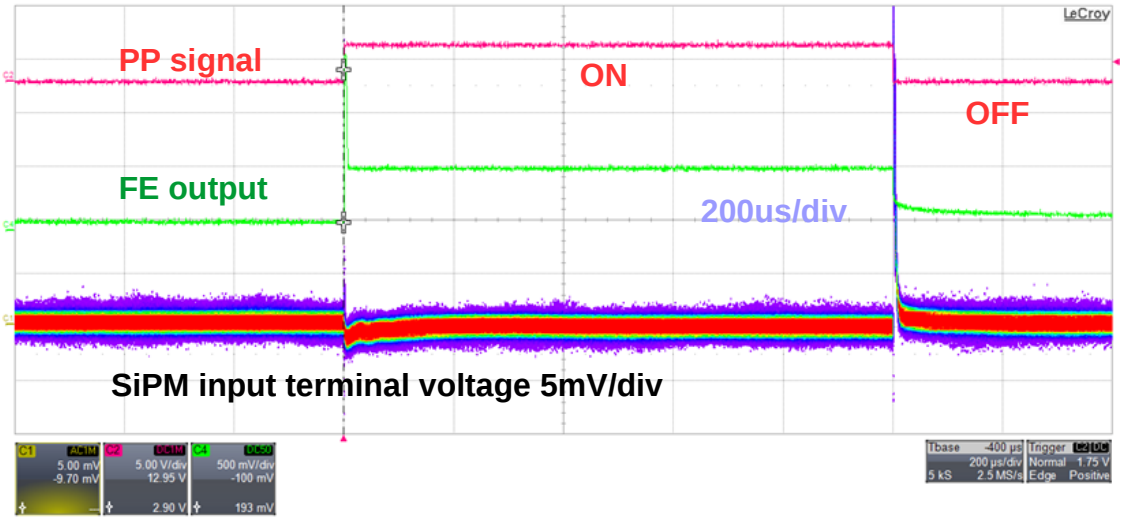
Power-pulsing features

Power pulsing scheme:

- Turn off ASIC when no events
- 25uW/Ch(>= 0.5%)

Beam structure





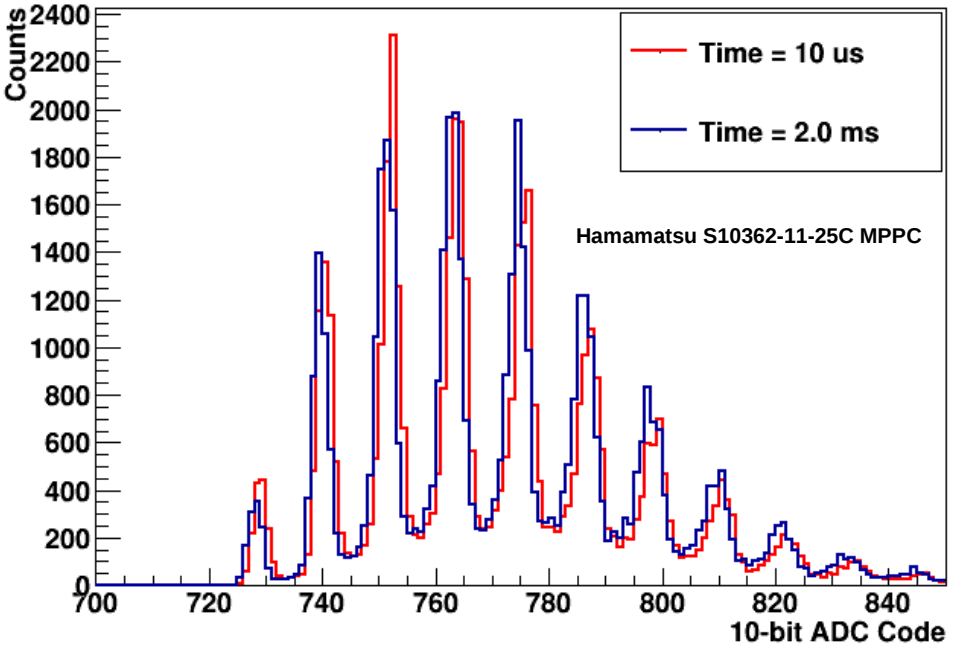
Key points:

- Stable bias voltage at the input
- Fast front-end setup < 10us

SPS at different illumination time respect to the ASIC ON time

- Almost no observable displacement

KLauS4 can work well with 10 µs after turn on during power pulsing



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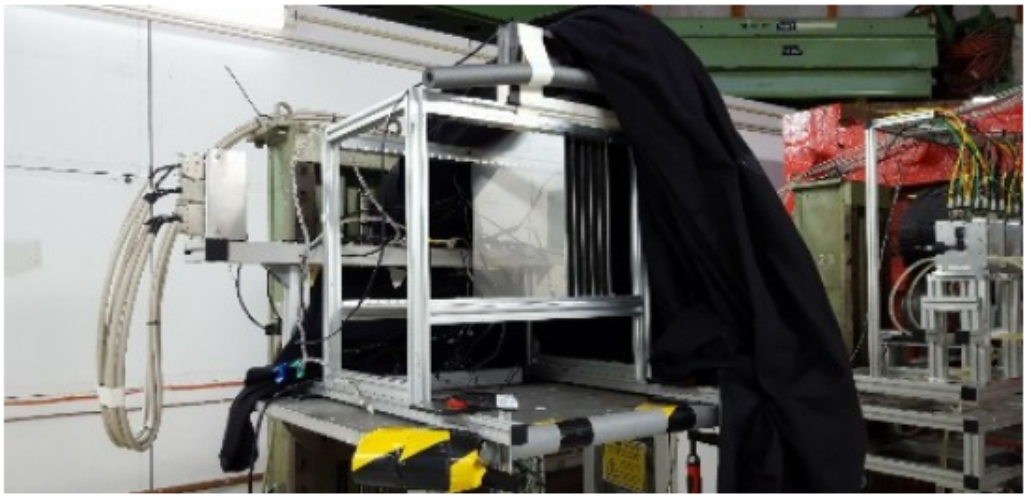
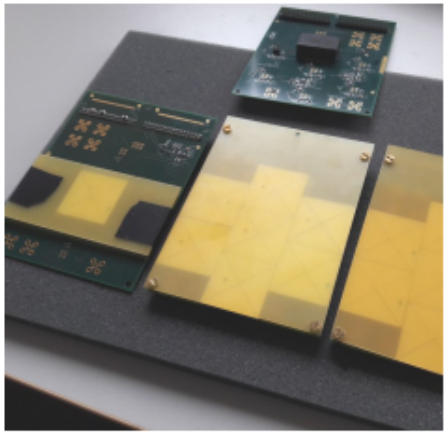
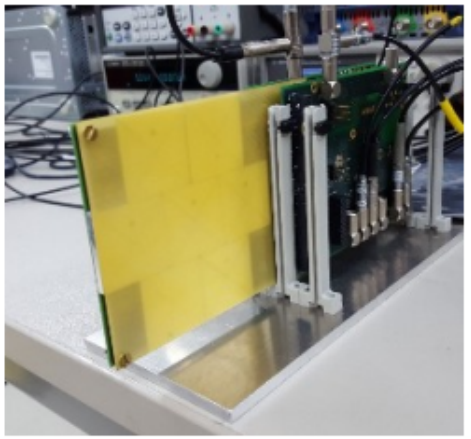
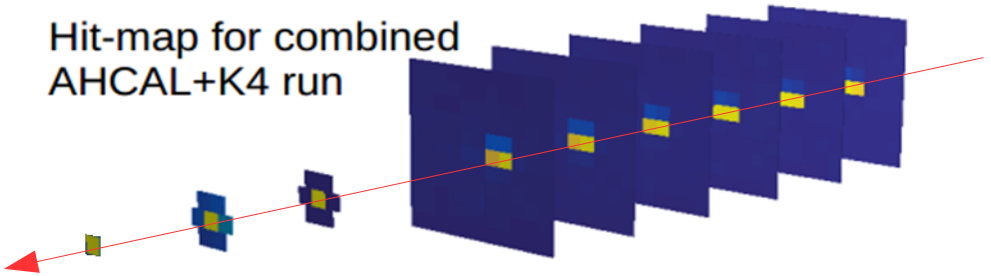
KLauS4 in DESY test-beam



- One week of beam in February
  - Parasitic to AHCAL DAQ tests
- 3 ASICs used
  - 1 board: single tile + SiPM in center
  - 2 boards: fully equipped (7 channels)



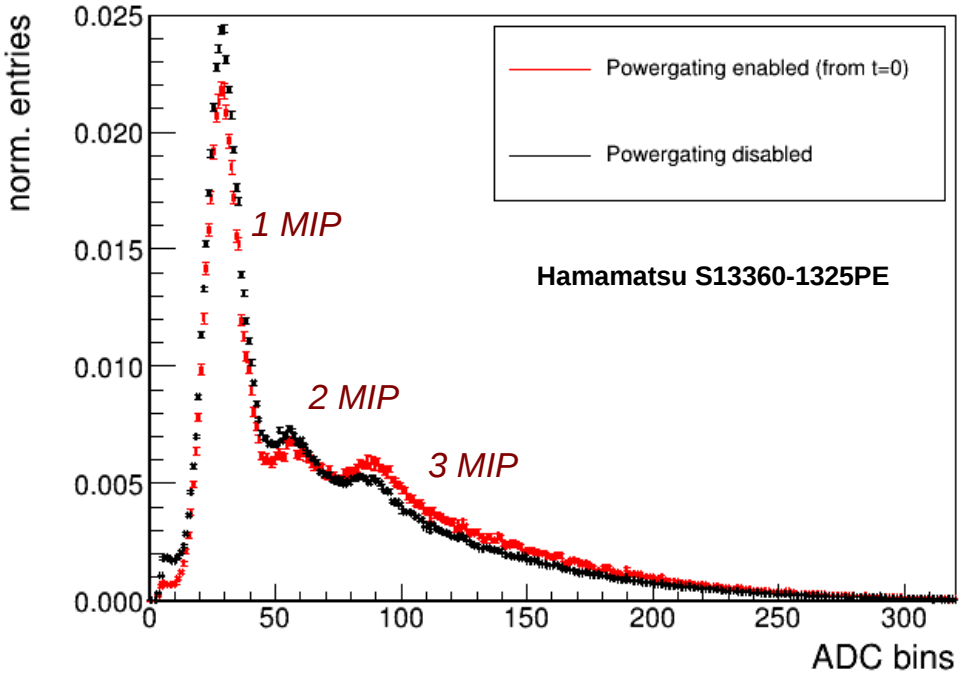




3 layers with KLauS4 6 AHCAL layers

Validation in test-beam

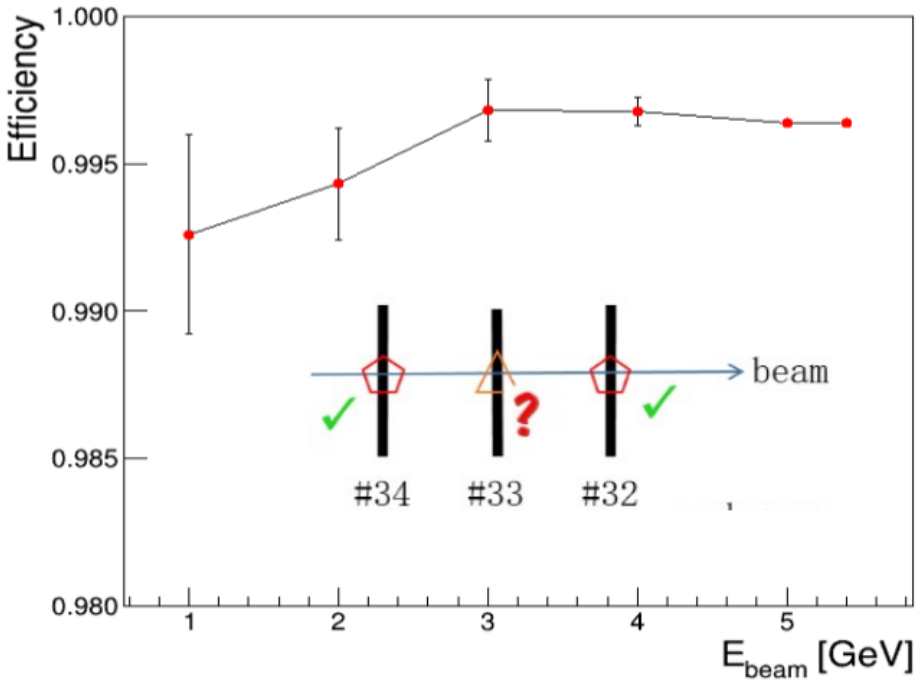
- **MIP spectra:** with/without power-pulsing



- The position of the MIP peaks is preserved
- The ASIC performe the same with and without power-pulsing

- **MIP efficiency:**

  Require coincidence in outer layer
  Check for hit in center layer



- The efficiency is > 99% for all the beam energy tested

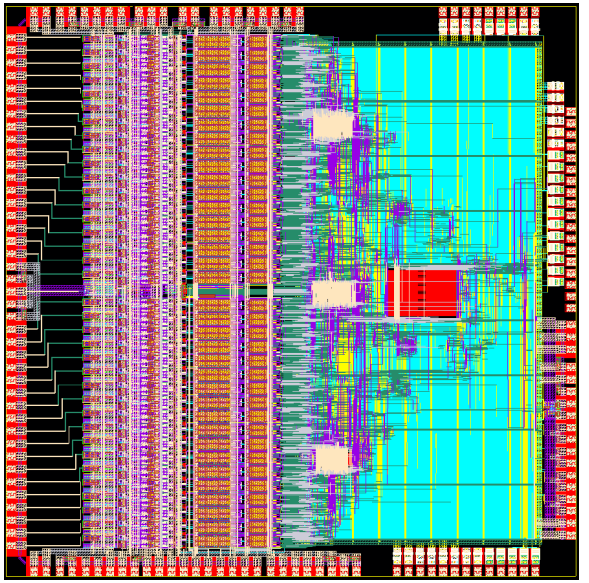
Summary

Current KLauS4 prototype

- ✔ Front-end and ADC working well
- ✔ Fulfill the design requirements
- ✔ Successful measured of SPS for SiPM down to 10um pixel size
- ✔ Validated the chip performance in the test beam at DESY

Next steps

- ➔ Plan to include the new chip in the future AHCAL prototype…
- ✔ **36 channels prototype submitted in July 2017**



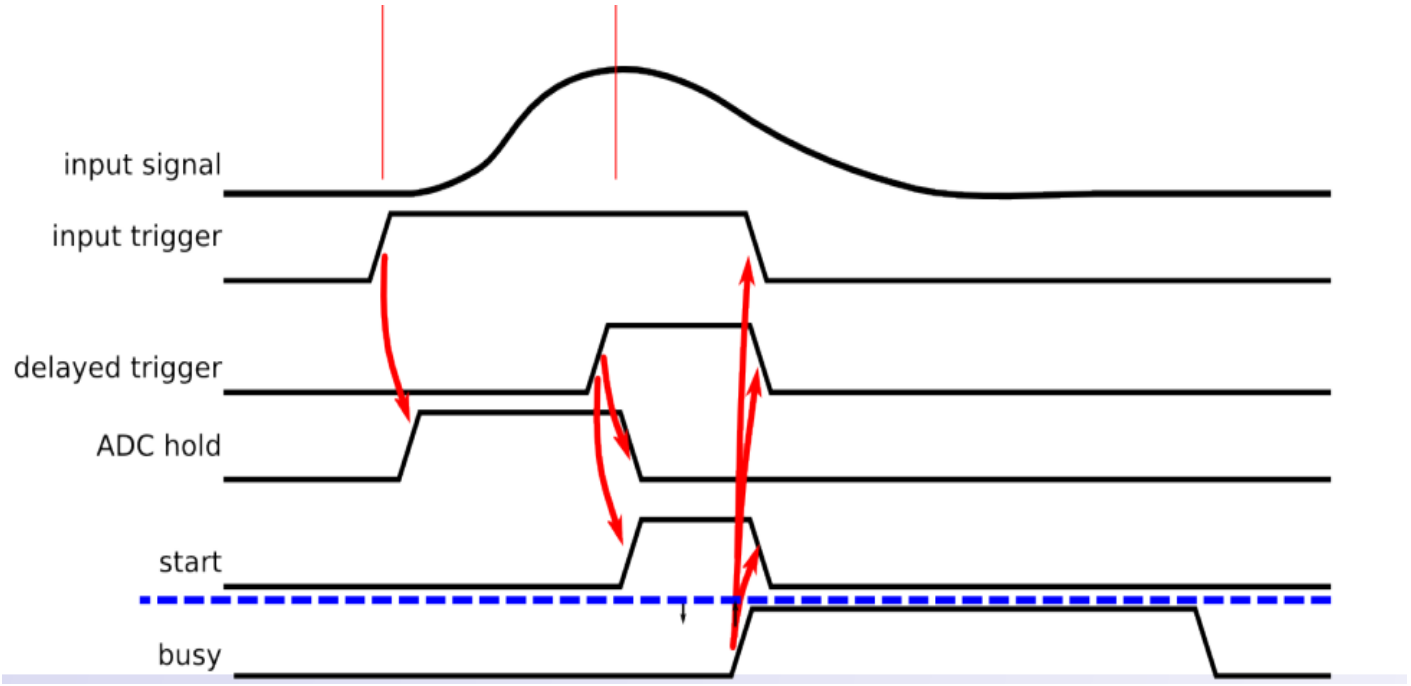
Thanks for your attention!

How the ADC digitize the Peak

The time comparator gives a trigger(input trigger) at the arrival of signal.

The Hit Logic delays the trigger signal (hold delay, configurable)

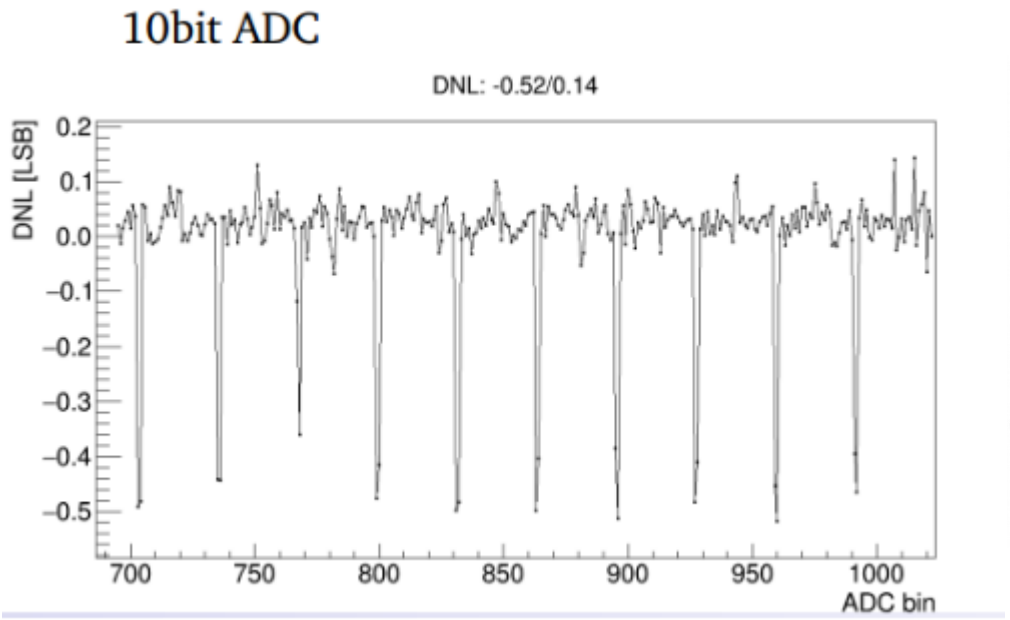
At the rising edge of delayed trigger, the ADC samples the input signal and start a conversion.

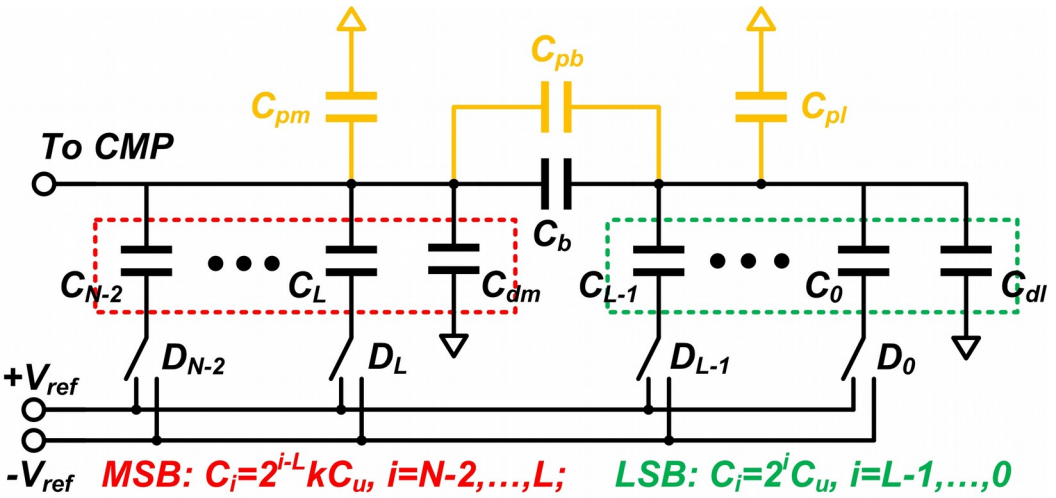


ADC DNL

Large Cpm → dynamic range shrink

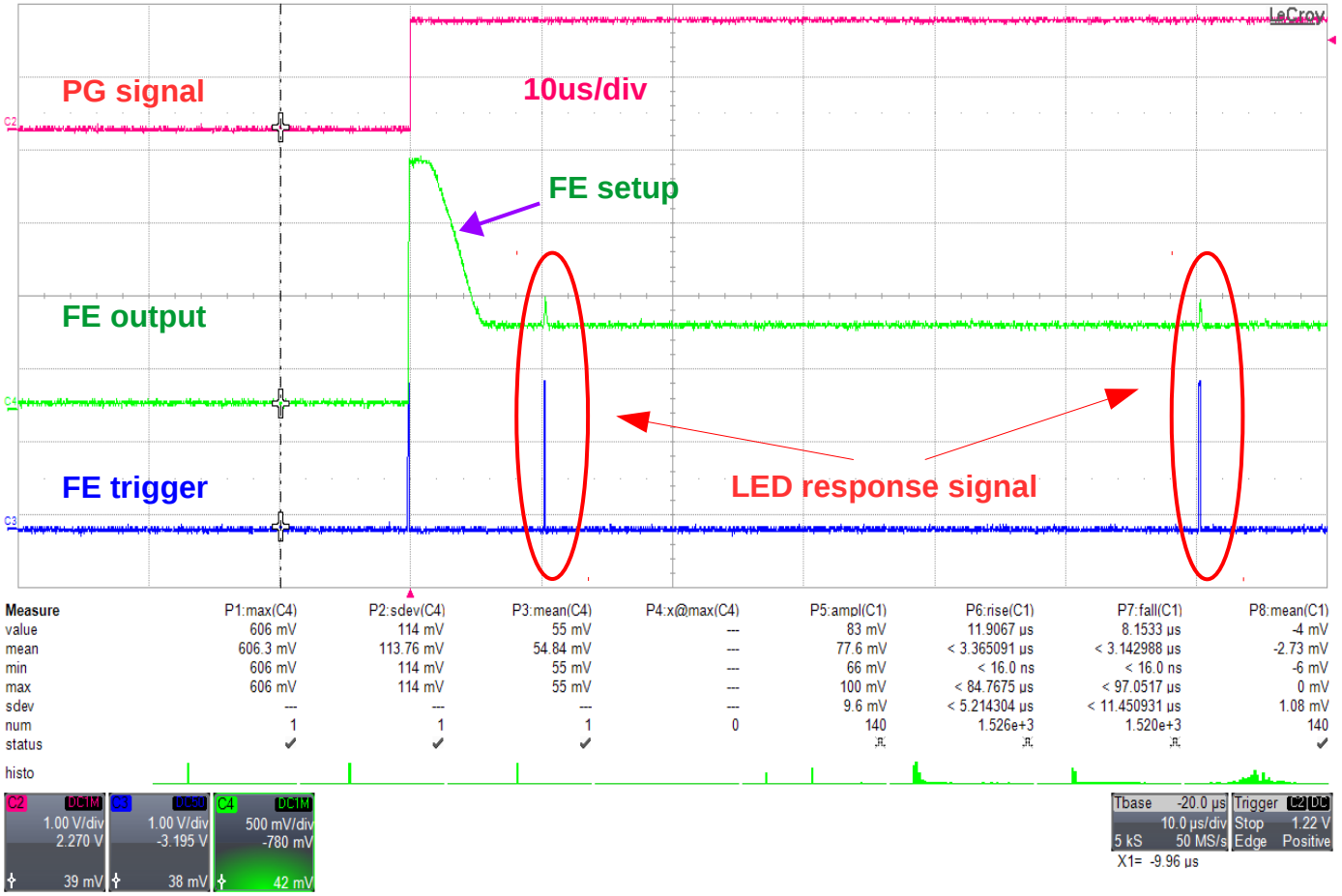
Large Cpb → DNL negative spikes





Front-end setup

Front-end can be setup less than 10 us during power-pulsing



Full chain : noise performance

- *Measurement : The Root-Mean-Square of the pedestal voltage for different capacitance connected to the input terminal.*
- *Fixed charge input*
- *For capacitance < 100pF, the equivalent noise charge (ENC) < than 6fC*
- *Code spans from 3~5 ADC codes*
- *Stddev is around 0.6~0.8 bins (LSB=3.2mV)*
- *The front-end noise is the dominant*