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KlauS4: A Multi-Channel Silicon-Photomultiplier Charge Readout ASIC in 0.18 µm UMC CMOS

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KLauS4 is a 7-channel mixed-mode Silicon-Photomultiplier readout ASIC for imaging calorimetry at a possible future linear collider, where one key aspect is the low-power consumption of the readout ASICs. Each channel consists of a low-noise front-end with two gain branches to deal with a large input signal range, and a 10-bit power efficient SAR ADC to digitize the charge information; a common digital part for data storage and transmission is also implemented into this chip. For each channel, an additional pipelined stage is used to increase the quantization resolution to 12-bit when necessary. Detailed design of the ASIC, results on characterization measurements and first test-beam results will be presented.

Summary

A high granular imaging calorimeter system with a large number of channels is planned to be operated at future linear collider experiments. For such a system the analog hadron calorimeter (AHCAL) of the CALICE collaboration is being developed; its concept is based on organic scintillator tiles read out by silicon-photomultipliers connected to highly integrated readout electronics. Due to the high integration and the dense environment, the used readout ASICs are required to dissipate not more than 25 µW per channel when being power pulsed with >0.5% duty cycle.

The analog front-end is designed to achieve sufficient SNR for a single pixel signal using low-gain SiPMs, while allowing charge measurements for the full sensor dynamic range. A current conveyor structure is used for the input stage to lower the input impedance. Two branches for charge integration with different gains are implemented: A high-gain branch for single pixel signals mainly required for calibration and a low-gain branch spanning the large charge range. An automatic gain-selection is implemented to determine which gain branch is digitized. In addition a comparator is implemented to generate a digital trigger signal for time stamping with sub-nanosecond resolution; the trigger is also used to initiate the ADC conversion.

The amplitude of the output signal from the front-end is digitized by an ADC to get the charge information. A 10-bit Successive-Approximation-Register ADC is adapted to minimize the power consumption. To measure the single pixel signal from SiPMs with the intrinsic gain as low as 105„ an addition pipelined SAR stage is implemented to increase the quantization resolution to 12-bit.

The design of the front-end and the ADC were already presented in TWEPP14 and TWEPP15. The current version, KLauS4, combines both parts into a single channel. In the new chip, 7 channels as well as the digital part for data transmission and configuration are implemented.

The performance of the chip has been characterized in detail under laboratory conditions. The equivalent noise charge for the high-gain stage is measured to be as low as 5 fC for a total input capacitance less than 100 pF. The low-gain branch can achieve 1% INL/FSR linearity up to 150 pC. For the 10-bit ADC, the DNL is measured to be -0.52/+0.14 LSB; for the ADC in 12-bit mode, the obtained DNL is -0.44/+0.36 LSB. Single-photo-spectra (SPS) for 10 µm pitch SiPMs have been obtained showing a clear separation of the photo-peaks. In power-pulsed operation, less than 10 µs is needed for the front-end to settle. The performance results for the chips with and without power-pulsing are compared with good agreement.

Test measurements have also been carried out at the DESY test-beam facility using a three-layer setup comprised of scintillator tiles, 25 µm SiPMs and KLauS4 ASICs. The multi-channel operation could be verified recording MIP spectra in all of the 15 equipped channels. Various analog and digital functionalities were tested successfully, such as the auto-gain selection and power-gating, which show good agreement with the pre-selected and non-gated spectra, respectively.

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