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Laboratory and Beam Test Results of TOFFEE ASIC and Ultra Fast Silicon Detectors

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We report on the measurements performed on the full custom ASIC TOFFEE designed to read out Ultra Fast Silicon Detectors (UFSD). The ASIC has been tested in laboratory with custom test boards and an infrared laser hitting the sensor and emulating a minimum ionizing particle signal.

Laser measurements showed that a time resolution of less than 50 ps is achievable with a 10 fC signal.

We will also present the beam test results for the TOFFEE and UFSD system which will be held in May at CERN.

Summary

In the High Luminosity LHC environment, the overlap of hundreds of events raises the need to distinguish events separated by a few tens of picoseconds.

In order to reach a precise time information it is required to have concurrently large and uniform signals from the detector and a fast readout electronics, as well as to minimize the noise.

To fulfill this requirement, the Ultra Fast Silicon Detectors (UFSD) are being developed and have an intrinsic resolution of about 20 ps, obtained at a beam test with pions in 2016. These sensors feature internal charge multiplication,

electrode segmentation and provide a signal between 8 and 10 fC for a minimum ionizing particle. The moderate charge multiplication allows to have a fast and steep signal while keeping the avalanche noise low.

The TOFFEE ASIC, a 8-channel amplifier comparator chip, has been specifically designed in UMC 110 nm CMOS technology to read out the UFSD: the input stage has been optimized for the shape and charge of the sensor signal.

The ASIC has been developed in UMC 110 nm CMOS technology and is aimed to fulfill the CMS-TOTEM Precision Proton Spectrometer (CT-PPS) time resolution requirements (~ 30 ps per detector plane). It features LVDS outputs and the signal dynamic range matches the requirements of the High Precision TDC (HPTDC) system.

The chip has been received from foundry in September 2016 and tests started in October with custom boards. Since February 2017, it has been possible to test the performances of TOFFEE coupled with UFSD sensors. The test board houses a 32-channel UFSD sensor wire-bonded to the ASIC and allows to read out 8 channels at the same time.

The laboratory setup involves the use of an infrared laser to emulate the charge deposition of a minimum ionizing particle in the sensor. The charge produced by the laser has been calibrated by means of a pin diode without charge multiplication.

A time resolution of less than 50 ps has been achieved with a 10 fC signal, dropping under 40 ps for higher charge values. These values include the jitter contribution of the laser and show good agreement with simulations.

A beam test is scheduled for May 2017 at CERN (SPS H8 beam line). In this beam test the data acquisition chain will be very close to the one foreseen at CT-PPS: an array of three TOFFEE + UFSD boards will be proofed with 180 GeV pions, while the output will be read out with the HPTDC.

This test campaign will be an important prediction of the actual performance of the system before its installation in the experiment, foreseen for the last quarter of 2017.

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