Test Vehicles for CMS HGCAL Readout ASIC

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On behalf of CMS collaboration

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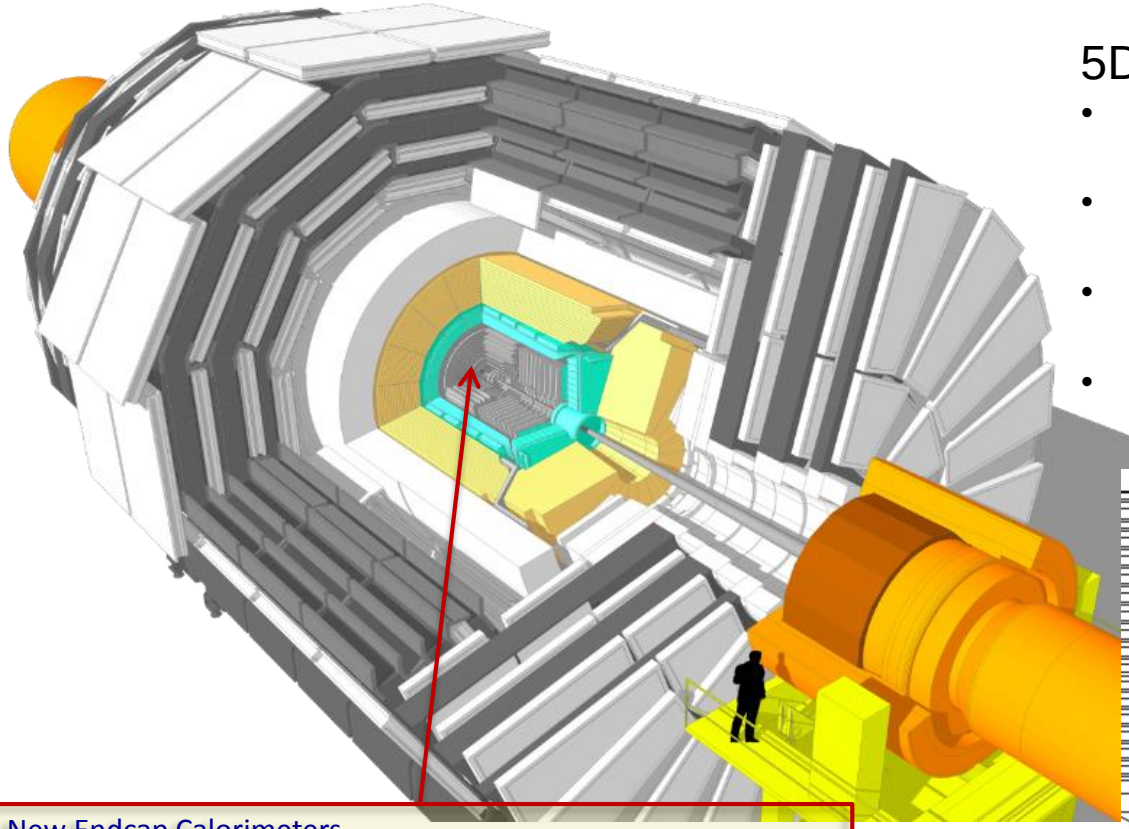
Organization for Micro-Electronics desiGn and Applications

HGCAL: CMS EndCap Calorimeters for the LHC Phase-II upgrade

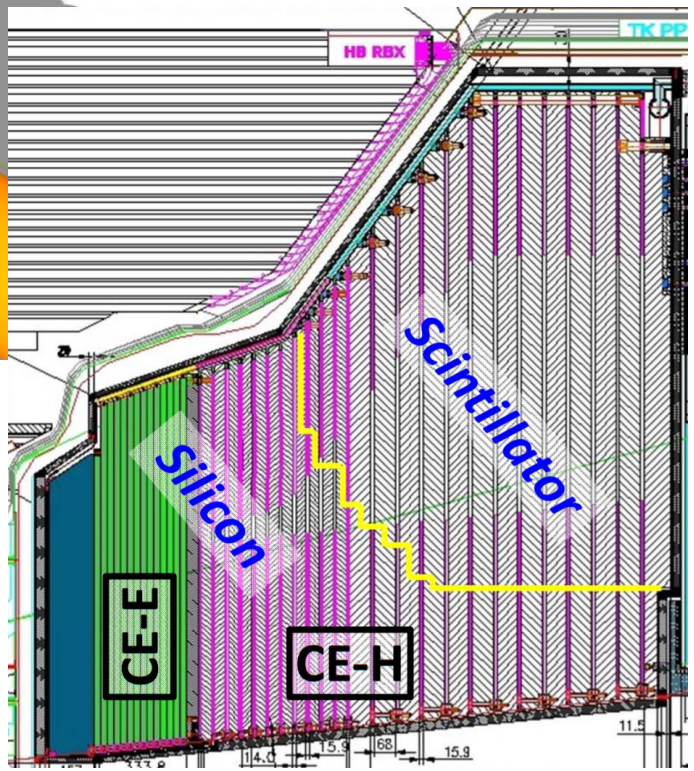


5D calorimetry: x, y, z, E, t

- High granularity ➔ Millions of channels ➔ low power
- Energy measurement: large dynamic range (0,1fC/10pC)
- Timing information: pile-up mitigation, need few tens of ps
- EndCap calorimetry ➔ 200 Mrad, 1E16 N

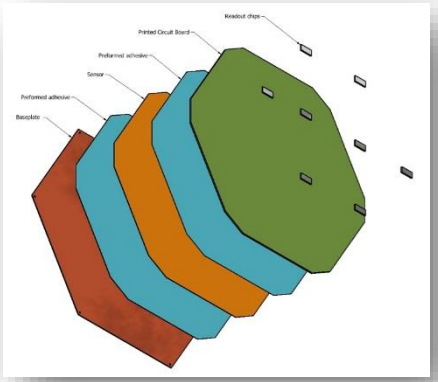
New Endcap Calorimeters

- Rad. tolerant
- High Granularity: increased transverse and longitudinal segmentation, needed to mitigate pileup effects to select events with a hard scatter process at L1-Trigger and to identify the associated vertex and particles
- precise timing capability: further mitigation of pileup effects

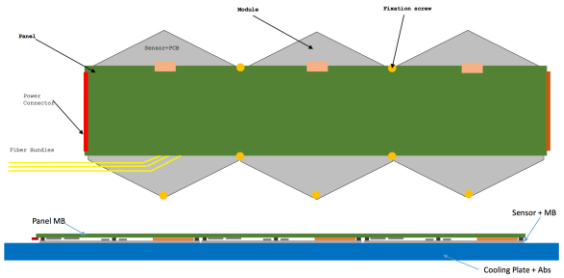


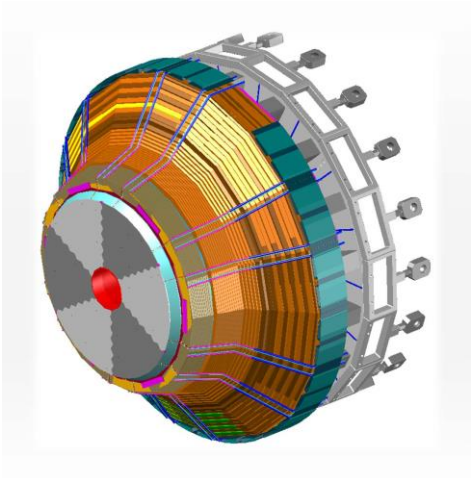
Modules, Cassettes and Mechanics

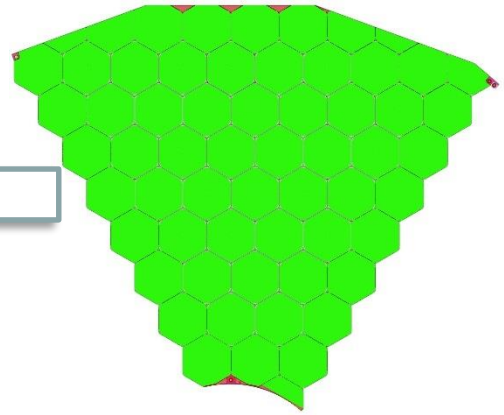
Modules (22k)
Glued stack of W/Cu baseplate, kapton, Hexagonal 8” Si sensor, PCB



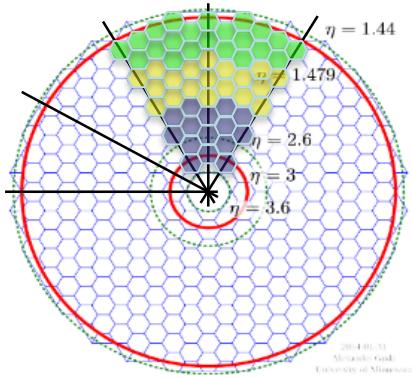
Motherboard Panel with concentrator ASIC and optical transmitters to readout data and trigger data of 6M channels







Cassette
(1,5 < η < 3,0)

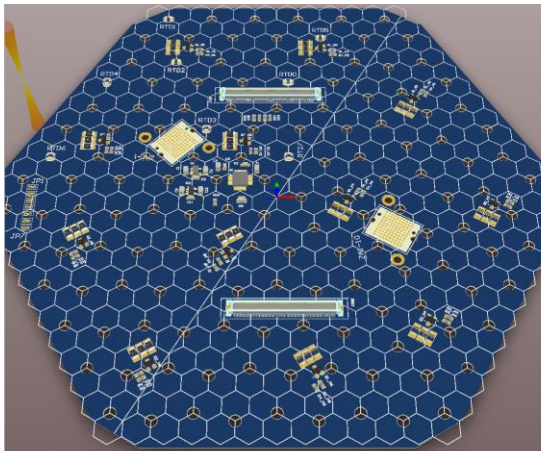


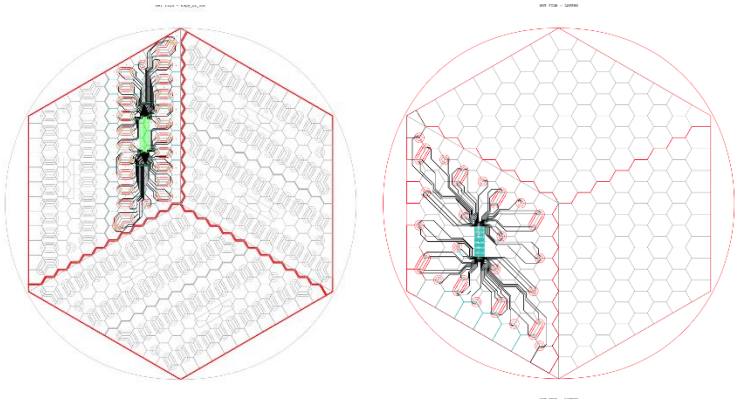
12 **Cassettes** mounted together to form the **ECAL (EE)** **and** **Front HCal (FH)**

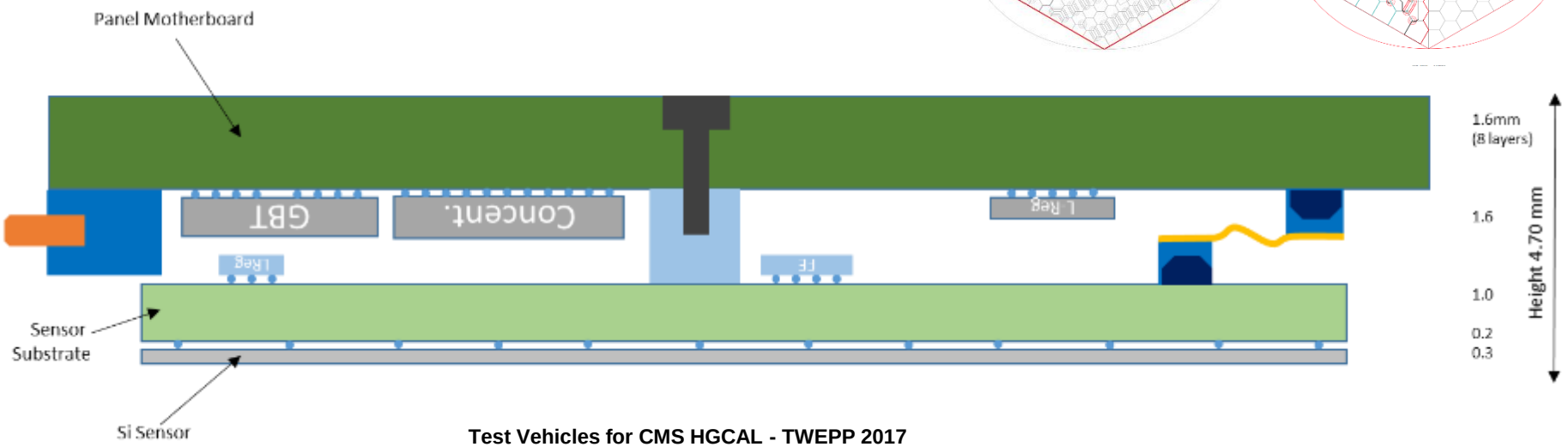
3 sensor active thicknesses 120-200-300 µm
0.5 (1) cm^2 pads for 100(200/300) µm

Challenges for electronics

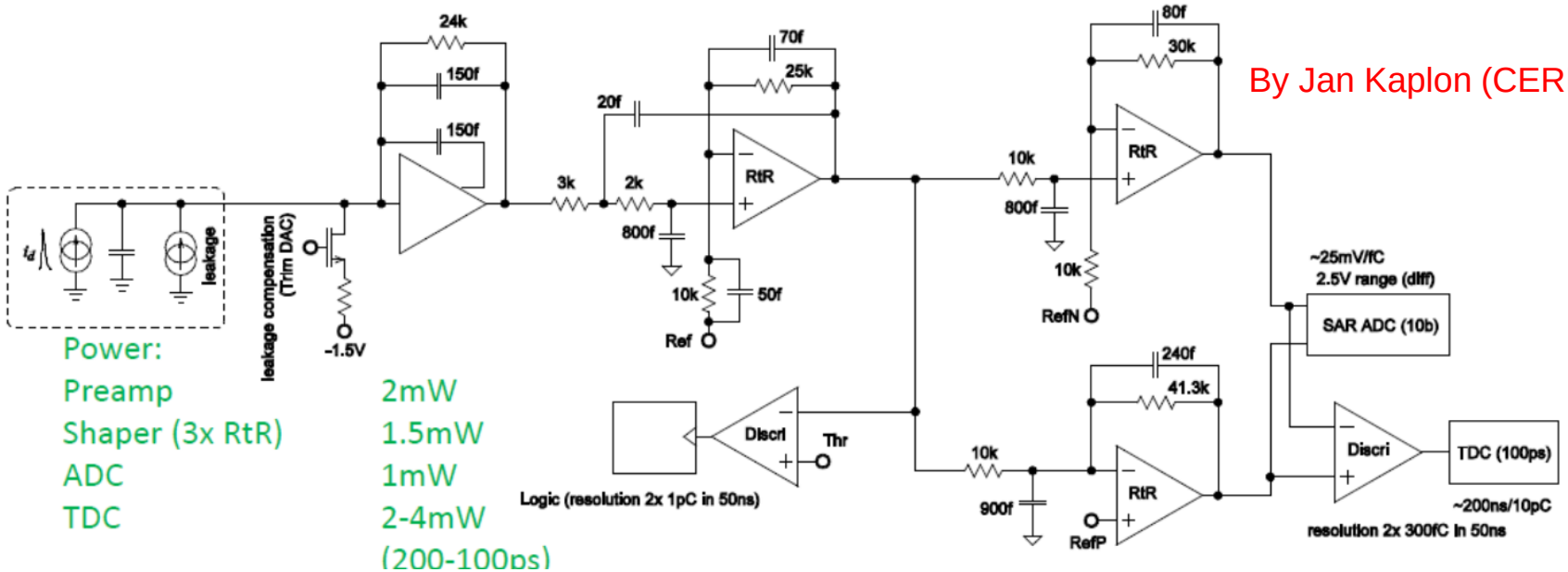
- Stringent requirements for Front-End Electronics
  - Low power (~10mW for analogue channel, ~5mW for digital)
  - low noise (< 2000 e-), MIP ~ 1-4 fC
  - Detector capacitance 40 – 60 pF, 10µA max. leakage
  - High dynamic range: up to 3000 MIP (10pC), 17 bits required with 0,1 fC resolution
  - Time measurement: 20 ps resolution, PU mitigation
  - High radiation (200 Mrad, 10^E16 N)
  - System on chip (charge, time, digitization, data and trigger processing, on-chip zero-supress…)
  - High speed readout (1,28 Gb/s)
  - ~ 1^E5 FE chips





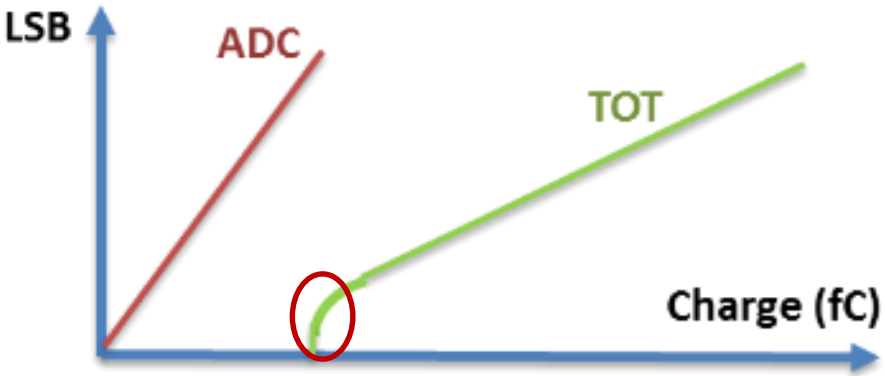


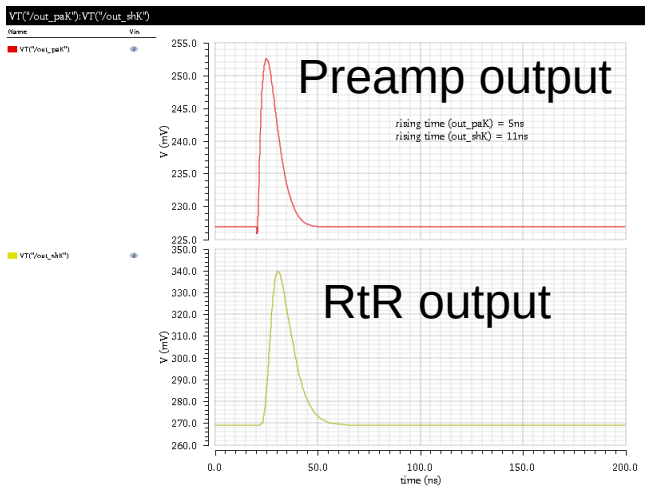
Baseline architecture (Technical Proposal)



By Jan Kaplon (CERN)

- Preamplifier and shaper DC coupled to detector, no reset, fast shaping (15ns peaking time)
- Analog gain around 25mV/fC (quantization noise negligible)
- Preamplifier linear range 100 fC => ADC conversion
- Above 80fC and after preamp saturation => ToT conversion

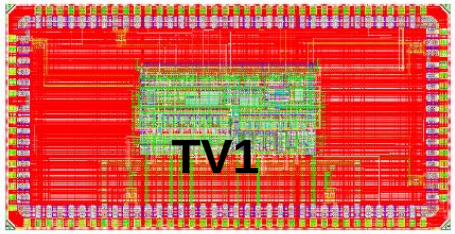


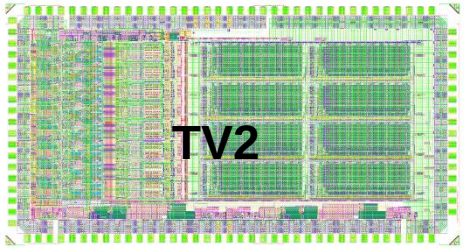


4 ASICs submitted in the past two years

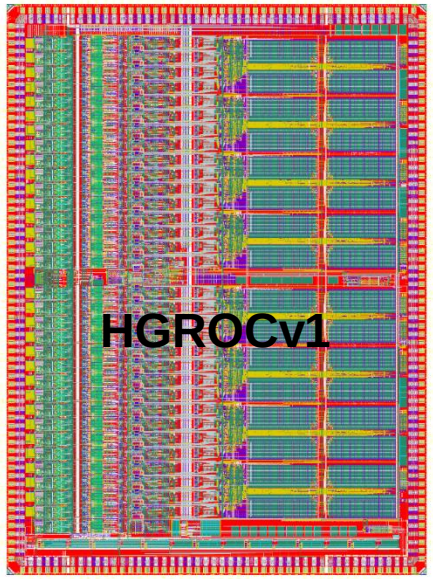
- **SKIROC2_CMS**
  - SiGe 350 nm
  - Submitted in January 2016
  - Dedicated to test beam

- 1st test vehicle: **TV1**
  - CMOS 130 nm
  - Submitted in May 2016, received in august 2016
  - Dedicated to preamplifier studies



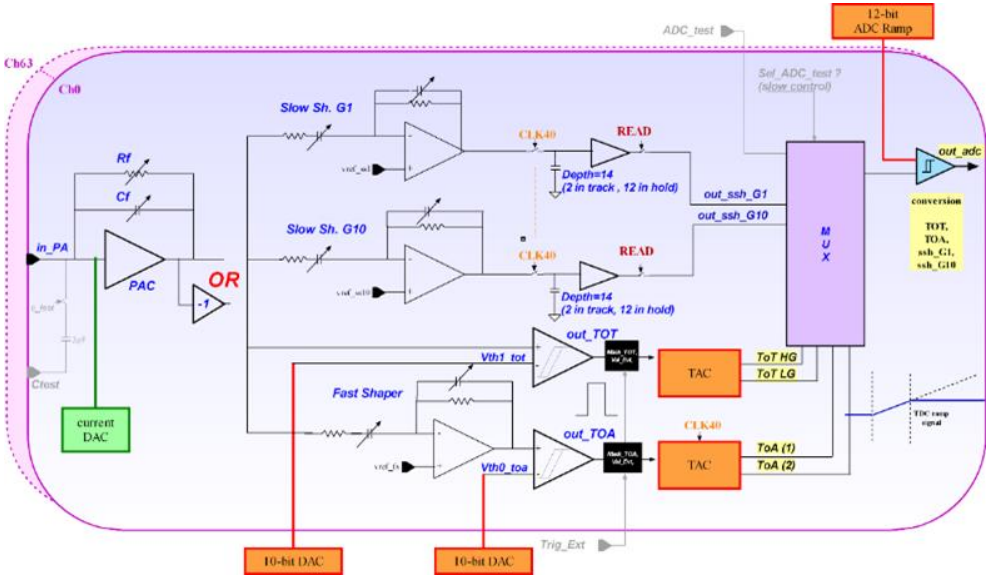


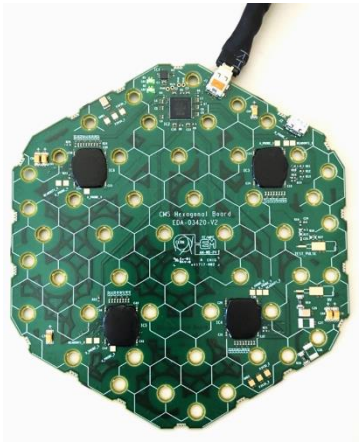
- 2nd test vehicle: **TV2**
  - CMOS 130 nm
  - Submitted in December 2016, received in may 2017
  - Dedicated to technical proposal' analog channel study
- **HGROCv1**
  - CMOS 130 nm
  - Submitted in July 2017, expected in October 2017
  - all analog and mixed blocks; large part, but not complete, digital blocks



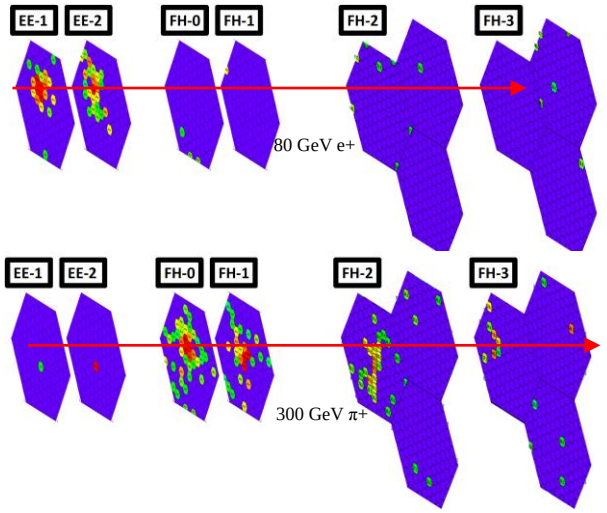
SKIROC2_CMS for HGCAL

- new SKIROC2 for CMS
  - Optimized version for CMS testbeam, pin to pin compatible
  - Dual polarity charge preamplifier
  - Faster shapers (25 ns instead of 200 ns)
  - 40 MHz circular analog memory, depth= 300 ns
  - TDC (TAC) for ToA and ToT , accuracy : ~50 ps
  - Submitted jan 2016, SiGe 350nm
- Test beam :
  - Pedestal stability, MIP calibration
  - HG to LG calibration
  - Showers for e+ and π+





Hexaboard designed at CERN



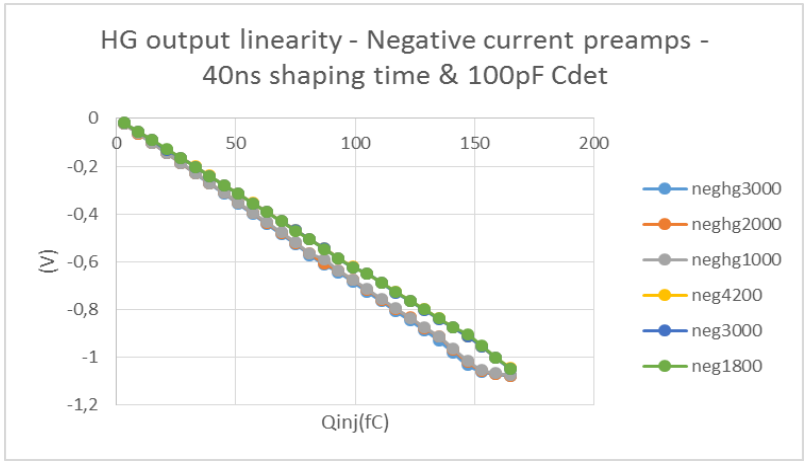
Electron and pions signals seen in testbeam

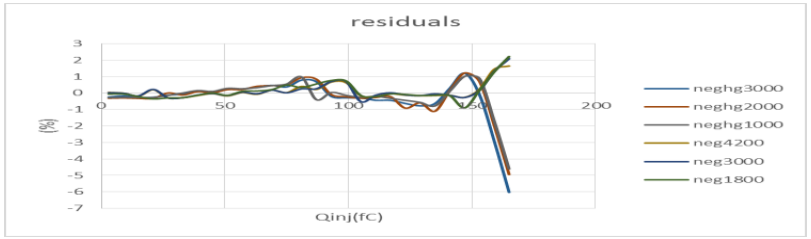
1st test vehicle: TV1

- Analog blocks for preamp characterization:
  - 6 positive & 6 negative input preamps
    - Use different transistor size ant type (lvt, typ, hvt)
    - 60dB and 90 dB OL gain architecture
    - Variable Rf and Cf: charge sensitive or current sensitive
    - CRRC shapers: HG and LG, 5 to 75 ns shaping time, => noise studies
  - 1 baseline channel from TP (CERN schematic)
  - 4 discriminators for TOT studies
  - Digital part for noise coupling tests

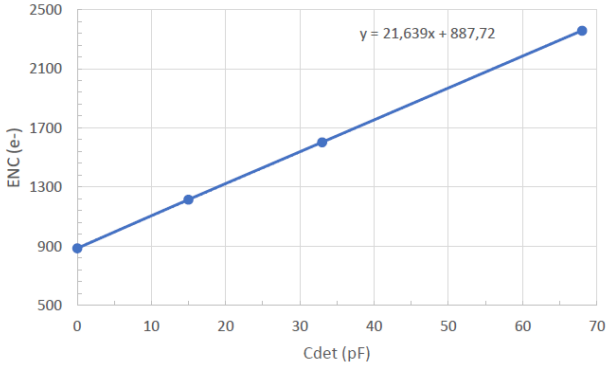
TV1 test results

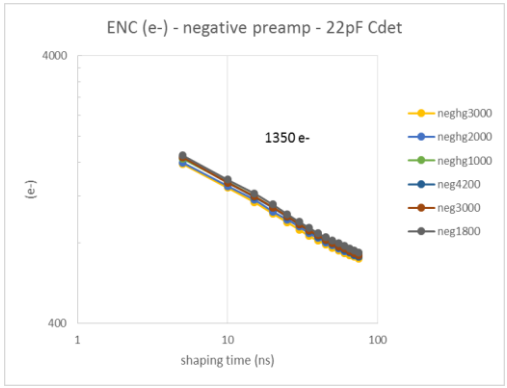
- "90dB" preamps, for both polarities, achieve the best performances in terms of open loop gain, linearity, speed and noise
- Issues found
  - Large parasitic capacitance (Cpa = 40pF)
  - Stability issues with R2R shapers
  - Poor modelization of Crtmom capacitors

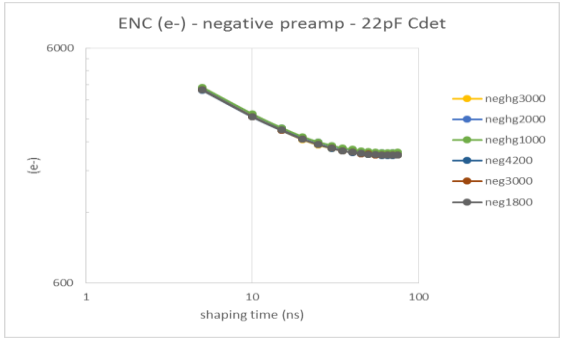




ENC noise vs detector capacitance

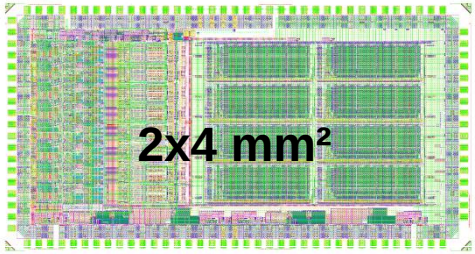


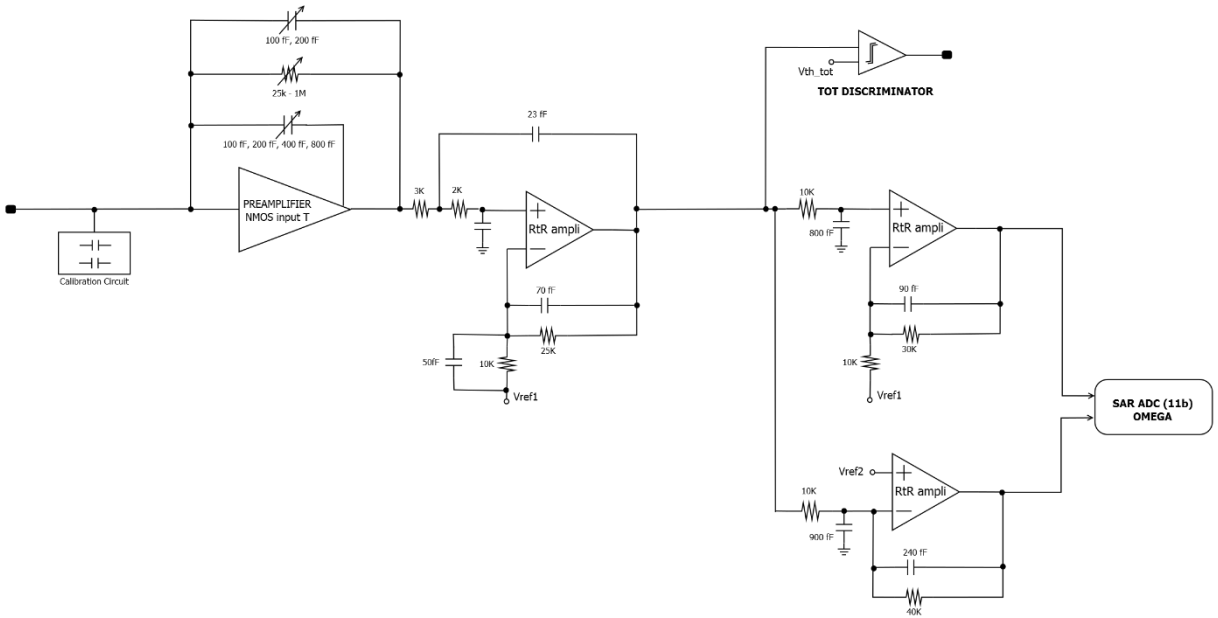




2nd test vehicle: TV2

- Negative input preamp
  - High OL gain (90dB)
  - Variable Cf: 0,1fF – 1,5pF
  - Two selectable Rf: 25K & 1M
  - Cf_comp for high gain setting
  - Different versions: baseline, low parasitics cap (custom layout)
- Baseline shapers
  - Tunable bias
  - Tunable miller comp
  - Global 10b DAC and 5b DAC in order to tune the Reference voltages
- 11b 40 MHz SAR ADC
- ToT: No TDC but discri output on a PAD
- ToA: not implemented (high speed TDC still not available)
- 32x512 SRAM (CERN)



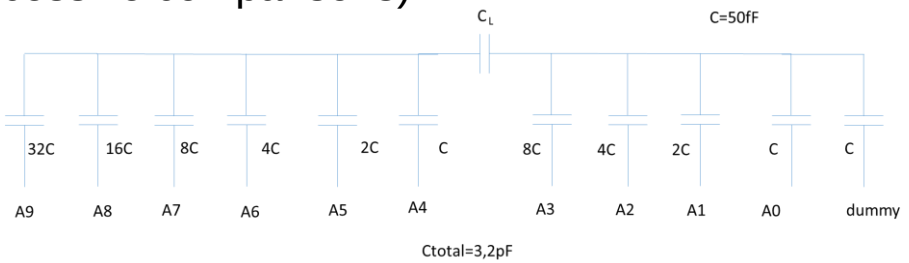


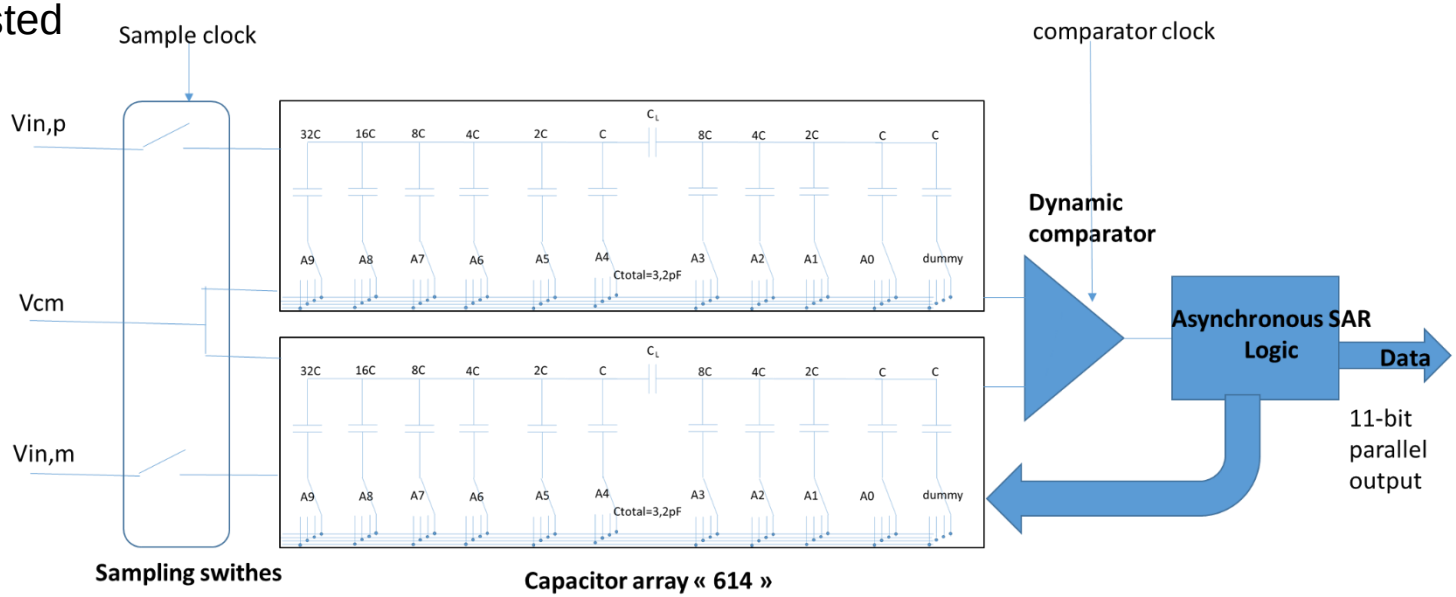
Different versions:

- Preamp: baseline, low parasitics cap (custom layout)
- 11b ADC: asynchronous and synchronous ADC, with and without bootstrap

TV2: ADC SAR

- 11-bit ADC SAR (MSB signal sign + 10 successive comparisons)
- Designed for 20 MSamples/second
- Design of 11-bit SAR ADC
  - Differential input signal
  - Based on a capacitive DAC architecture (« 614 » :Split 6b/4b DAC)
  - Based on a asynchronous SAR logic and tunable settling delay
- Power consumption ~3mW @ 20MHz (~50% capa array;~50% digital)
- 4 ADC SAR architectures in TV2 (w and w/o bootstrap; asynchronous/synchronous) to be tested





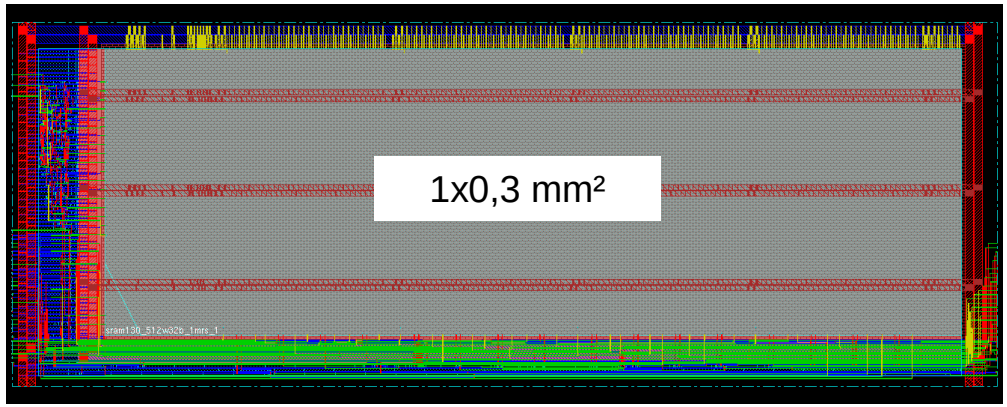
TV2: L1 Buffer SRAM

- L1 Buffer in TV2 (TSMC 130 nm):
  - 512w x 32 bits
  - Use CERN memory generator
  - 1 SRAM / channel (in TV2)
  - Full digital power consumption spec: 5mW/ch

	Area mm²	Power mW / ch	Processing Time (ns)
RAM 32b x 512w	0,35	**~ 4**	R @ 1 MHz W @ 40 MHz

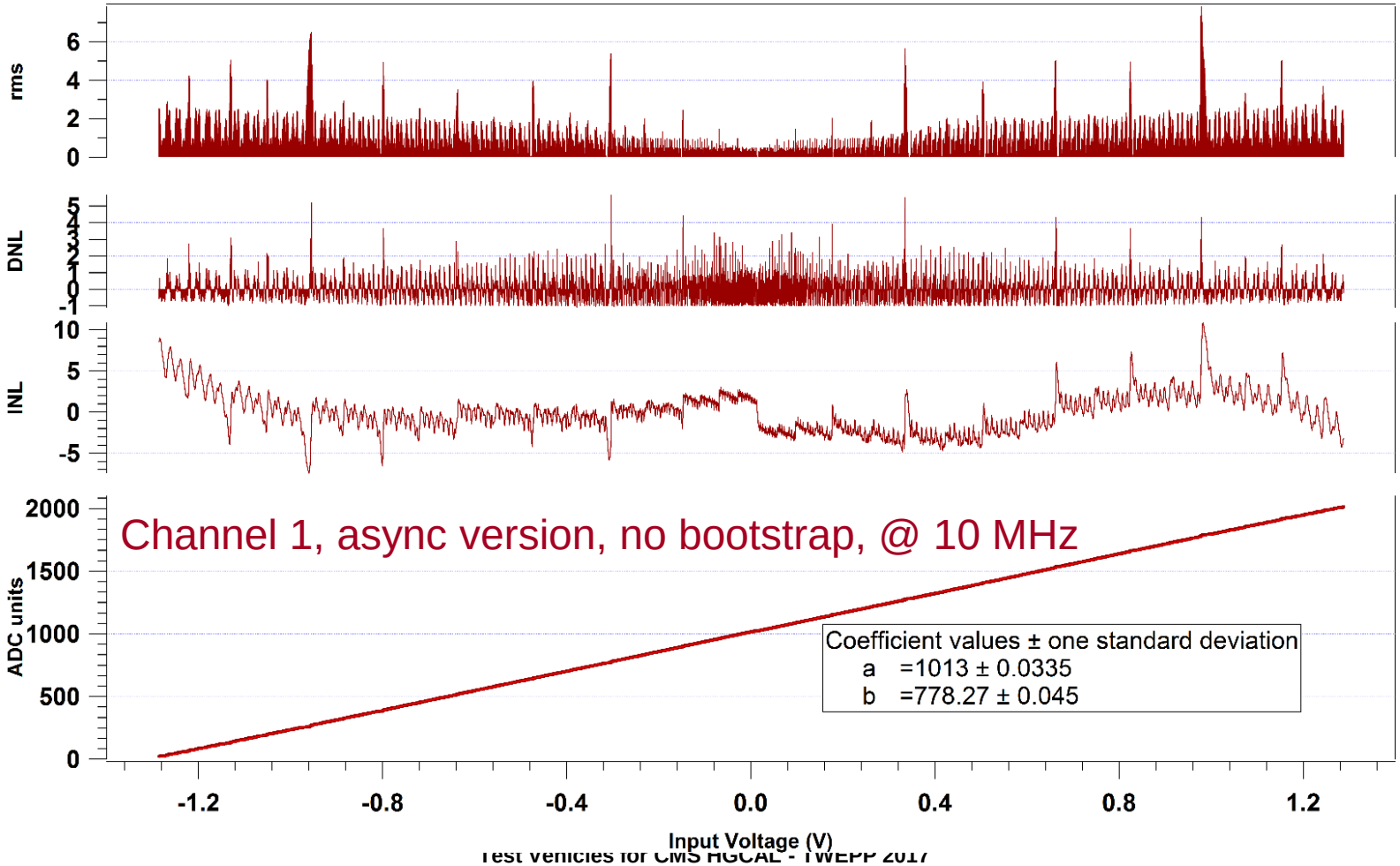
	energy READ*	energy WRITE*	energy R&W*	energy NOP	leakage
	uW/MHz	uW/MHz	uW/MHz	uW/MHz	uW
WC	51.2	71.3	130.0	20.2	30.55
TC	65.7	85.6	148.4	16.1	3.75
BC	86.5	108.2	179.9	24.9	5.06
TL	70.5	93.3	161.9	24.7	90.53
LT	81.5	105.5	187.4	32.6	1.82
ML	98.9	128.4	223.1	33.6	283.22

Measured 3mW/SRAM with only 2x12 bits toggling (writing @40MHz, reading @1MHz, but ADC @ 10MHz)



TV2: SAR ADC tests

- Maximum sampling frequency: 15MHz, but 10MHz achieve better results
- DC characterization: INL, DNL, capa network
- Many parameters to be explored: delay, reference voltages, dynamic performance…



Preliminary

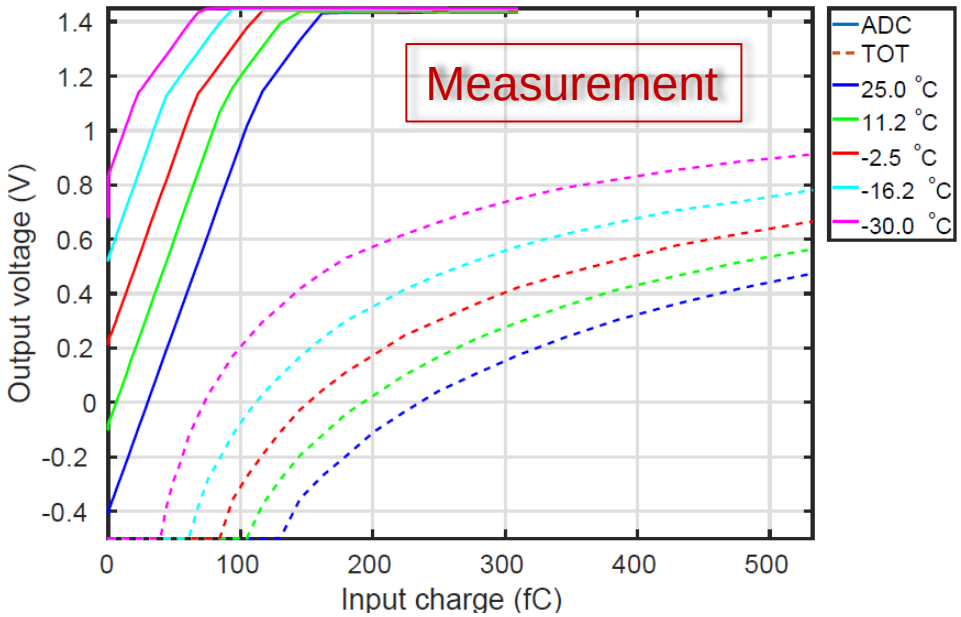
TV2: charge linearity

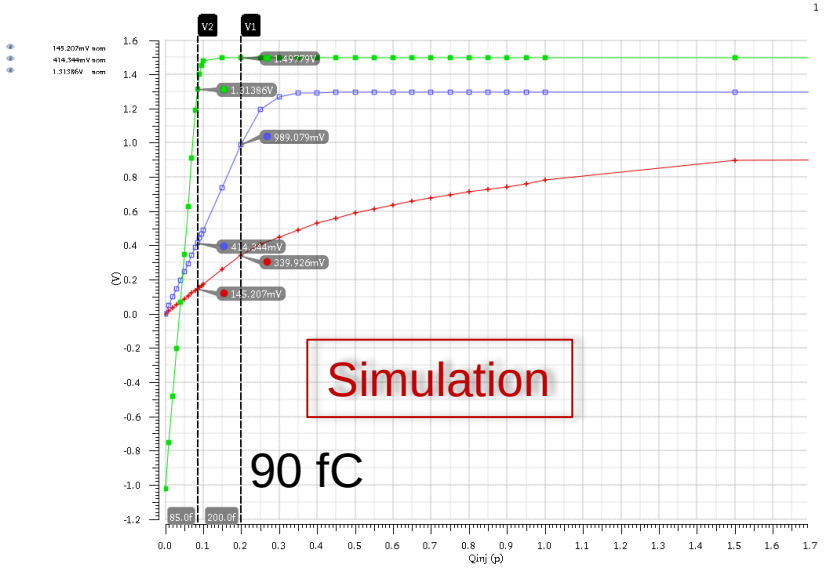
- Analog measurements (scope)

- Strong DC dependency to the Temp
  - DC coupled channel, gain 15
  - Input preamp 1mV/°C

  ⇒ 15 mV/°C at the ADC

  ⇒ See in room condition

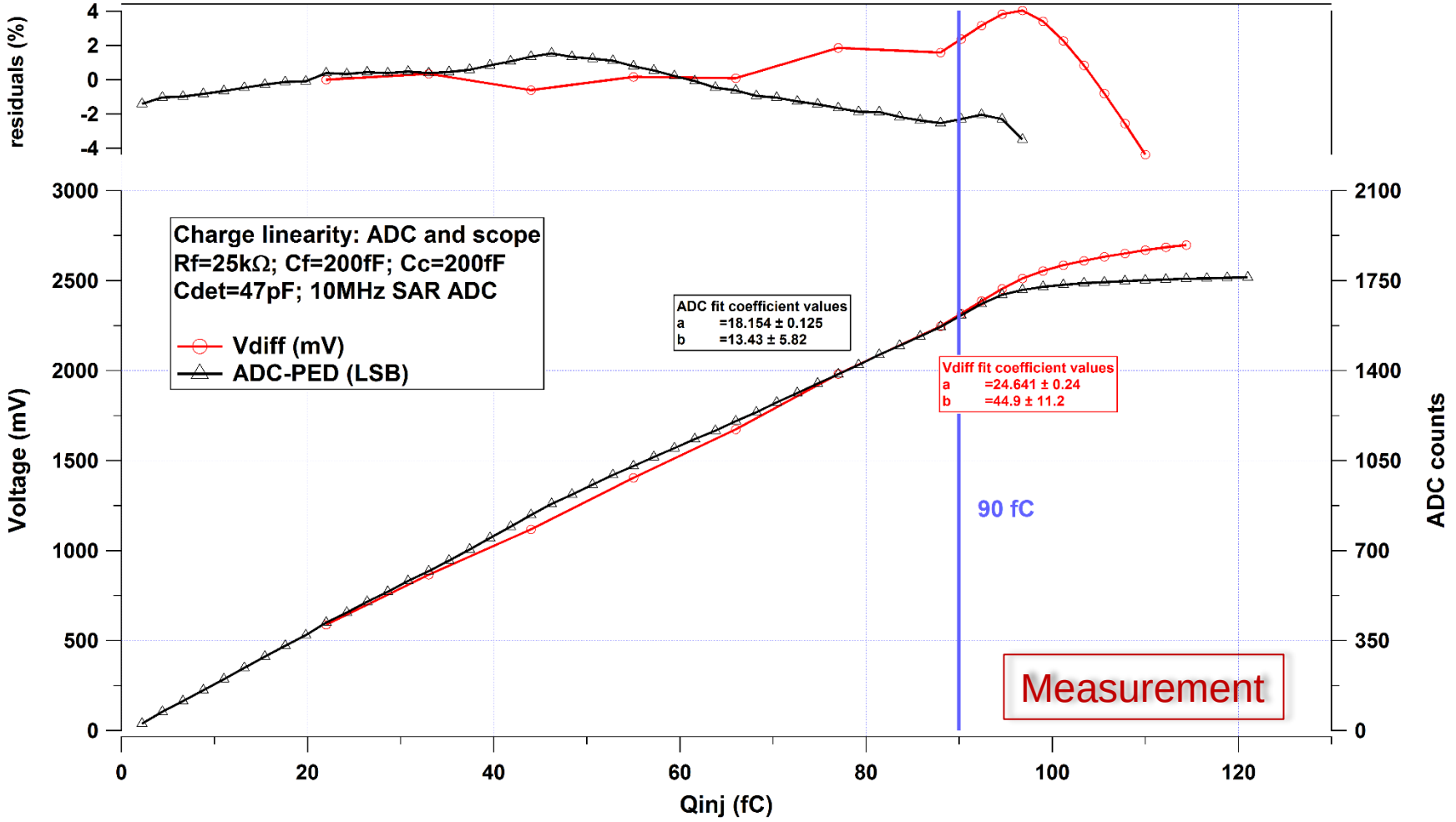




TV2: charge ADC linearity

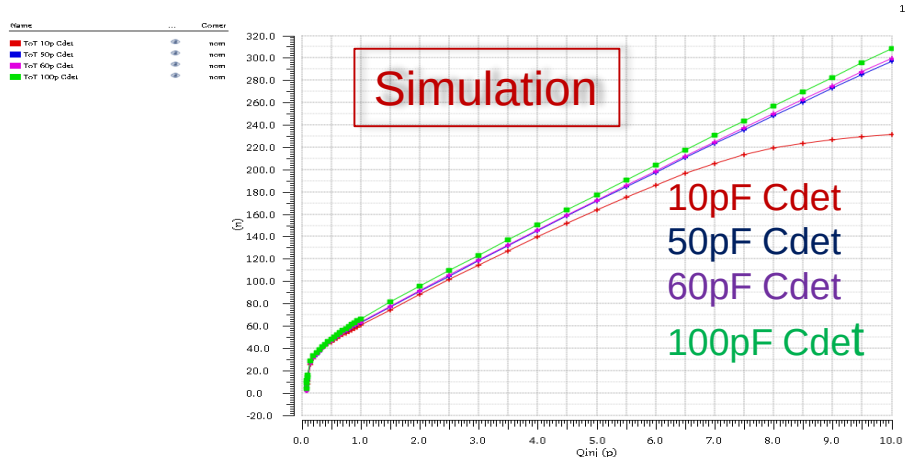
Good agreement between simulation and measurement

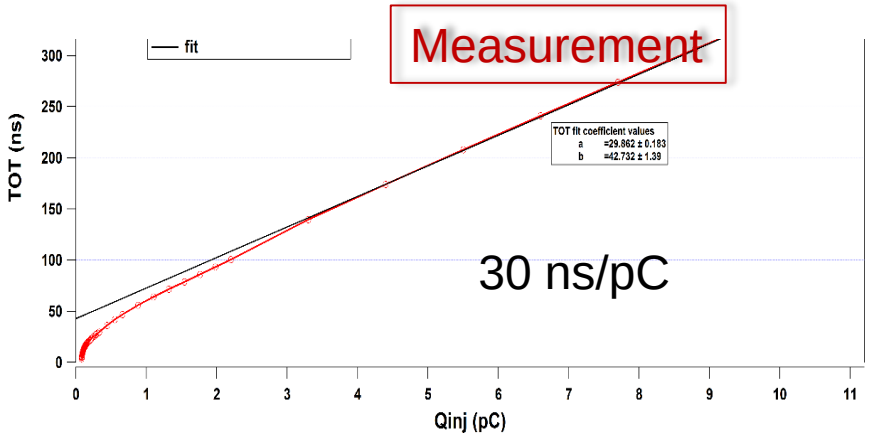
- Linear up to 90fC
- But ADC brings a non linearity, likely due to mismatches of its capa network (half range)

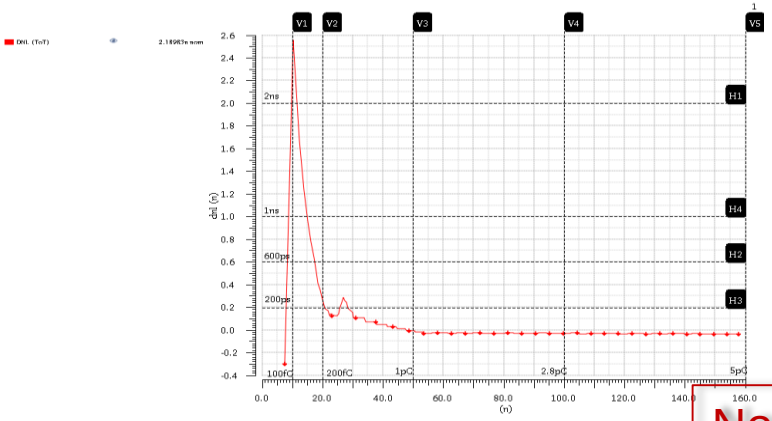


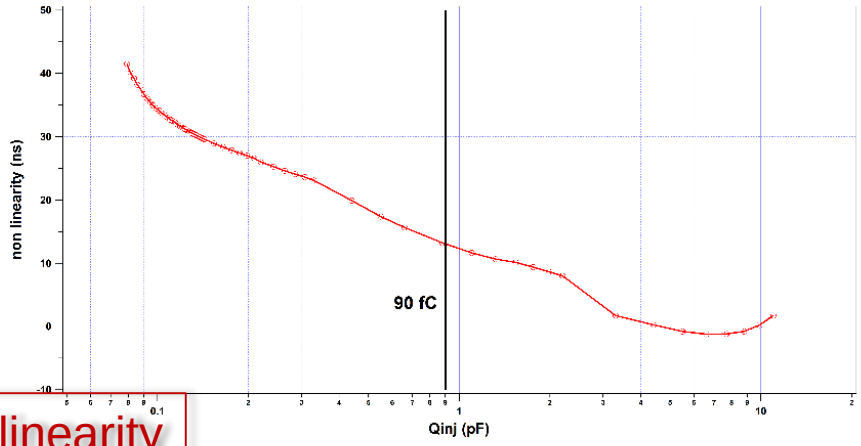
TV2: TOT linearity

Good performance of TOT but after 3pC, 1pC in simulation => have to be understand







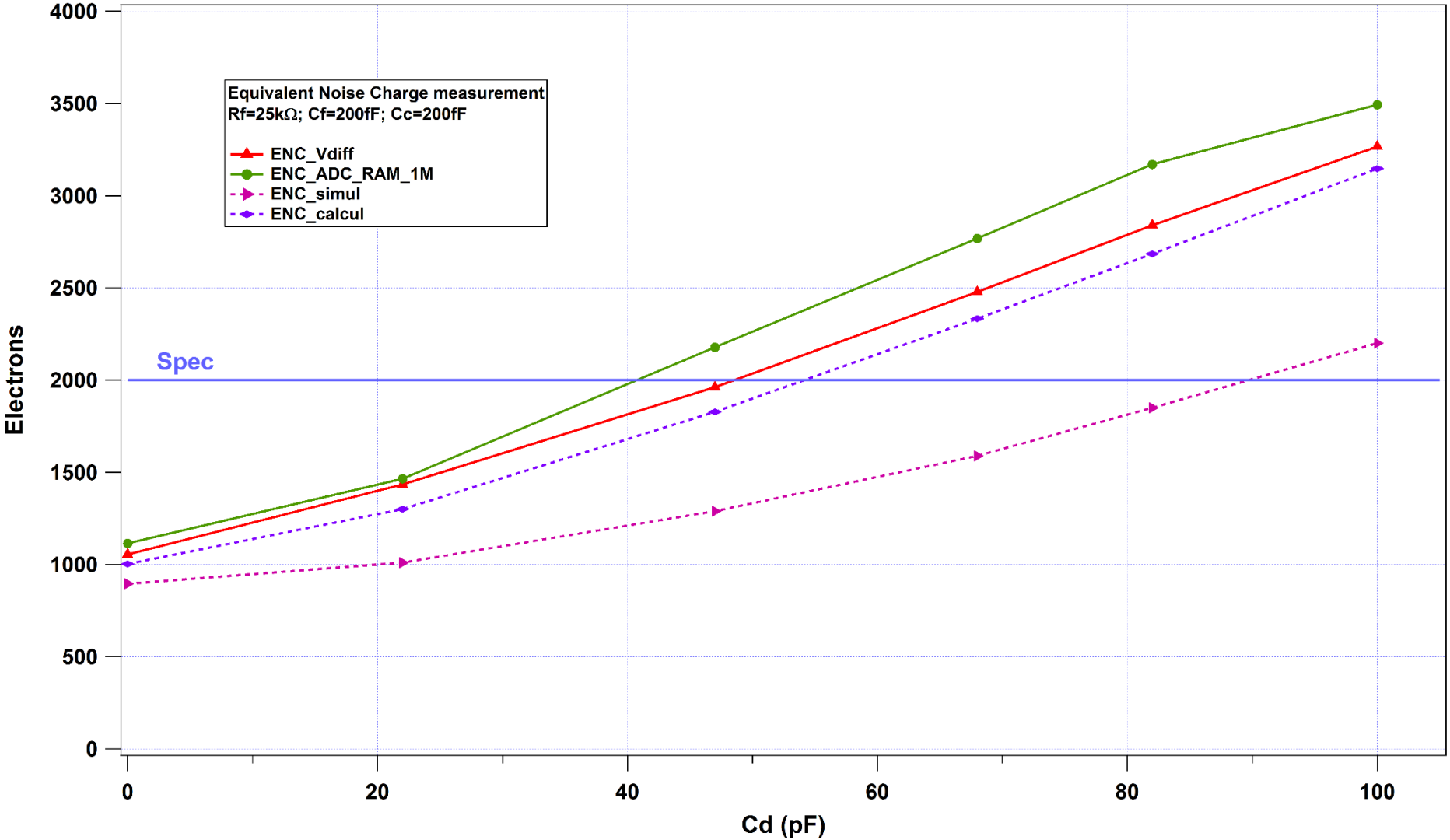


Jitter on TOT

- Spec < 50ps
- @ 200 fC 30ps simulated, 75ps measured

TV2: Noise measurements

- Spec 2000 electrons with 50pF detector capacitance
- OK without ADC and running RAM
- Discrepancy between simulated and theoretical/measured values

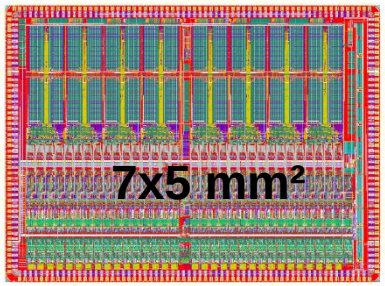


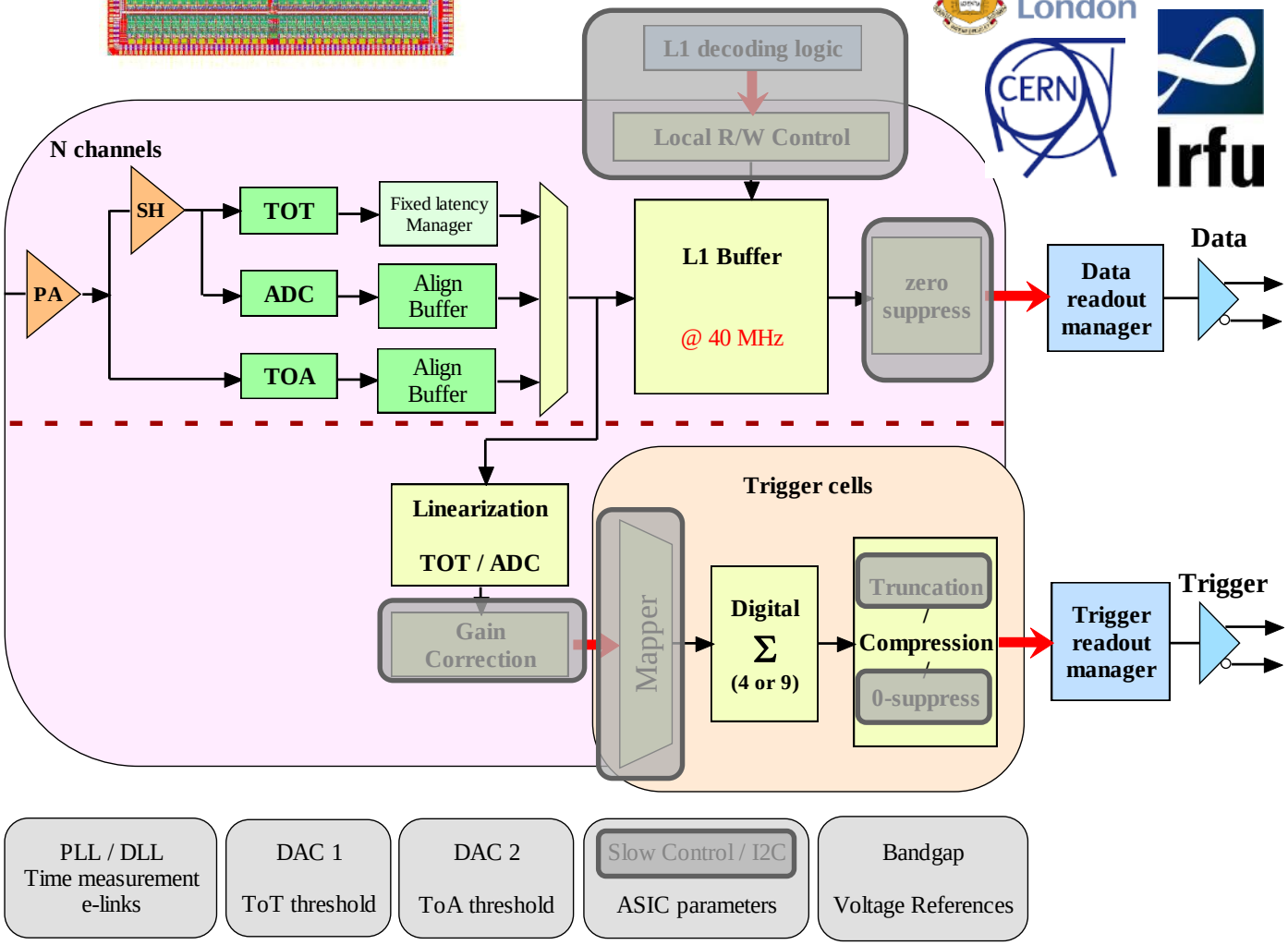
HGROCv1

Collaborative ASIC

HGROCv1 features:

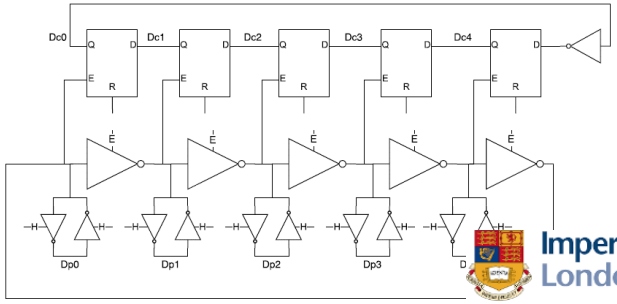
- 32 channels
- Dual polarity
- TOT with 2 variants:
  - Low power @ Imperial
  - DLL @ OMEGA (CERN based)
- TOA (CEA-IRFU)
- 11-bit SAR ADC @ 40MHz (OMEGA)
- Simplified Trigger path
  - Only sum by 4
  - No 0-suppress (4+4 log)
- Data readout @ 320MHz
- SC with triple voting (shift register like SK2-CMS)
- Many digital block with simplified architecture
- Services
  - Bandgap from CERN
  - PLL from CEA-IRFU
  - 10b DAC from TV2

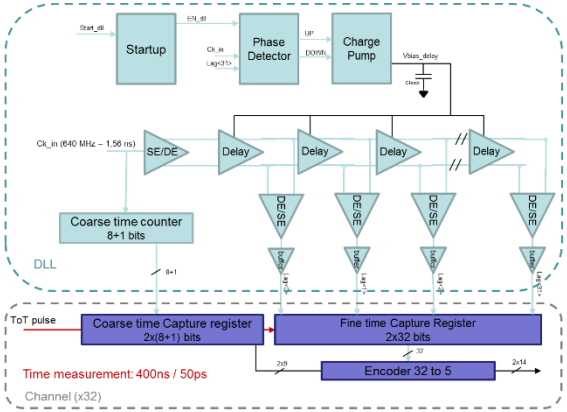


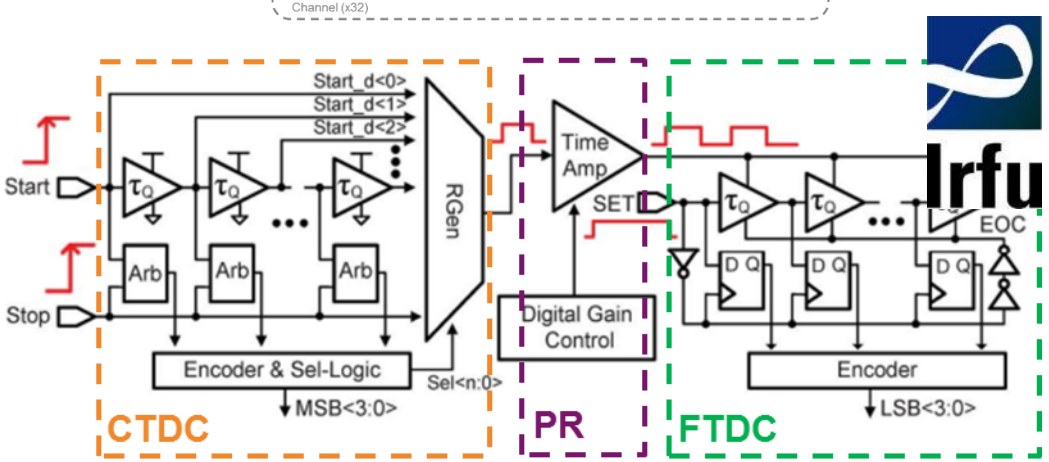


HGROCv1: mixed signal blocks

- ADC
  - OMEGA design, 11 bit, 40MHz
- 2 TDCs for TOT
  - IC design, 50ps/200ns, based on a ring oscillator
  - OMEGA design, 50ps/400ns, based on a global DLL running at 640MHz
- TDC for TOA
  - CEA-IRFU design
  - 10/11 bit, 24/12 ps binning
- PLL
  - CEA-IRFU design
  - 40MHz input clock
  - 1,28GHz VCO frequency



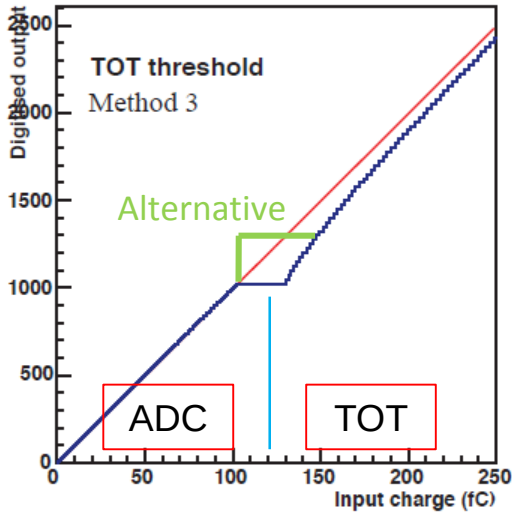




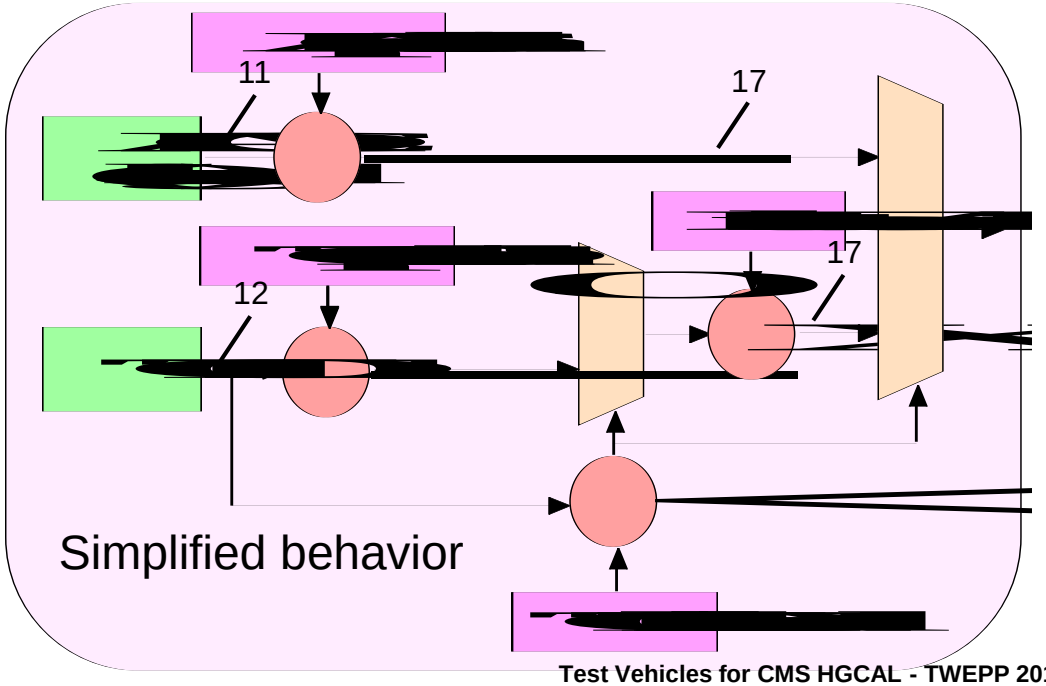
HGROCv1: ADC/TOT linearization for Trigger path

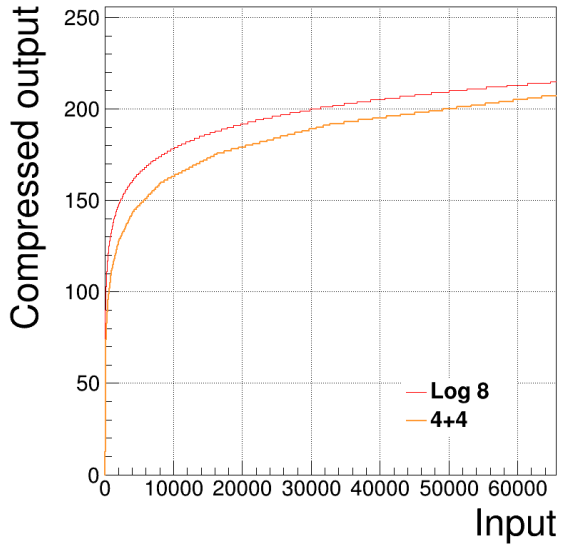
- Digitized charge data:
  - HG: 10/11-bit ADC for charge up to ~100/200 fC ➔ **LSB @ 0,1 fC**
  - LG: 12-bit TDC for the TOT (charge up to ~10 pC) ➔ **LSB @ 2,5 fC**

- Block needed to:
  - Compensate LSB ratio (~25) ➔ 17 bits
  - Automatic switching between ADC/TOT
  - Do the sum over 4 channels ➔ 17+2 bits
  - Compression: 4+4 encoding ➔ 8 bits
    - 4 bits for the MSB @ 1 position (Pos)
    - 4 bits for the following bits



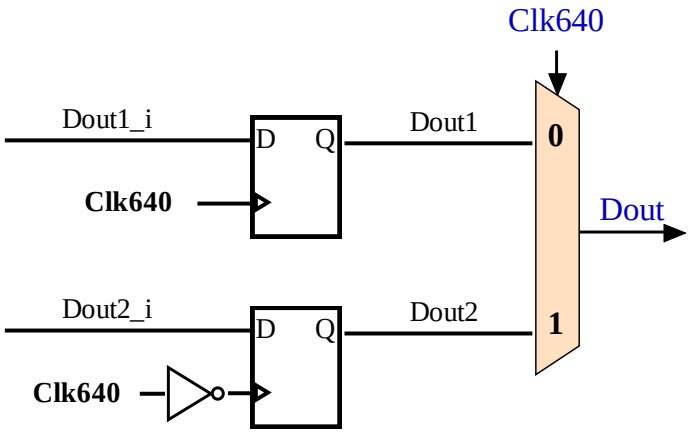
	Area µm²	Power µW/channel	Processing Time (ns)
Linearization + 2x2 sums	28 000 (175 x 160)	100-250 (post syn)	~25





HGROCv1: elink for trigger readout

- The chip integrates 2 elink transmitter to handle the 64 bits from the trigger path
  - 4 channels are encoded into 8 bits (with 4+4 encoding)
  - 2 variants (fully digital or mixed ➔ way the last mux is done)
  - Possibility to readout a known frame (set by SC)
  - Default is 1,28 Gb/s (640 Mb/s possible)

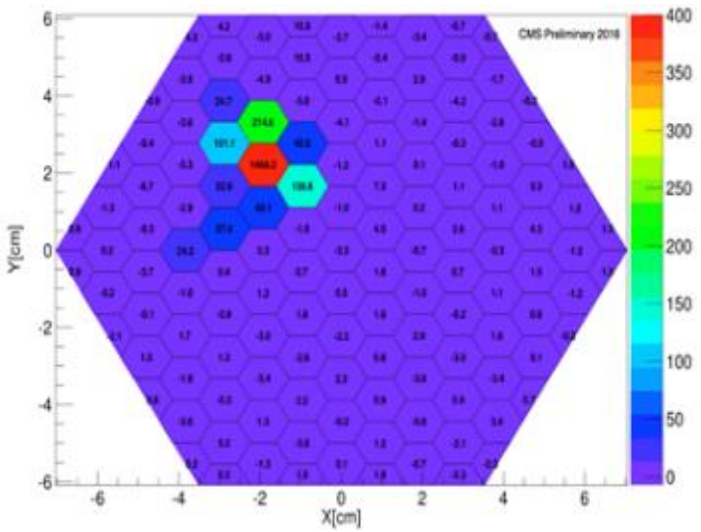


- Main specifications:
  - Data rate 1,28 Gb/s (internally 640M DDR)
  - Compatible with LpGBT protocol
  - Programmable Pre-emphasis (based on Paulo Moreira scheme)
  - Synchronization pattern on request (in place of trigger data)

Specification description	Value
Vcm (common voltage)	0,6 V
Vdiff (differential voltage)	100 to 200 mV
Pre-emphasis current	0,5 to 4 mA
Termination load	100 Ω

Conclusion

- Challenging ASIC
  - High speed low noise large dynamic range readout
  - High integration and large data output



- Several issues to be studied rapidly
  - ToT accuracy. Timing performance.
  - System issues.
  - Prototypes assembled for tests in beam

Additional slides

HGROCv1 analog channel

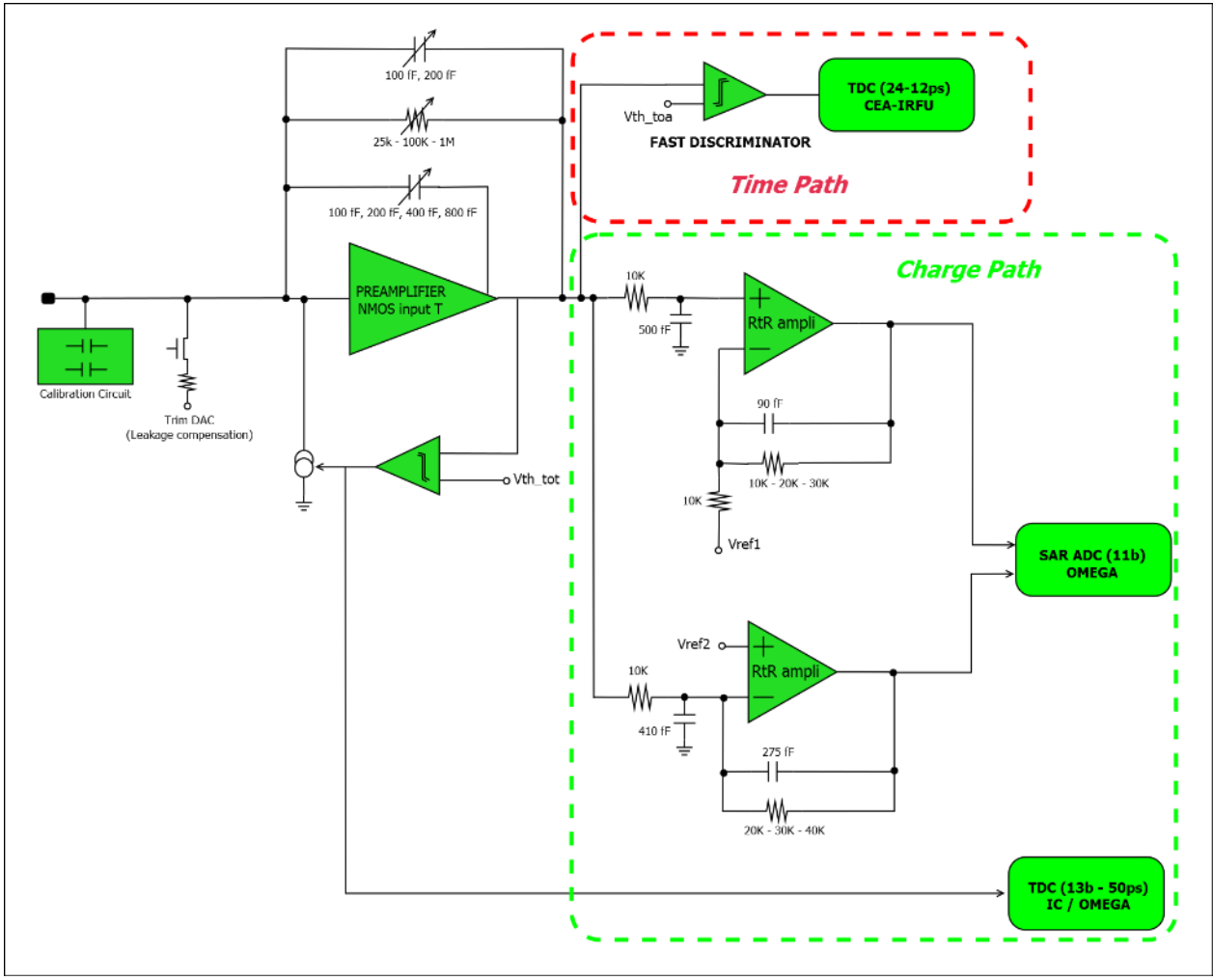
- Input DAC: leakage compensation over +/- 10µA to 300nA accuracy (30 mV preamp output DC shift)

- Cf = 0,1 0,2 0,4 0,8 pF
- Cf_comp = 0,1 0,2 pF
- Rf = 25k, 100k, 1M

- itot: 6bits global setting, 80µA max, 40µA default
- Vth_tot: 100mV – 1,2V dynamic range, 7bits global (0;1,2V;9mV), 5bits local (20mV;0,625mV)

- Single-to-differential shapers, 20-30ns peaking time; gain 2, 3, 4
- Vref1: 0 – 700mV, 7bits global
- Vref2: 0 – 700mV, 7 bits global, 5bits local

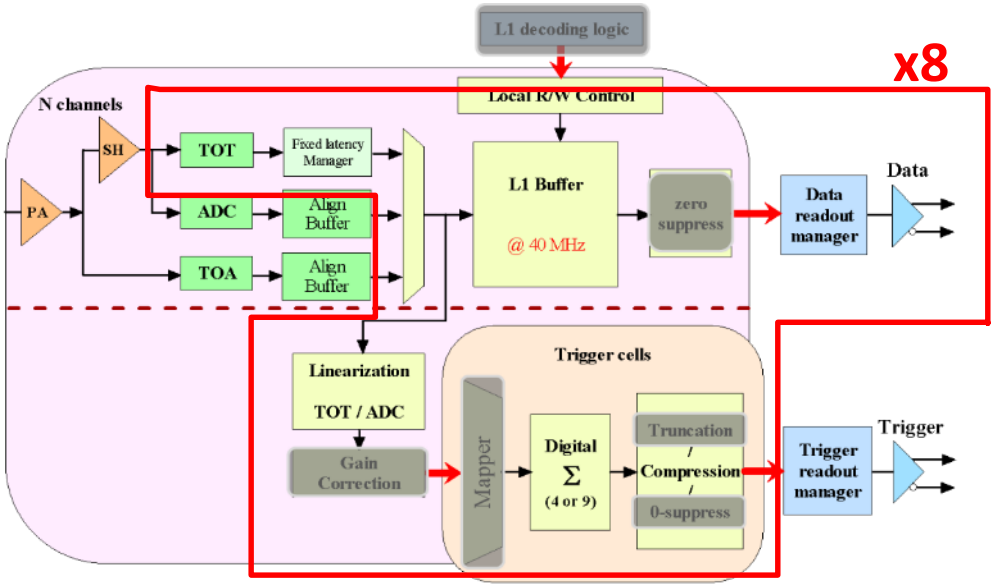
- Vth_toa: 0 – 700mV, 7bits global, 5bits local



Power dissipation @ 1,5V supply
- Vdda (preamp): 1,6mA
- Vdd (tot): 160µA
- Vdd(shaper, toa): 1,1mA

HGROCv1 “4 channels” block

- Main feature ➔ to be able to characterize analog + mixed signal blocks
- 1 digital block handles 4 adjacent channels: data path and 2x2 sums for trigger path
- The 32 channels have been grouped into cluster of 4 to fit the 2x2 sums
  - 1 digital block handles 4 adjacent channels + 2x2 sum
  - 2 clocks needed: 40 MHz + 320 MHz for data readout
  - External inputs available (raw data mode)

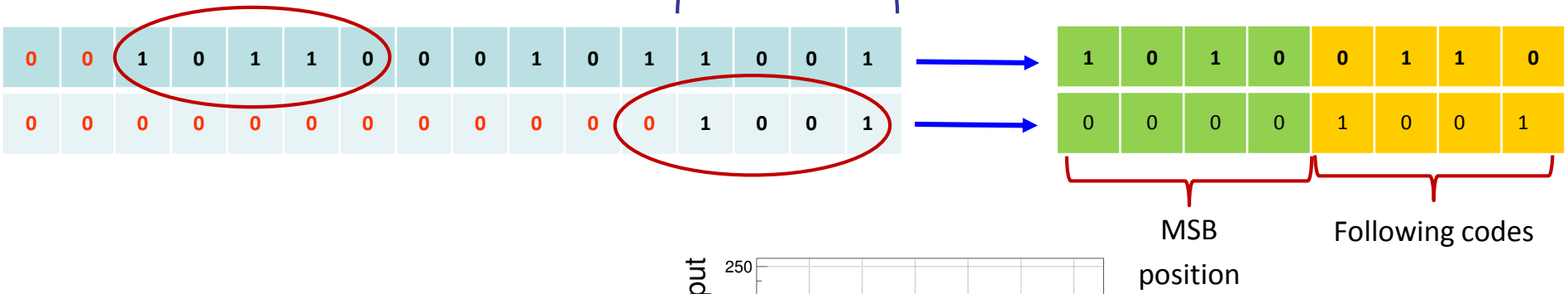


“Log” compression logic

- Compression with “4+4 encoding”:
  - Keep the 5 MSB of the linearized charge:
    - 4 bits for the MSB @ 1 position (Pos)
    - 4 bits for the following bits
  - Can keep special behavior if MSB@1 between LSB 0-4
  - Encoding on sensor:
    - 192 channels ➔ TC4 on 19 bits
    - 432 channels ➔ TC9 on 21 bits

```
If Qt < 16 then
   Pos = 0
   Bits = Qt(3 downto 0)
Else
   i = 15
   EndConv = 0
   Loop
      If Qt(i) = 1 then
         Pos = i
         Bits = Qt(i-1 downto i-4)
         EndConv = 1
      else   i--
   while (EndConv = 0)
```

Pos = 1,2,3 do not appear



	Area µm²	Power µW/channel	Processing Time (ns)
19 bits ➔ 4+4 encoding	1500 (175 x 9)	30 (post syn)	7