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MuTRiG: A Silicon Photomultiplier Readout ASIC with High Timing Precision and High Event Rate Capability

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The MuTRiG chip, which is dedicated to the Mu3e experiment, is a 32 channel mixed-signal Silicon Photomultiplier readout ASIC with high timing precision and high event rate capability designed and fabricated in UMC 180 nm CMOS technology. It combines the excellent timing performance of the fully differential analog front-ends and the 50 ps time binning TDCs with a high event rate capability from a dedicated on-chip digital logic circuit and a gigabit LVDS serial data link. The design of the chip and the results from the characterization measurements will be presented.

Summary

The Mu3e experiment is designed to probe new physics by searching for the lepton flavour violating decay of $\mu^+ \rightarrow e^+e^+e^-$ at a sensitivity level of 10^{-16}. A high timing resolution of 100 ps (σ) and 500 ps (σ) is required for the Mu3e Tile Detector and the Mu3e Fibre Detector, respectively, in order to suppress the combinatorial background below the signal level as well as to facilitate the event reconstruction. The event rate of the Fibre Detector will be at the level of 700 kHz/channel to 1.3 Mhz/channel, posing extra challenges to the detector system and the readout electronics.

MuTRiG is a mixed-signal Silicon Photomultiplier (SiPM) readout ASIC with high timing precision and high data rate capability. It is dedicated to the readout of the Mu3e Tile Detector and the Mu3e Fibre Detector. MuTRiG consists of 32 SiPM readout channels, each of which comprises an analog front-end and a Time-to-Digital Converter (TDC), as well as an integrated digital logic circuitry for event processing and data transmission to an external Data Acquisition system (DAQ). The analog front-end is designed in a fully differential structure to suppress the common mode noise from both the on-chip digital circuit and the external sources. The TDC has a binning of 50 ps, ensuring a precise time digitization. The analog front-end and the TDC have been extensively characterized with the STiCv3 chip and have proven an excellent timing performance. The digital logic circuitry has been upgraded to sustain the high input event rate as well as to provide additional functionalities such as external trigger function, channel event counters and CRC for data transmission error detection. A gigabit serial data link consisting of a Double Date Rate (DDR) serializer and a customized LVDS transmitter has been implemented in the MuTRiG chip to tackle the high event rate challenge from the Mu3e Fibre Detector.

Characterization measurements have shown an analog front-end jitter of less then 20 ps when injecting charge via a 33 pF capacitor, a Single Photon Time Resolution (SPTR) of 150 ps obtained with Hamamatsu S13360-1350CS MPPCs and reliable 8b/10b encoded data transmission at a data rate of 1.28 Gbps. In this paper we will present both the design and the characterization measurement results of the MuTRiG chip.

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