Contribution ID: **176** Type: **Oral**

FPGA Based Wireless Time Interval Measurement System with Picosecond Resolution

Thursday 14 September 2017 11:05 (20 minutes)

We present a theoretical analysis, simulation and implementation results of an FPGA-based wireless Time Interval Measurement (TIM) system. The TIM features a single channel TDC with a Serial Peripheral Interface (SPI) and wireless transmission. The TDC is based on the Vernier ring oscillator method to achieve both high resolution and wide dynamic range. The TDC architecture with an SPI is implemented in Altera Cyclone IV Device, and a wireless ZigBee module (IEEE 802.15.4 standards) is used for transmission of the measured time interval values. The paper concludes with the description of the prototype application to investigate SPAD after-pulsing.

Summary

Timing measurement is used to determine most of the physical quantities like the energy of a particle or crossing time. In mixed-signal systems used for timing measurement, TDCs are the vital building blocks used for digitizing of analog signals in time domain. The emergence of High Energy Physics (HEP) detectors measuring in sub 10 ps-rms resolution demand a high-resolution TDC for timing measurements in the ps-rms resolution to realize the full potential of today‘s HEP detectors.
Compared to full-custom CMOS ASIC, FPGAs have advantages in the implementation of fully digital TDC architectures as it provides benefits such as cheaper development cost, customizability, etc. The prototype discussed in this paper is implemented in an FPGA.The standard uncertainty for the time intervals from 0 to 30 ns were less than 17.43 ps-RMS with the resolution of approximately 10 ps and reliable wireless data transmission using Zigbee protocol.

Primary authors: Mr SRINIVASAN, Balaji (LICET); Dr S, Ramasamy

Presenter: Mr SRINIVASAN, Balaji (LICET)

Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods