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DRM2: the Readout Board for the ALICE TOF Upgrade

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For the upgrade of the ALICE TOF electronics, we have designed a new version of the readout board, named DRM2, a card able to read the data coming from the TDC Readout Module boards via VME. A Microsemi Igloo2 FPGA acts as the VME master and interfaces the GBTx link for transmitting data and receiving triggers and a low- jitter clock. Compared to the old board, the DRM2 is able to cope with faster trigger rates and provides a larger data bandwidth towards the DAQ. The measurements on the received clock jitter and data transmission performances in a full crate are given.

Summary

The ALICE Time Of Flight (TOF) detector is a large array of Multi-gap Resistive-Plate Chamber (MRPC) strip detectors for particle identification in the intermediate momentum range at the ALICE experiment (CERN). Each of the 18 sectors is read out by four VME electronic crates, each hosting 9 or 10 TDC Readout Module (TRM) boards and one Data Readout Module (DRM) card. In order to cope with an increase in the trigger rate up to 200 kHz in proton-proton collisions and 50 kHz in lead-lead collisions, we have designed a newer board, named Digital Readout Module 2 (DRM2). The card features a faster link towards the data acquisition system using the GBTx ASIC and VTRx optical transceiver from CERN, which allow a user bandwidth towards the Data AcQuisition system (DAQ) of 3.2 Gb/s. The readout will be implemented with synchronous triggers at fixed bunch crossing at 100 KHz,
setting a matching window of 10 microseconds in the TDC ASIC installed in the TRMs,
the HPTDC. This solution will mimic a full-fledged continuous readout as the one implemented in the new ALICE TPC and ITS readout. The same link is also used for receiving triggers and a low-jitter clock, which is distributed to the front-end electronics. For the TOF detector the quality of this clock is crucial and a campaign of measurements on the clock received from the ALICE data acquisition card named CRU (Common Readout Unit) has been done: we measured a RMS clock jitter as low as O(10) ps, which is compatible with the requirements.
The heart of the board is a Microsemi Igloo2 FPGA, which is a Flash-based device. This device has been chosen since the expected TID (Total Ionizing Dose) for the board (4 meters far from the beam pipe) is 0.13 krads in 10 years, which is acceptable for such a device. The advantage is that the FPGA configuration memory is SEU (Single Event Upset) immune, so that scrubbing is not needed. Upon reception of a trigger, the Igloo2 FPGA drives the VME interface using the VME64x 2eSST feature for reading out the TRM boards at 160 MB/s and packs events towards the GBTx link, which are then sent to the CRU.
The FPGA implements a proprietary 1.25 Gbps serial link from CAEN, named CONET2, which is used for reading temperatures, voltages and for monitoring physics data. The DRM2 board also hosts an Atmel ARM processor running Linux on a commercial piggy-back mezzanine (named A1500 from CAEN), whose purpose is to remotely re-program the Igloo2 FPGA via an Ethernet link when a new firmware revision is released and some other slow-control functionalities.
The paper will present the design details of the DRM2 board, together with the measurement results of the performances obtained working with DAQ cards (CRU and C-RORC), for what concerns both the received clock quality and the data transmission bandwidth towards the DAQ.

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