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New Slow Control FPGA IP for GBT Based Systems and Status Update of the GBT-FPGA Project

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The GBT-FPGA, part of the GBT project framework, is a VHDL-based IP designed to offer a back-end counterpart to the GBTX ASIC, a radiation tolerant 4.8 Gb/s optical transceiver. The GBT-SCA (Slow Control Adapter) radiation tolerant ASIC is also part of the GBT chipset and is used for the slow control in the HEP experiments. In this context, a new module named GBT-SC has been designed and released to handle the slow control fields hosted in the GBT frame for Internal Control (GBTx) and External Control (SCA). This paper presents the architecture and performance of this new module as well as an outline of recent GBT-FPGA releases and future plans.

Summary

The GBT-FPGA project was launched in 2009 following a study that consisted in validating the implementation of the GBTX serializer-deserializer in FPGAs. The project then gradually evolved to provide a common and centrally supported VHDL core to the GBT community. This IP, available for many FPGAs, ensures proper communication with the GBTX ASIC through the GBT link. This complete communication architecture has been widely selected for the upgrades of the DAQ, trigger and timing systems of the LHC experiments.

Based on the GBT chipsets, this system is divided into two parts: the Rad-hard ASICs, which are used close to the detectors, and the back-end modules implemented in FPGAs. The GBT-FPGA core offers a back-end counterpart to the GBTx, compatible with GBT frame definition and providing a 4.8 Gb/s high-speed serial link. The communication is typically done using the GBT protocol which is organized in frame of 120 bits sent at 40MHz. The frame structure can be divided in 5 fields: the header, Internal Control (IC), External Control (EC), payload and Forward Error Correction (FEC). The GBTX can be configured to divide the payload in up to 40 fields, called e-links, dedicated to the communication with front-end chips. The EC field is an additional e-link specifically designed to be used for the control of the GBT-SCA. Finally, the IC field is internally used for the configuration of the GBTX.

The GBT-SCA is a radiation tolerant chip that is used by the LHC experiments for the slow control of the front-end electronics. It provides several interfaces that can be controlled by a set of internal registers: 32 General Purpose IOs pins, up to 16 concurrent I2C masters, one SPI master with 8 slave select outputs, one JTAG master, up to 32 ADC inputs including one hard-wired internal temperature sensor and 4 DAC outputs. The GBT-SCA follows the HDLC communication standard by means of an 80 Mb/s serial lane, which is driven by a dedicated GBTX e-link. However, all of the general purpose e-links can be used for this purpose meaning that up 41 GBT-SCA chips can practically be concurrently controlled over the same GBT link.

A new VHDL module, released in spring 2017, fully compliant with the GBTX and the GBT-SCA ASICs, has been designed by the GBT-FPGA team in order to provide a common IP dedicated to Slow Control. Named GBT-SC, it offers a simple solution to manage the Internal and External Control fields of the GBT frame and can be instantiated in complement to the GBT-FPGA IP. Allowing to control between 1 and 41 SCAs, it features parallel configuration of several chips and is optimized in terms of latency and resource. Finally, additional acceleration modules are implemented in example designs to speed up as much as possible the use of the GBT-SCA interfaces. These goal are to limit the impact of the protocol used to control the firmware and can be additionally implemented depending on the requirements.

This talk introduces the new GBT-SC IP with a presentation of its architecture and performance as well as a summary of the recent GBT-FPGA developments and future plans.

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