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Characterization and Verification Environment for the 65 nm Pixel Readout-Chip RD53A

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For the Phase II Upgrade of LHC, new hybrid silicon pixel detectors are required for charged particle tracking. The RD53 collaboration is currently designing a large-scale prototype sensor readout chip "RD53A", which will be available soon. The SiLab group at the University of Bonn is highly involved in testing/verification and several chip design tasks.

A modular and versatile test- and data acquisition system for this next generation pixel readout is being developed to perform single-chip and module measurements. The concept and implementation of this FPGA-based system, the software framework and first test results of RD53A will be presented.

Summary

Due to significantly increased hit rates, new readout chips with highly complex digital architectures will have to deliver drastically increased data rates and ensure unprecedented radiation tolerance, especially close to the interaction point. The collaboration "RD53"was formed to approach these challenges, by designing a pixel readout chip in a 65 nm CMOS process, suitable for the inner layers of both the ATLAS and the CMS experiment.

The design efforts for the 500-million-transistor RD53A chip are split in two fundamental parts: Full custom analog and synthesized digital. In order to verify the digital design and to characterize the prototype chips, a test- and data acquisition (DAQ) environment, consisting of software frameworks and dedicated FPGA-based hardware, is currently being developed in Bonn. The aim is to use the same Verilog/Python framework for the DAQ system hardware as well as during the design verification process. This is achieved by utilizing a Co-Simulation testbench environment and including the System-Verilog repository, which finally will be used to synthesize the digital part of RD53A into CMOS logic for production. This approach also allows for valuable feedback to the digital designers and more efficient firmware development, because it can already be evaluated with the behavioral model of the chip prior to its submission.

Several aspects of the existing USBpix3 DAQ system must be adapted for the needs of RD53A, in order to cope with the increased data rate of up to 5 Gbit/s using the Aurora 64b66b protocol in single- and multi-lane configurations. This requires a new variant of USBpix3 with several Multi-Gigabit-Transceiver channels, DDR3 memory for buffered readout and a new dedicated Single Chip Card (SCC) for the first measurements of the prototype chips. The SCC hosts the wire-bonded device under test, provides thermal management and allows for multiple powering schemes, including serial powering. As soon as the prototypes are available, characterization measurements will be performed with the new DAQ system.

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