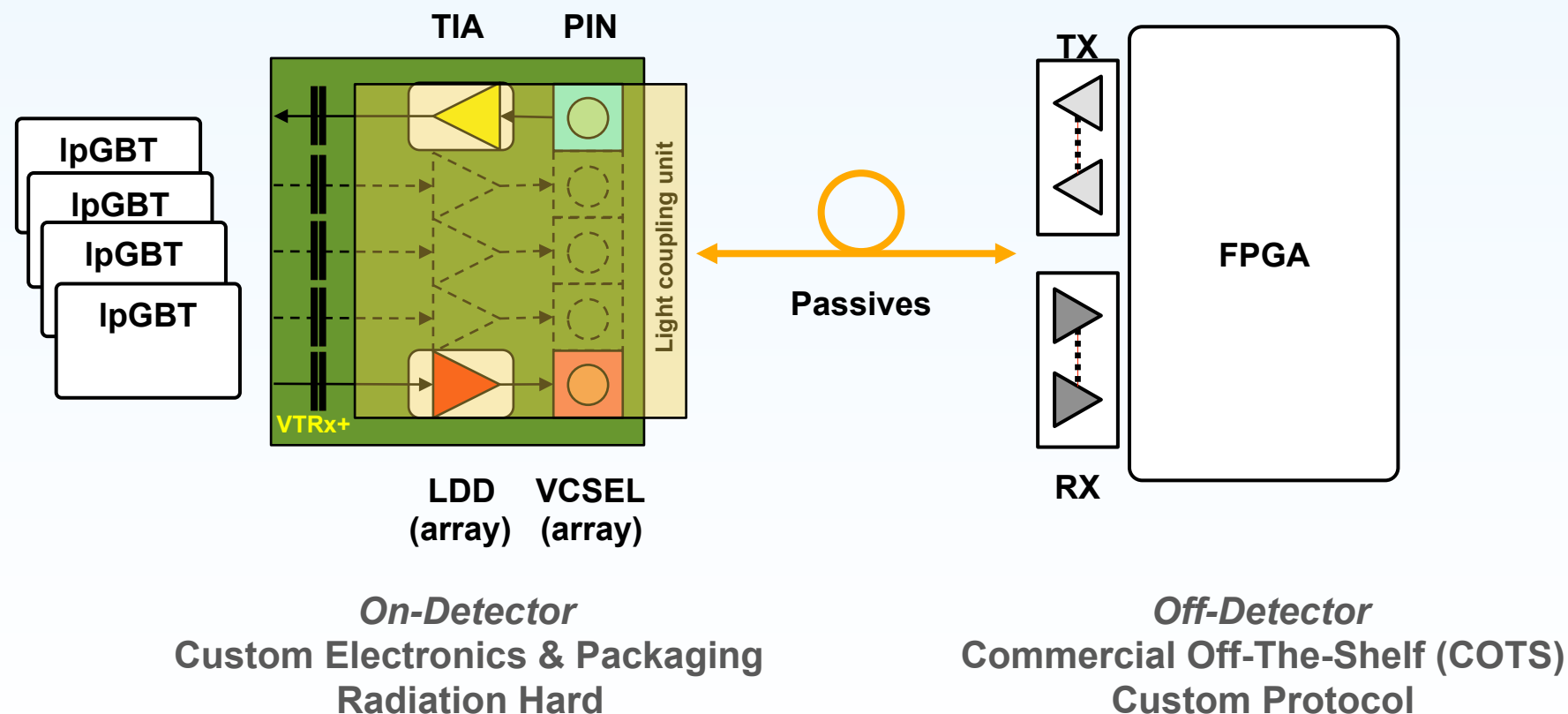


# The VTRx+, an Optical Link Module for Data Transmission at HL-LHC

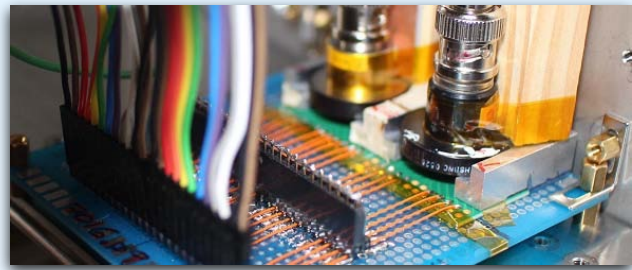


Jan Troska, Alexander Brandon-Bravo, Stephane Detraz,  
Andrea Kraxner, Lauri Olantera, Carmelo Scarcella,  
Christophe Sigaud, Csaba Soos, Francois Vasey

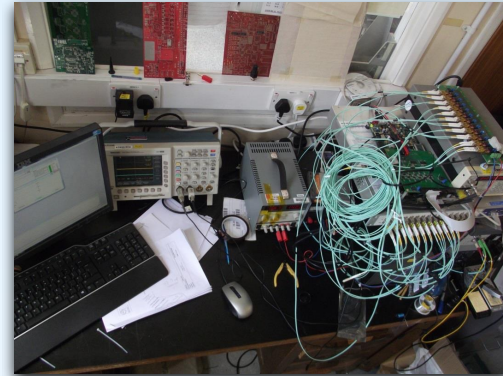
- Front-end to Back-end link targeting Inner Detector use at HL-LHC
  - Tracker-like environment
    - 1 MGy,  $3 \times 10^{15}$  n/cm<sup>2</sup>
    - -35 to +60 °C
  - Asymmetric Data-rates
    - 5 or 10 Gb/s upstream (out of detector)
    - 2.5 Gb/s downstream



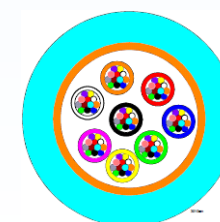
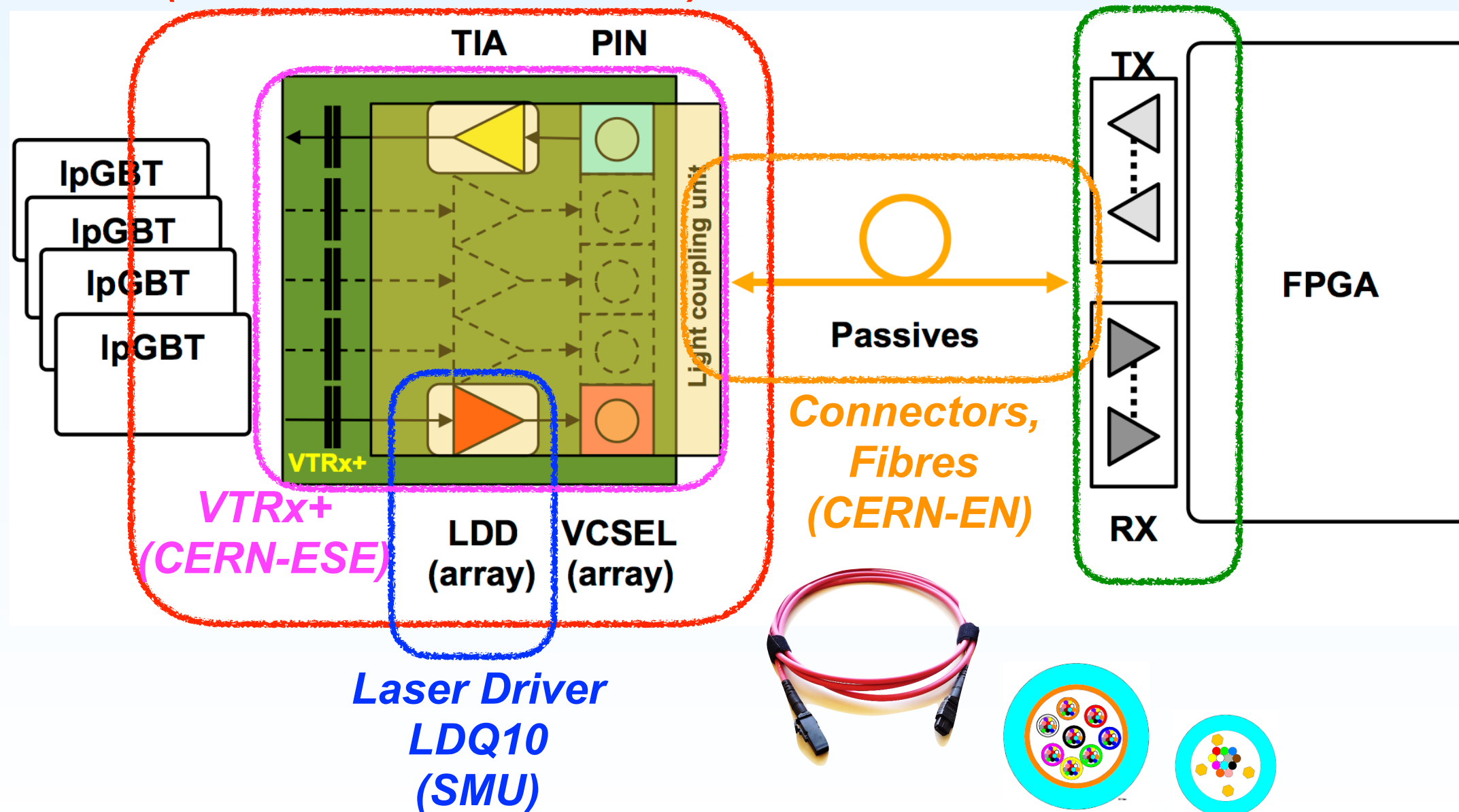
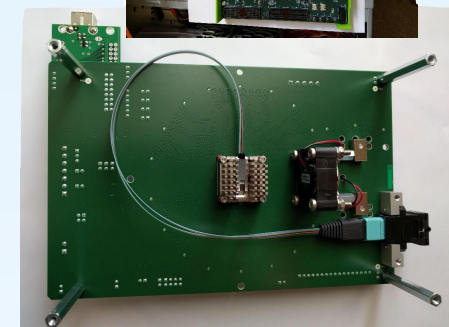
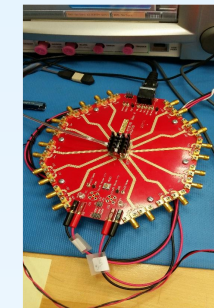
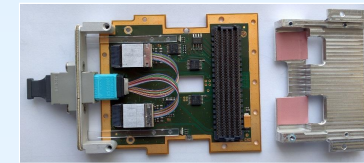
# VL+ project collaboration



**Reliability**  
(Oxford, Academia Sinica)



**Commercial  
Array TRx**  
(FNAL)



# System Specs

	<b>VTx+ to Rx (10Gbps)</b>	<b>Tx VRx+ (2.5Gbps)</b>
<b>Tx OMA</b>	> -5.2 dBm	> -1.6 dBm
<b>Rx sensitivity</b>	< -11.1 dBm	< -13.1 dBm
<b>Power budget</b>	> 5.9 dB	> 11.5 dB
<b>Fiber attenuation</b>	< 0.525 dB	< 0.525 dB
<b>Insertion loss</b>	< 1.5 dB	< 1.5 dB
<b>Link penalties</b>	< 1.0 dB	< 1.0 dB
<b>Tx radiation penalty</b>	< 1.0 dB	NA
<b>Rx radiation penalty</b>	NA	< 5.4 dB
<b>Fiber radiation penalty</b>	< 1.5 dB	< 1.5 dB
<b>Margin</b>	> 0.375 dB	> 1.575 dB

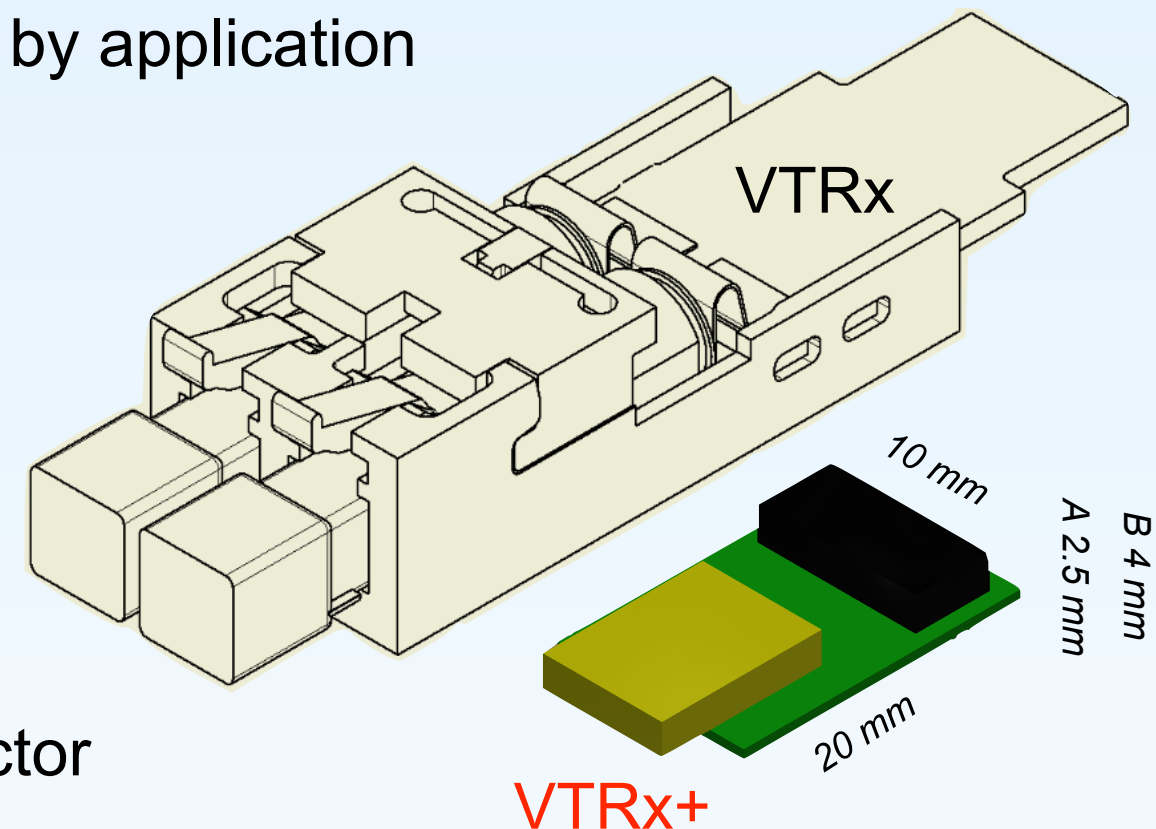
- Link Budget being defined
- Trade-off between requirements at either end of link
  - Penalties are asymmetric
  - Cannot simply apply standard e.g. 10 GbE specs

VTRx+  
Module

Commercial  
Module



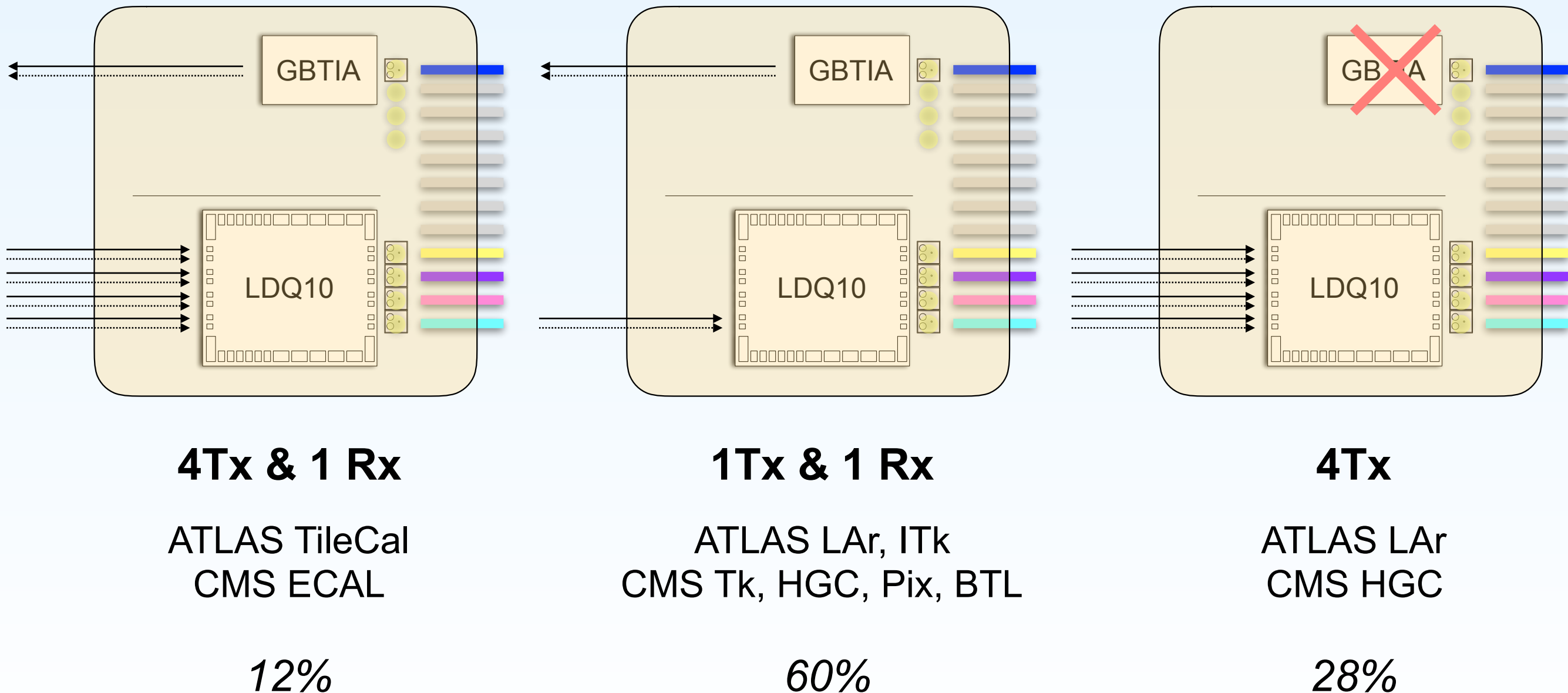
- Versatile
  - multi-channel, Rx/Tx count usage defined by application
- MM only
  - 850 nm VCSEL
  - InGaAs PIN (TBC)
- Miniaturized
  - Target dimensions 20 x 10 x 2.5/4 mm
- Pluggable
  - Either optical or electrical (or both) connector
- Data-rate matching IpGBT:
  - Tx: 5 and 10 Gb/s
  - Rx: 2.5 Gb/s
- Environment
  - Temperature: -35 to + 60 °C
  - Total Dose: 1 MGy qualification
  - Total Fluence:  $1 \times 10^{15}$  n/cm<sup>2</sup> and  $1 \times 10^{15}$  hadrons/cm<sup>2</sup>



*Total Quantity  
20000-50000 modules*

# VTRx+ module flavours & users

- Settled on using optical coupling block that can support up to 4 Tx and 1 Rx
  - Surveyed potential users to gain insight on the required quantities



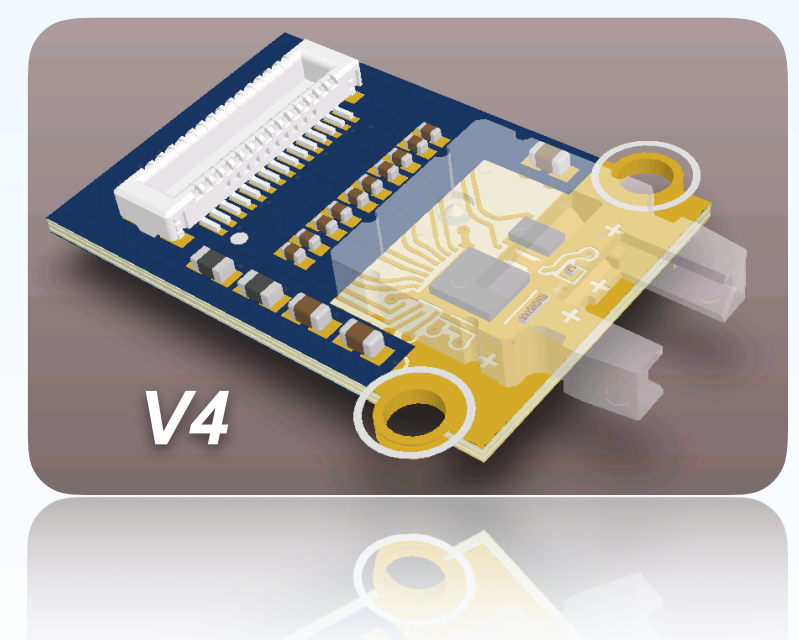
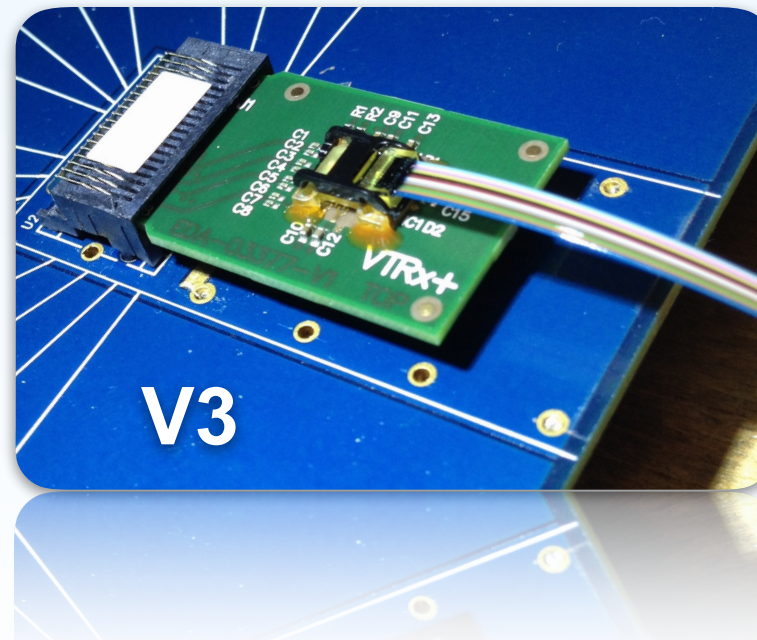
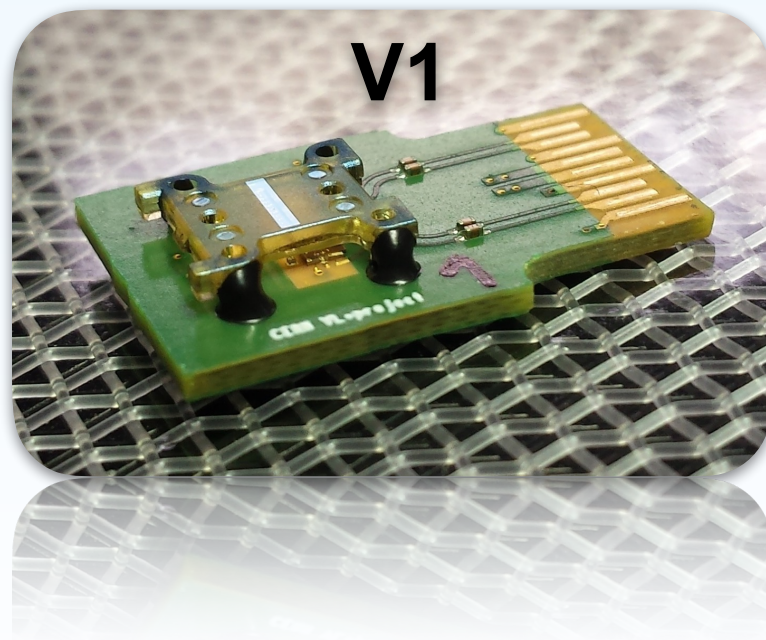
# Approach to VTRx+ prototyping

- Modification of existing commercial modules
  - Working in close collaboration with various industrial partners
  - Typical path
    - Identify interesting part
    - Procure opto-die only variant for environmental testing
    - Insert CERN-specified ASICs (LDD, TIA-LA)
- In-house design of module
  - Working in close collaboration with suppliers of optical coupling blocks
  - Working in close collaboration with industrial partner on integration
    - CERN-designed PCB
    - CERN-specified or procured opto-die
    - CERN-specified or procured ASICs (LDD, TIA-LA)

***! NDAs !  
limit sharing  
of design details***

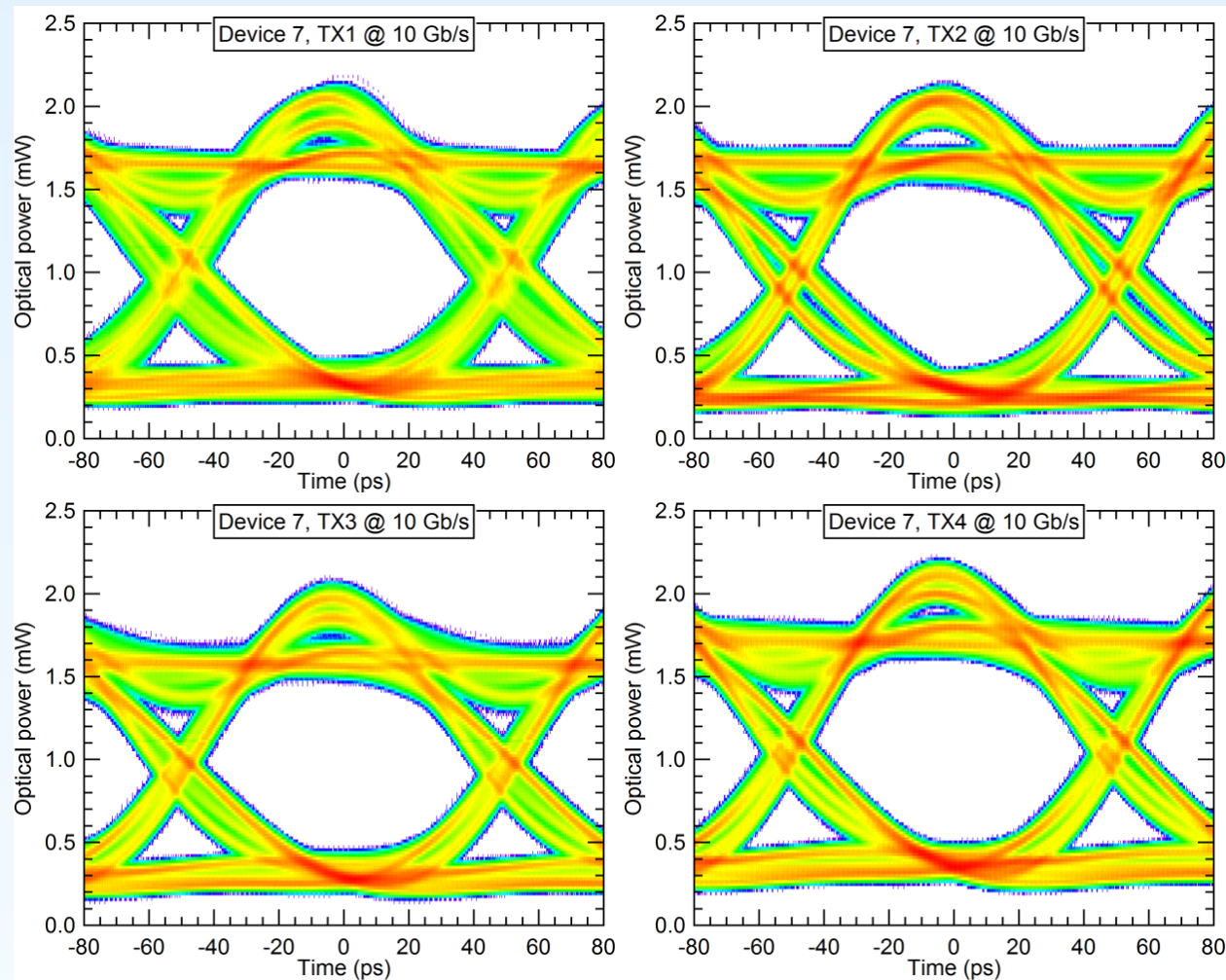
# CERN-design VTRx+ prototypes

Version	Tx		Rx		Light Coupling Block	Quantities
	LDD	VCSEL	TIA	PD		
V1	COTS	ULM14G	GBTIA	ULM14G PIN	12ch. MOI	9
V2	COTS	ULM14G	GBTIA	ULM14G PIN	2+2 Lightpeak	10
V3	LDQ10	ULM14G array	GBTIA	ULM14G PIN	12ch. MOI	7
V3b	LDQ10P	ULM/II-VI array	GBTIA	ULM14G PIN	12ch. MOI	5-10
V4	LDQ10	ULM/II-VI array	GBTIA	ULM14G PIN	2+2 Lightpeak	tbc

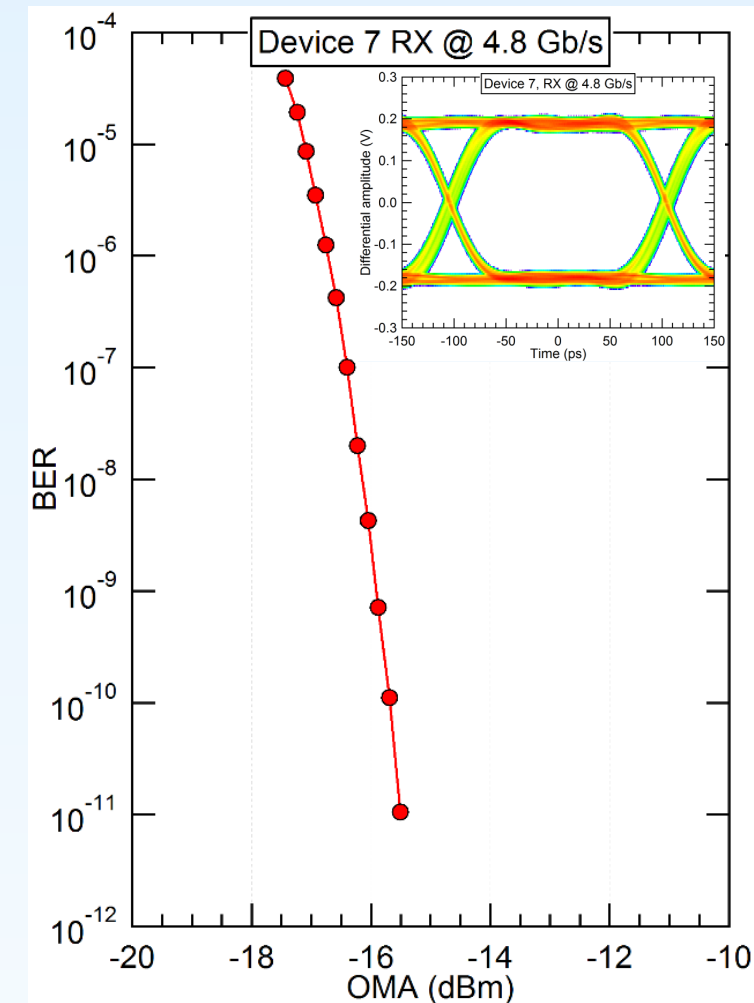




# Sample v3 VTRx+ results



- 10 Gb/s with default settings meets module spec.
  - Good coupling efficiency



- Rx operating with good margin
  - No influence of Tx operation on Rx performance



# Commercial roadmap

- Development (*until 2018*)

- CERN Market Survey

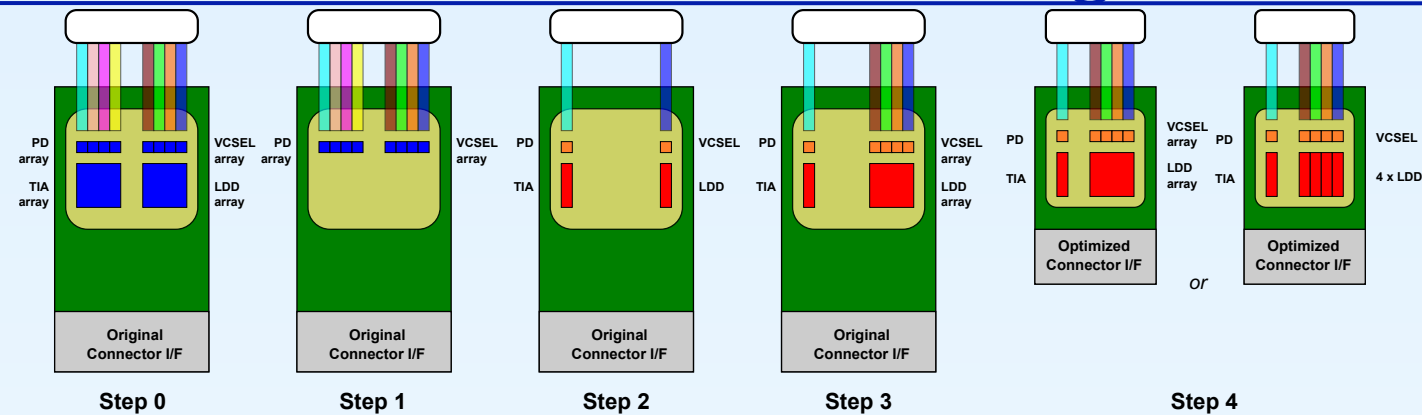
- CERN issues Technical Requirement & Questionnaire
- Companies return completed Questionnaire
- CERN reserves the right to order samples (Steps 0, 1) and/or ASIC drop-ins to existing parts for evaluation (Steps 2, 3)
- CERN qualifies companies having required technology

- CERN Price Enquiry

- Qualified companies receive full technical specification for development
- Qualified companies bid for development (Step 4)
- CERN develops customised prototypes with selected company(ies)

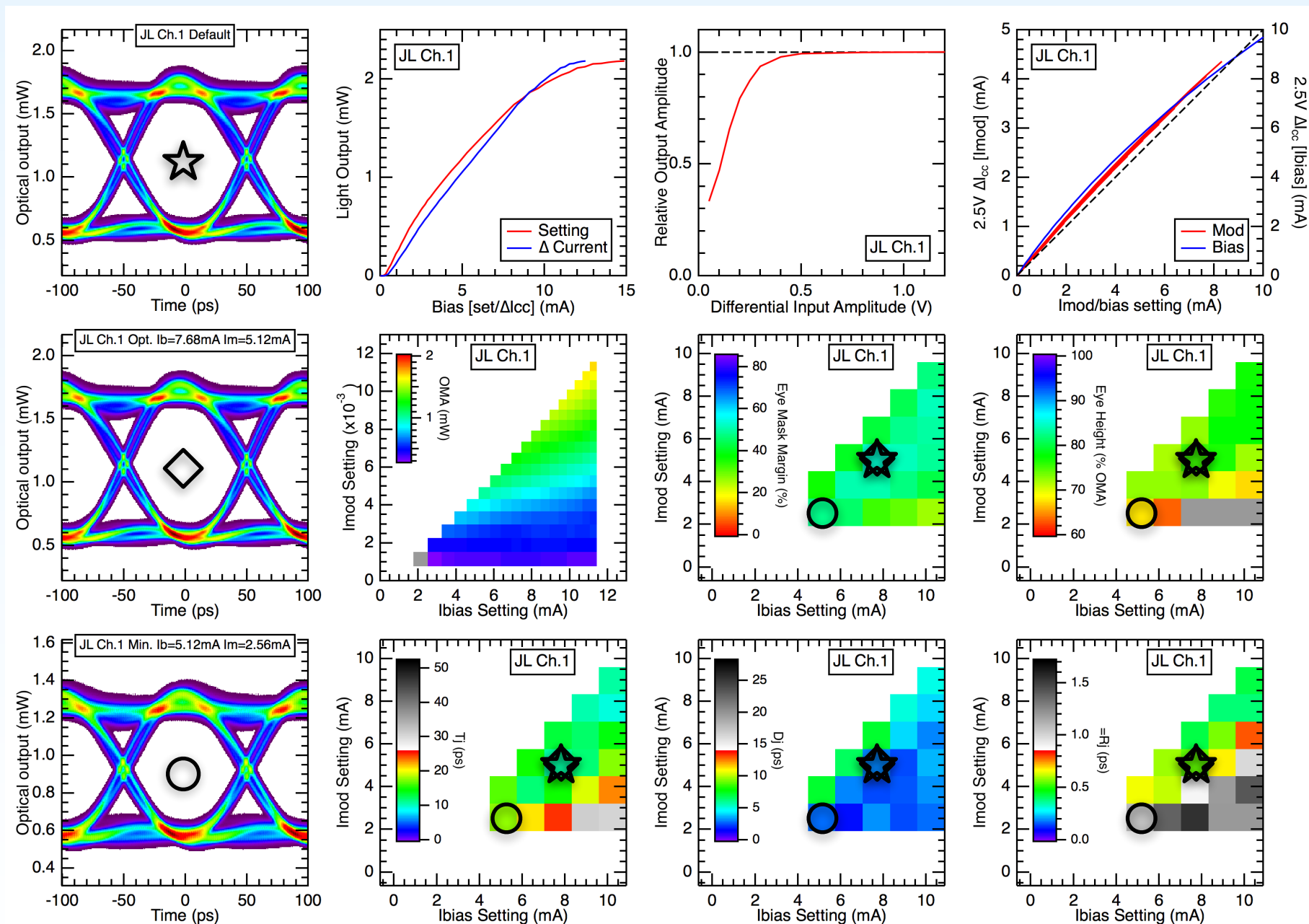
- Production (*2019 onwards*)

- Companies having successfully completed development (on time, in budget) will be invited to tender for full production
- One or two lowest cost bidder(s) will receive production contract



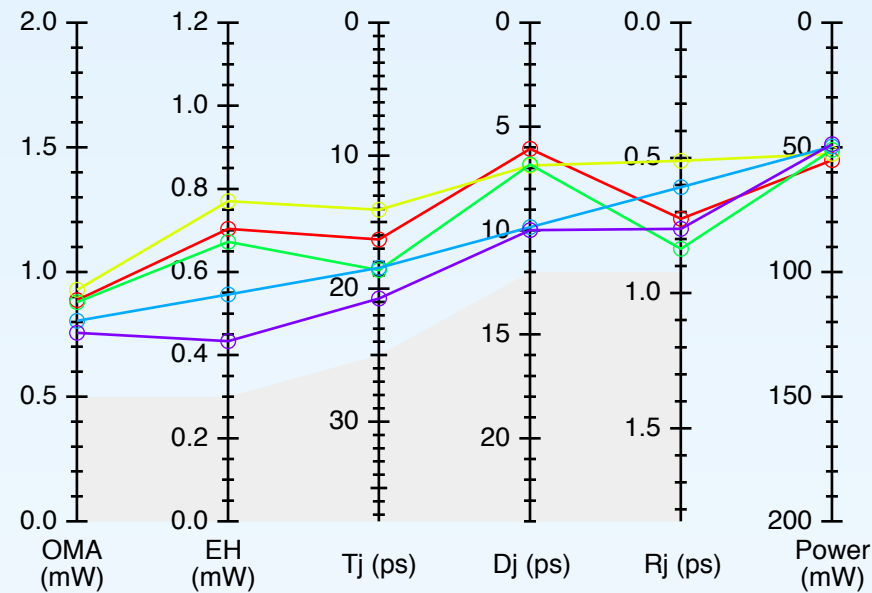
# Commercial Modules with LDQ10

- LDQ10 integrated into commercial packages with multiple vendors
  - Used to explore setting parameter space to optimise performance

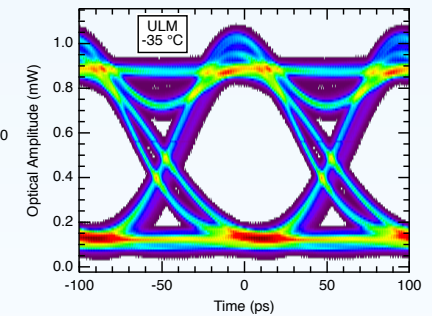
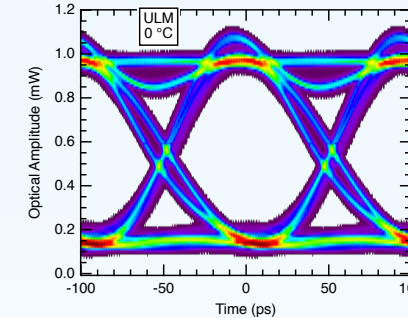
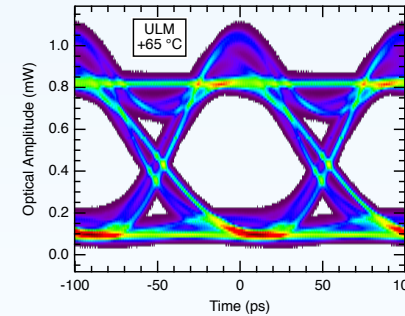
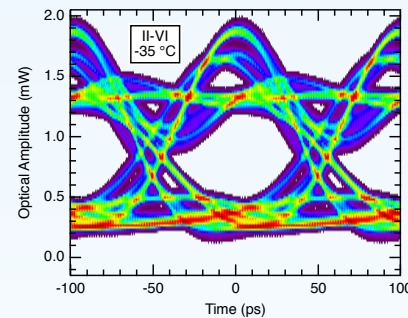
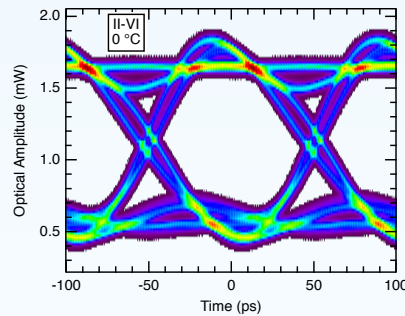
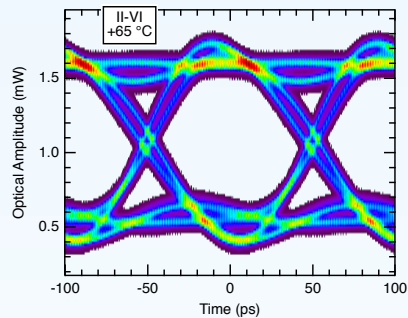
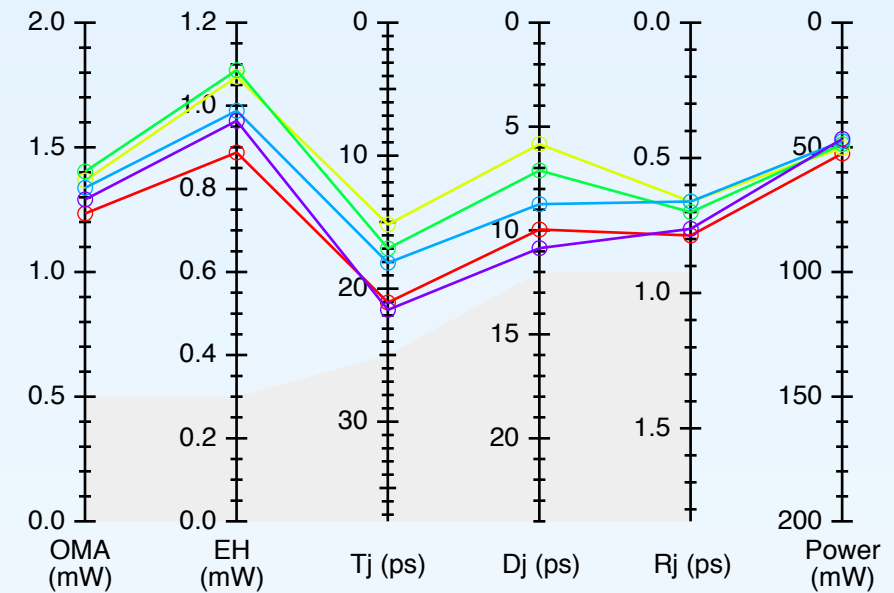


# Performance over temperature

VCSEL A

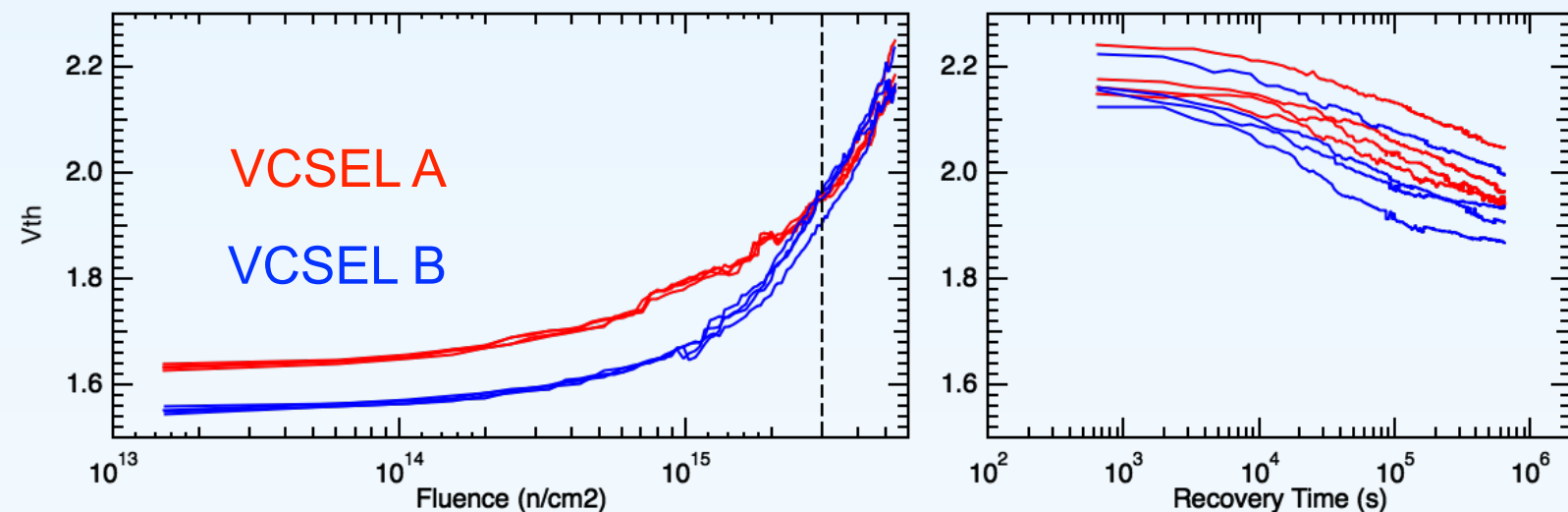
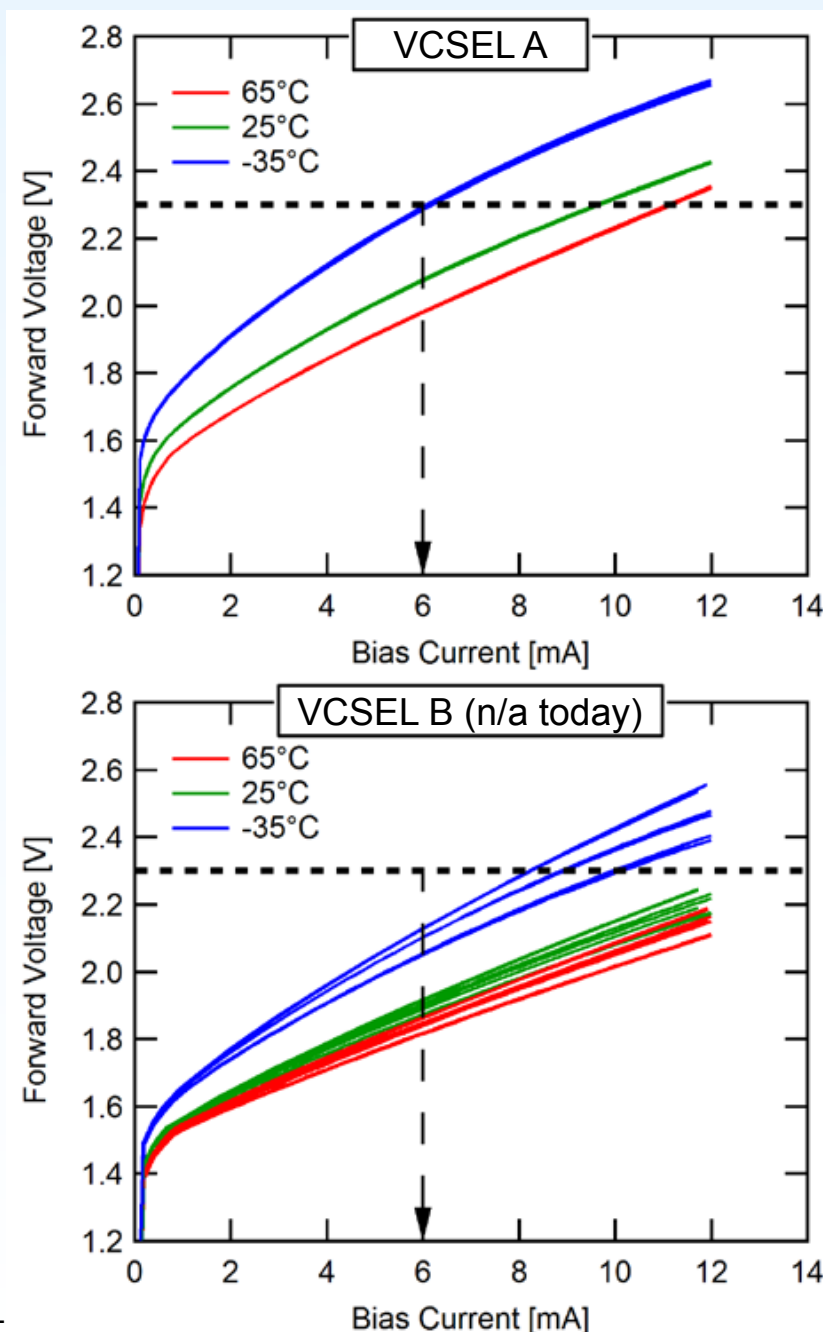


VCSEL B



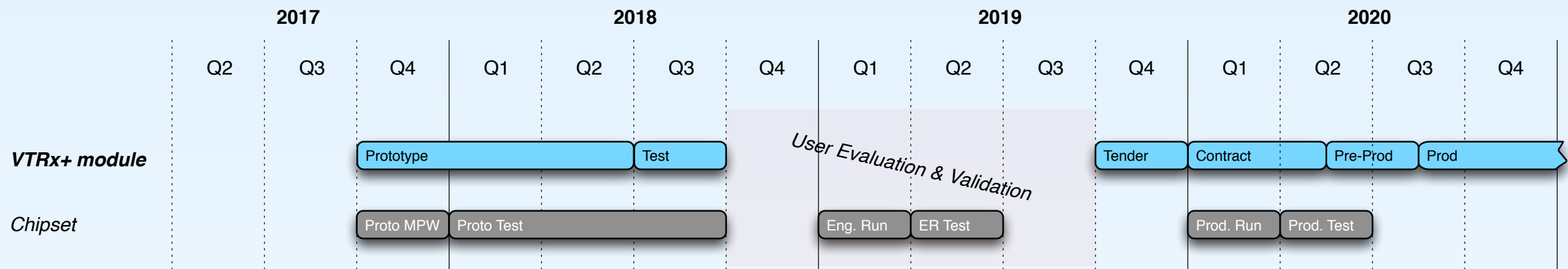
- Measured performance over full temperature range
- Either candidate VCSEL may work
- Power Consumption similar

- Largest unique challenge comes from ensuring sufficient voltage headroom for operation of VCSELs with 65 nm CMOS driver that limits voltage rail to 2.5 V



- Going cold and irradiating the VCSEL make the situation worse
  - VCSEL forward voltage increases
- Need some voltage headroom for the driver's output transistor
- Currently validating the margin we have for operation

# Schedule overview



- Expecting answers to Price Enquiry for development in next two weeks
  - Development slated for 9 months from order placement
- Will then have several possible designs in hand in sufficient quantity for evaluation by user community
- Tendering for volume production will take place during 2019
  - Final module format only known after tendering
- Coupled with IpGBT project for chipset production



- Versatile Link + project developing Rad-tolerant link for deployment in HL-LHC experiments
  - Operating at 5 or 10 Gb/s Tx and 2.5 Gb/s Rx to match IpGBT
  - Rad tolerant to Tracker levels
- Front-end module development based on
  - In-house design
  - Minimal customisation of commercial module
- Good results achieved with current prototypes
  - Both in-house and commercial designs
  - Understanding of system margins over temperature and after irradiation ongoing
- Challenging to meet smallest height requirement
  - Special development will be required