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Serial Powering Optimization for CMS and ATLAS Pixel Detectors within RD53 Collaboration for HL-LHC: System Level Simulations and Testing

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Serial powering is the baseline choice for low mass power distribution for the CMS and ATLAS HL-LHC pixel detectors. For this scheme, two 2.0A Shunt-LDO (SLDO) regulators are integrated in the RD53 prototype chip (65 nm) and are used to provide constant supply voltages to its power domains from a constant input current. System level simulation studies will be presented, in which a detailed regulator design in serially powered topology is used to evaluate and optimize system parameters for different operational scenarios of HL-LHC pixel detectors. Performance results from testing prototype SLDO chips will be shown, including x-ray irradiation.

Summary

Serial powering has been identified as the baseline low mass choice for powering the CMS and ATLAS pixel detectors in the HL-LHC era. The very large number of pixels, the high hit and trigger rates required designing a new chip in 65 nm CMOS technology within RD53 collaboration. Such a chip would require current levels of ~2.0 A under normal operating conditions. In a serially powered topology, pixel detector modules would be serially powered and each of those would be composed of up to four chips powered in parallel. Consequently, each current chain could require up to 8.0 A, including extra headroom to comply with fast dynamic current variations of the digital logic of the chip.

A serial powering scheme, based on a constant current supply, is possible by integrating an on-chip shunt-LDO regulator (SLDO) for each of the power domains of the chip (analog and digital). The SLDO concept, firstly introduced in FE-I4 chips (130 nm), combines a Low Drop-out (LDO) regulator with a shunt. Therefore, any excess of current injected in the serial power chain can be shunted, while the linear regulator part of the SLDOs provides independently the required voltage to the analog and digital power domains of the chip.

The SLDO has been redesigned in 65 nm and it is able to carry up to 2.0 A. The resistive behavior of the SLDO allows for the operation of multiple SLDOs in parallel, with well-defined current sharing, determined by their effective resistance, which is configurable. Another important novel SLDO feature is a configurable voltage, which allows an optimization of the power consumption in case of a failure of a chip in a module.

System simulations for a serial power system for the configuration of the CMS pixel detector have been used to study the performance of the SLDO under various operating conditions.
The simulation was based on the SLDO 2.0A regulator detailed design, with serially powered pixel modules, each consisted of either two or four pixel chips powered in parallel. The dynamic profiling of both digital and analog power, failures and power up scenarios have been simulated to understand and optimize the parameters for stable operation of a serially powered system. The coupling of digital noise to the analog domain and vice versa has also been evaluated to be within the acceptable levels and the amount of extra shunt current needed for reliable, yet efficient, operation of the front-ends chips has been optimized.

In addition, a 2.0A SLDO prototype chip has been tested in serially powered mode, where its characteristics have been investigated e.g. the effective resistance, the use of the configurable voltage and the coupling of the noise of chips operated in parallel and in series. Finally, Xray irradiation of the test-chips demonstrated radiation hardness of up to 500 Mrad without significant impact on their performance.

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