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A 2.5V Step-Down DC-DC Converter for Two-Stages Power Distribution Systems

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A prototype second-stage buck DC-DC converter has been designed in 130nm CMOS and fully characterized. This circuit provides up to 3A at an adjustable output voltage of 0.6-1.5V from an intermediate bus voltage of 2.5V. Hardness by design techniques have been systematically used, and the prototype successfully passed TID irradiation up to more than 200Mrad and Single Event Effects tests with a heavy ion beam. Safe integration on-board requires an optimized PCB design and bump-bonding assembly to reduce parasitic inductances along the input current path. An alternative quasi-resonant topology enabling significant reduction of the inductor size is also described.

Summary

Some detector systems for upgraded LHC experiments require the distribution of different voltage supply levels on the same compact module. The use of two-stages step-down conversion is a convenient and efficient way of doing that. The first conversion stage provides a regulated intermediate bus voltage of 2.5V that can be used on module to power opto-electronics components. This converter, powered via a single 12V line by off-detector supplies, is a modified version of an already qualified circuit (upFEAST2) widely used in LHC detector upgrades. In this work we present the development of a second-stage Point-Of-Load (POL) converter, radiation and magnetic field tolerant, and providing up to 3A at 0.6-1.5V to the load from the intermediate bus voltage.

The first prototype converter circuit for this application uses a simple buck topology and has been designed in the mainstream 130nm CMOS technology supported within the CERN Foundry Services. The I/O 2.5V transistors available in this technology have been used in the design of the power portion of the circuit, while all the control benefits from the better performance and radiation tolerance of the core 130nm transistors. One of the main difficulties to overcome originates from the large switching input currents inherent to the functionality of a buck converter: parasitic inductances along the input current path generate large voltage transients at high frequency that challenge the reliability of the device. This has been addressed in the design with reduced slew rates in the commutation of the power transistors. In an effort to reduce the parasitic inductance the circuit is bump-bonded to a PCB whose design has been optimized with the help of ANSYS SIwave, a specialized design platform for power integrity. On-chip voltage transients have been measured on the prototype with a dedicated on-chip track-and-hold circuit, and agree with expectations.

Total Ionizing Dose (TID) tolerance has been achieved with the systematic use of Enclosed Layout Transistors (ELT) and guardrings, and relying on the natural radiation tolerance of the thin gate oxides. Provisions to protect the circuit from Single Event Effects (SEE) include over-sized logic gates, triplication, and the use of a novel Pulse-Width-Modulation generator circuit capable of fast recovery from a possible particle hit. These built-in properties have been confirmed with irradiation at an X-ray system up to more than 200Mrad (TID) and at a heavy ion accelerator (SEEs).

The first prototype converter switches at frequencies between 4 and 8MHz using inductors of 47 to 100 nH. Its efficiency, strongly determined by the working conditions, is in the range of 85-89% for an output voltage of 1.2V and 81-86% for 1V. Full electrical characterization shows that most of the integrated functions perform correctly, while highlights some issues that are addressed in a second prototype that will be manufactured over

the summer. We are also developing an alternative design based on a quasi-resonant topology that promises to yield higher efficiency while drastically reducing the inductor size to 10-20nH, allowing for a considerable mass and size reduction very attractive for tracker detectors.

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