Contribution ID: **56** Type: **Oral**

ATLAS ITk Short-Strip Stave Prototypes with 130nm Chipset

Wednesday, 13 September 2017 08:30 (25 minutes)

The ATLAS ITk is working to deliver a new Inner Tracking detector for use at HL-LHC. The strip tracker community has recently constructed partially loaded, double sided demonstrator staves using the HCC / ABC130 chipset in 130nm CMOS technology. Mindful of the need to maximise power efficiency whilst minimising the cost and material of associated cable plant, the system design includes the integration of a low-mass DC-DC converter and sensor bias (HV) switch within each module. This paper documents the first results from the demonstrator staves. The system concept and the roadmap toward a full system test are also outlined.

Summary

The ATLAS ITk is working to deliver a new Inner Tracking detector for use at HL-LHC. The strip tracker, comprising a series of concentric barrels with endcaps formed of petals, applies a common system architecture to the two geometrically different regions.

Each stave or petal comprises a support structure made of carbon fibre and foam, into which a cooling pipe has been integrated. Polyimide flex circuits known as ''bus tapes" are co-cured upon them to route electrical services between the End of Substructure (EoS) card, which provides the interface to the off-detector systems, and the detector modules. In order to maximise power efficiency and to minimise the cost and material of associated cable plant, each stave or petal side has a common low voltage power bus at 11V. As such, low mass DC-DC converters form an integral part of the strip module design: these are used to deliver the 1.5V needed to power the front end chipset.

The detailed module design and standalone performance is presented elsewhere in this conference. This paper documents the first results from the demonstrator staves. This year our community has constructed partially loaded, double sided demonstrator staves using the HCC / ABC130 chipset in 130nm CMOS technology. The system architecture of these staves differs slightly from that proposed for production units with the ABCstar/ HCCstar chipset in the same technology, but is sufficiently representative so as to make this an important test. Key differences include the use of EoS cards which connect to the DAQ hardware by means of parallel electrical links provide a buffered, parallel connection instead of the lpGBT chips to be used in the experiment, and the use of early bus tape designs with a common multi-drop bus to supply Trigger, Timing and Control (TTC) signals to the 13 short strip modules on each side. Signal propagation tests with these tapes had noted a marked deterioration of TTC quality when more than 4 modules are loaded, so these early demonstrators shall not be fully loaded. The design was shown to work very well and results shall be presented.

The next generation of staves will use segmented TTC links to deliver high quality signals to 14 modules, hence they may be fully loaded, and their EoS cards will use the GBTx chip in order to facilitate optical readout of the modules. The way forward to a system test using such staves shall be outlined.

Primary authors: PHILLIPS, Peter (STFC - Rutherford Appleton Lab. (GB)); SAWYER, Craig Anthony (STFC - Rutherford Appleton Lab. (GB)); DOPKE, Jens (STFC - Rutherford Appleton Lab. (GB))

Presenter: PHILLIPS, Peter (STFC - Rutherford Appleton Lab. (GB))

Session Classification: Production, Testing and Reliability

Track Classification: Production, Testing and Reliability