A compact size, 64-channel, 80 MSPS, 14-bit dynamic range ADC module for the PANDA Electromagnetic Calorimeter

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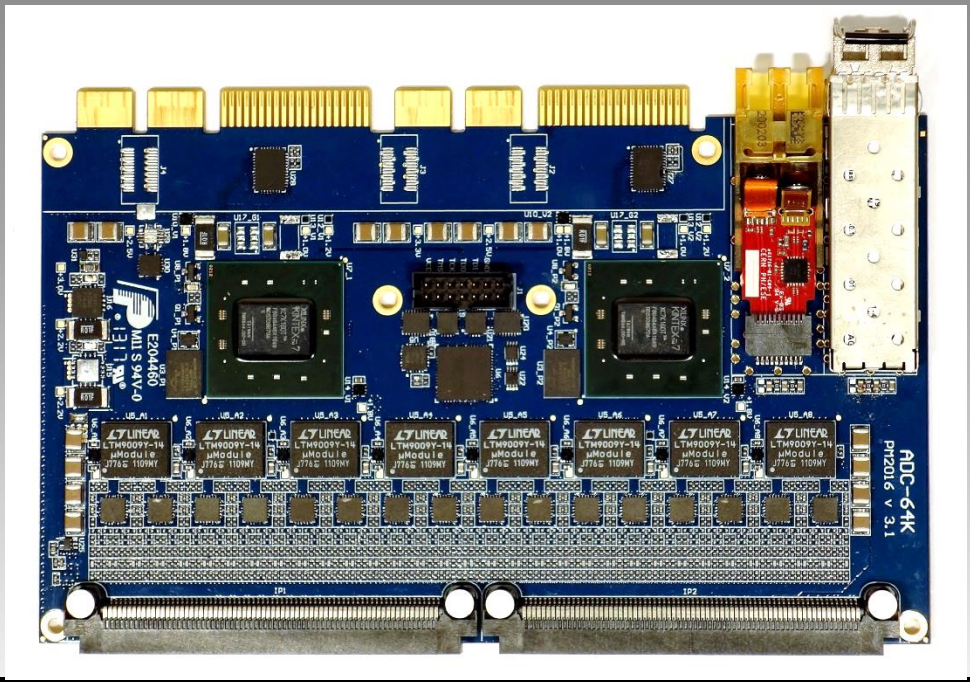
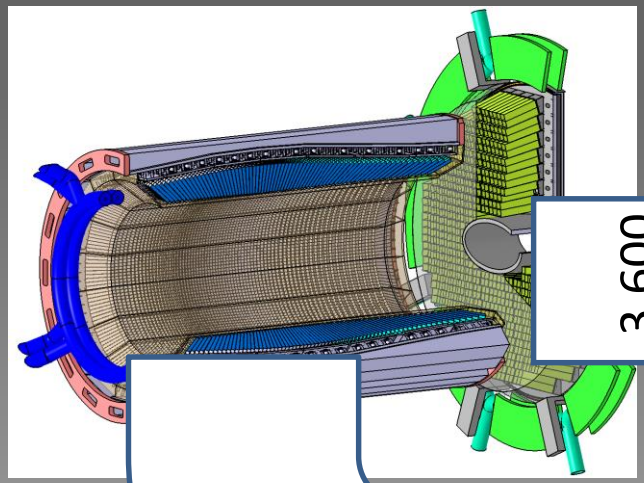
M. F. Preston, K. Makonyi, Per-Erik Tegner, Stockholm University, Sweden
P. Schakel, M. Kavatsyuk, KVI Groningen, The Netherlands
J. Müllers, University Bonn, Germany
M. Albrecht, Ruhr University Bochum, Germany



ADC for EMC

- PANDA EMC Readout System



3,600

11,952

Photosensor VPTT

Preamplifier Basel

Photosensor APD

Preamplifier APFEL (GSI)

14400

47808

225 ADC 64-ch

375 ADC 128ch

225

125

22 Data Concentrator, 16-ch

22

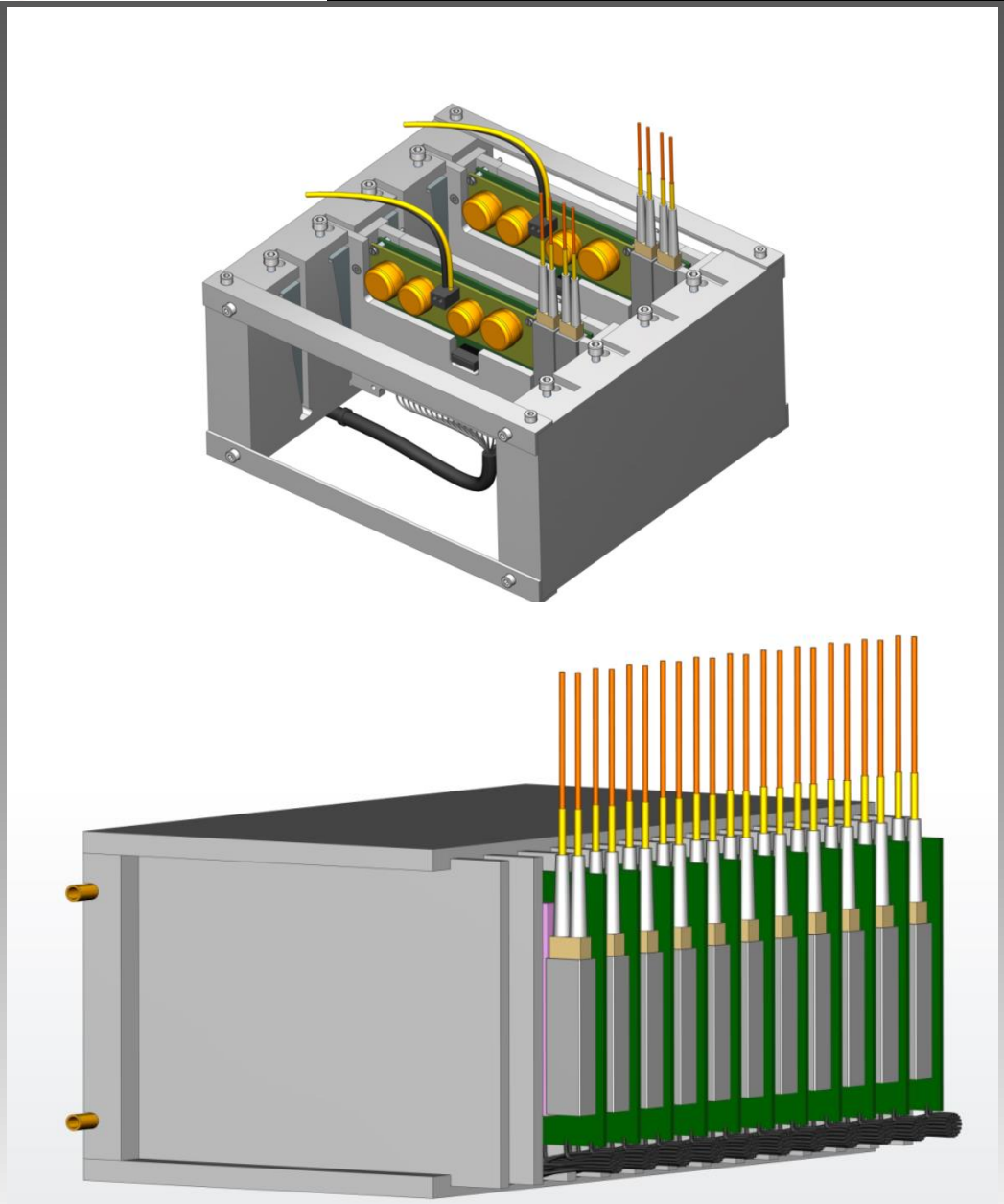
Compute Node

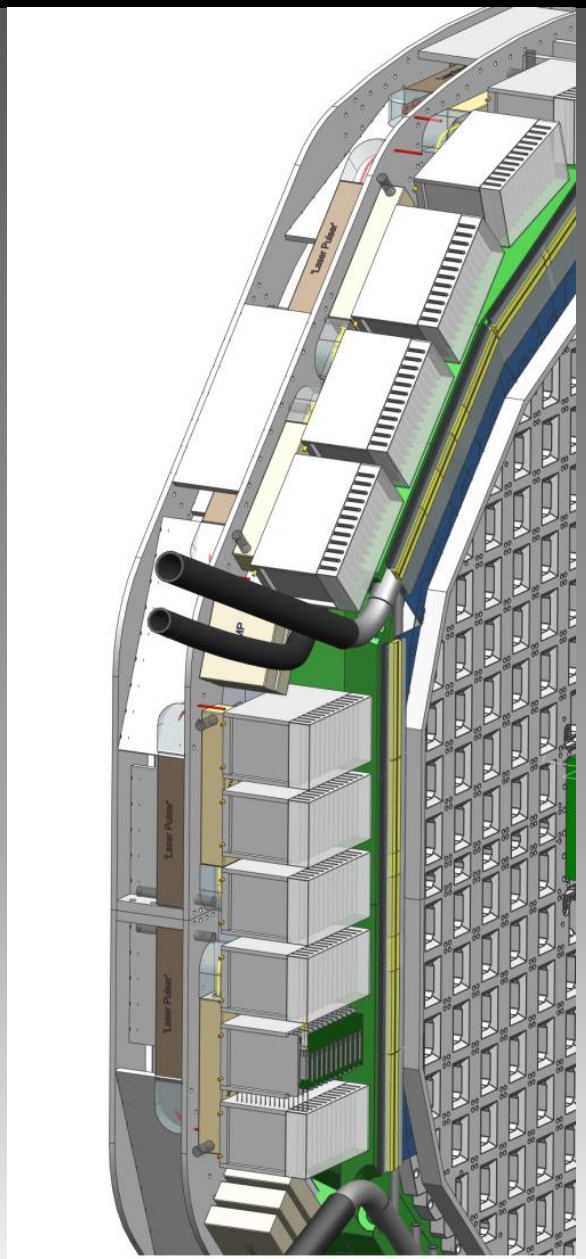
- **15000 channels**
- **Dual photosensor readout**
- **Dual range**

- **High channel density**

ADC for EMC-Endcap

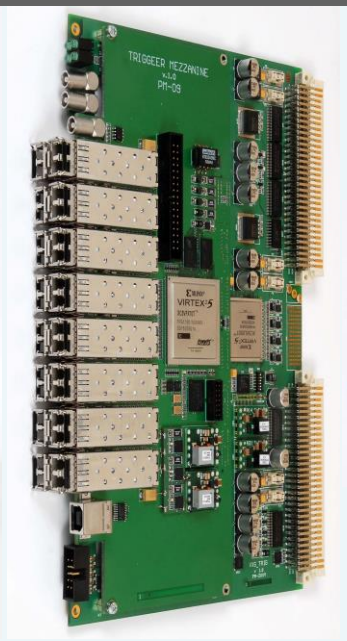
- Encapsulation and Cooling





ADC for EMC

- SADC development for PANDA



2008
16-ch, 12-bit
160 MSPS ADC
Used for the first tests, sold to WIENER

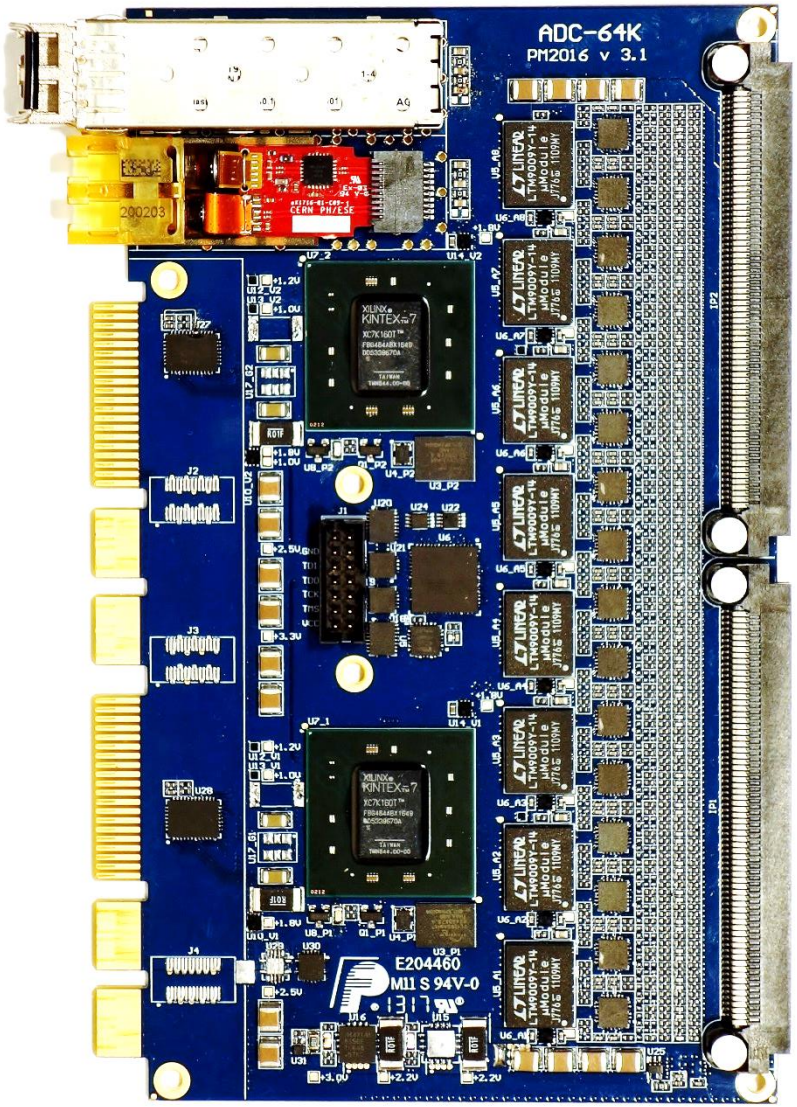
2010
16-ch, 2GBit/s
Optical Data Concentrator
Used in many experiments including WASA, KLOE2

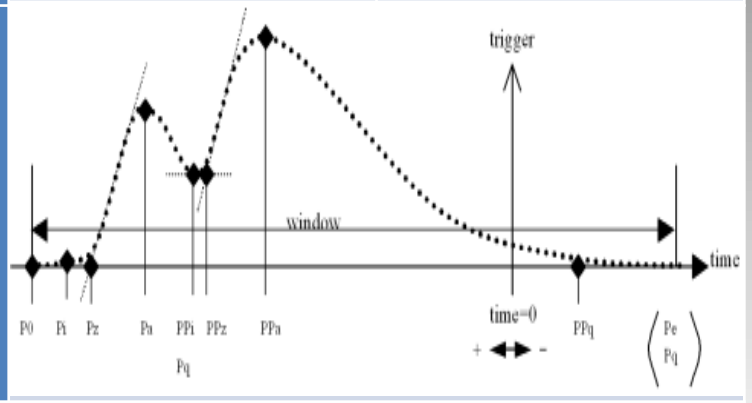
2011
16-ch, 14-bit
125 MSPS ADC
Virtex-5
Used for evaluation of DSP algorithms

2012
32-ch, Dual-range, 14-bit
80 MSPS ADC
Virtex-6
Used for first data taking and durability tests

2013
64-ch, 14-bit
80 MSPS ADC
Kintex-7
Close-to-final prototype

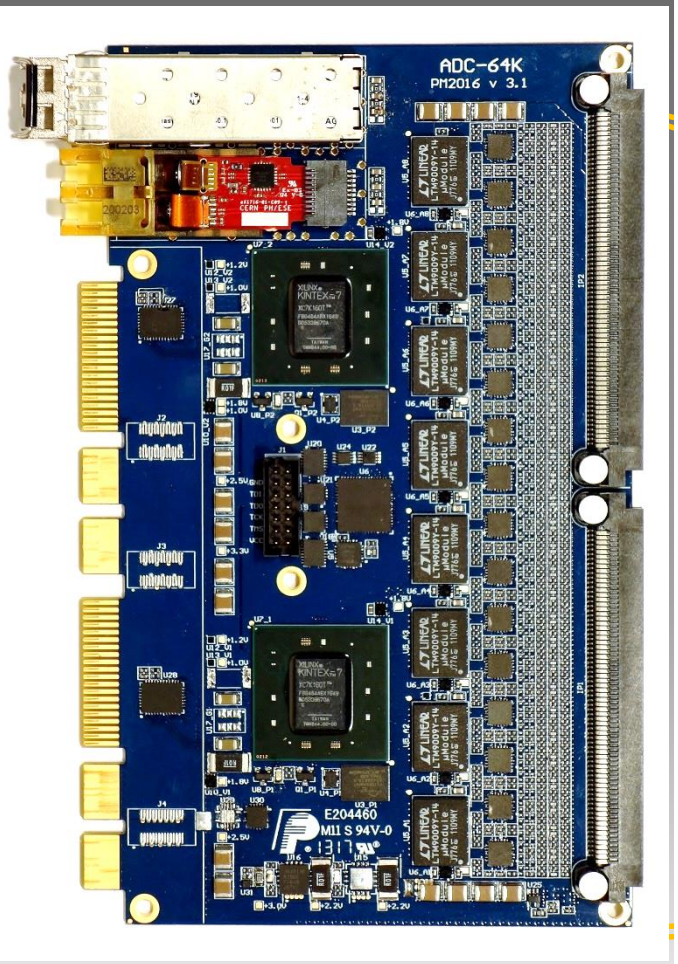
ADC for EMC
- ADC_64K



ADC Model	ADC_64K EMC-FE	ADC_64K SHASHLYK
No. of channels	32 (64)	64
Sampling rate	80 MSPS	125 MSPS
Input coupling	AC, DC, positive, negative, diff	
Resolution ENOB	14-bit (dual range)	11.5-bit
Input Connector	Samtec	
Baseline	0V	
Input range (dual)	±2.2V, ±140 mV	±1.0V
Noise (rms)	100uV	
Data retention/ch.	25us	
Input filter	Active-filter/Amplifier	
Interface	Optical, SFP, LC-type, 2 Gbit/s	
Power	18W	21W
Feature extraction:		

ADC for EMC-Endcap
– Design idea

SADC Prototype

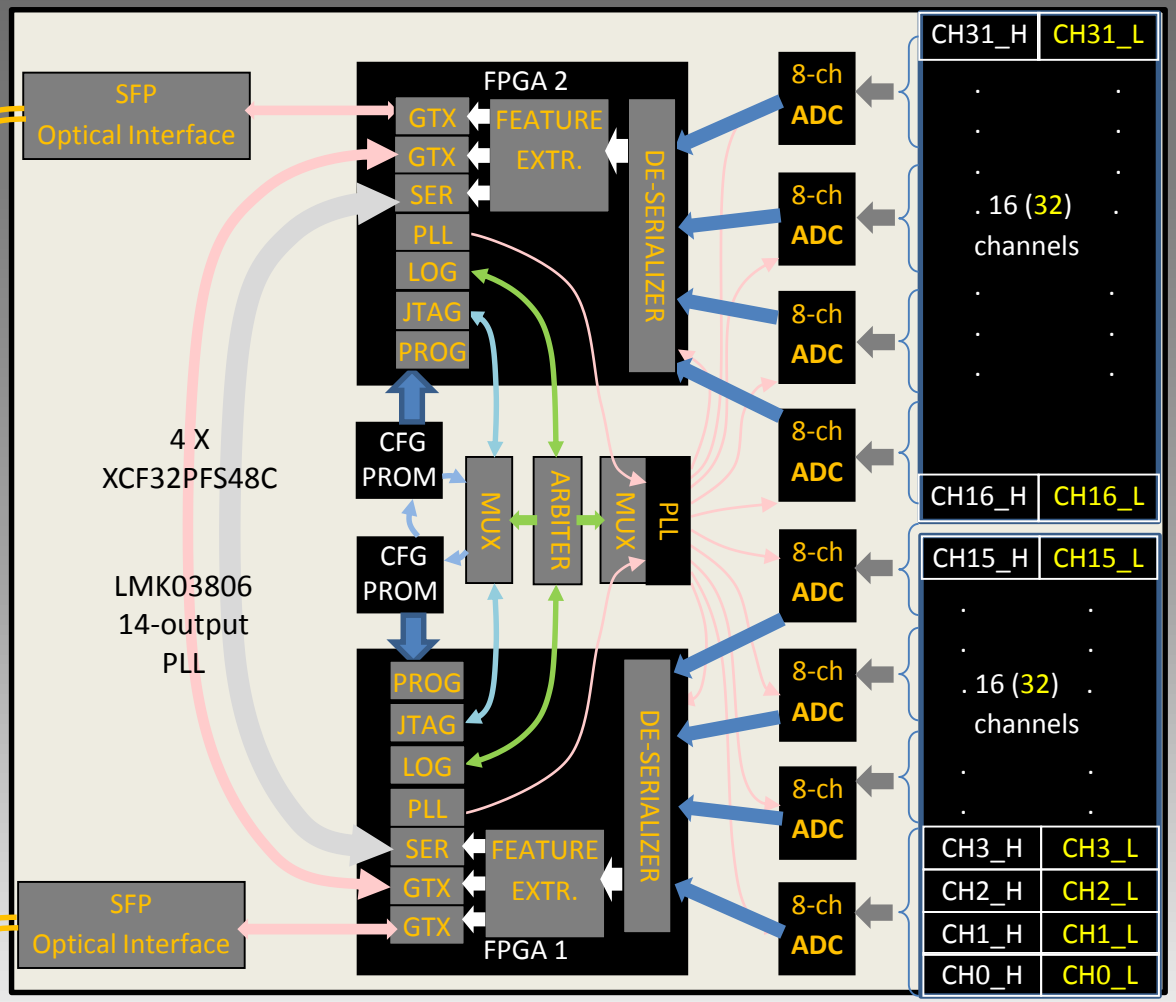


2 X
Finisar
2.1 Gbit/s

2 X
XC6VLX130T-
3FFG484C

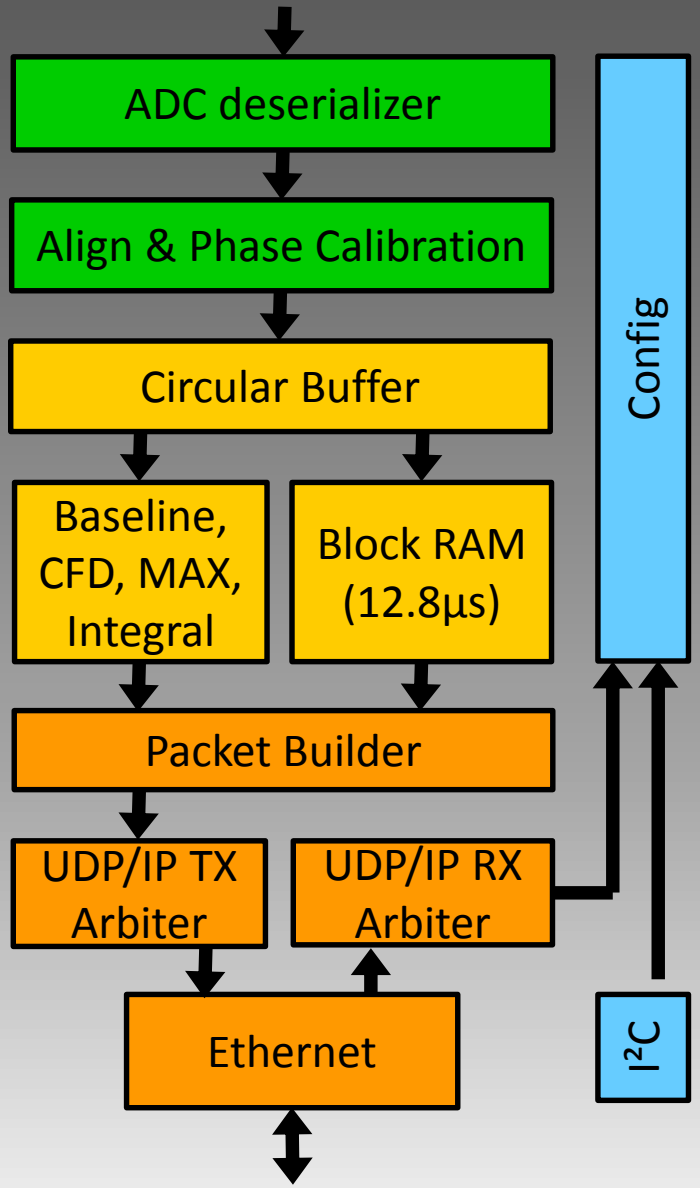
8 X
LTM9009-14
14-Bit, 80-Msps
Low Power
Octal ADCs

64 X
ADA4940-2
Low Power
diff op-amp



ADC for EMC-Endcap

- Test Firmware



Written for Crystal Barrel @ ELSA (Bonn) by Johannes Müllers

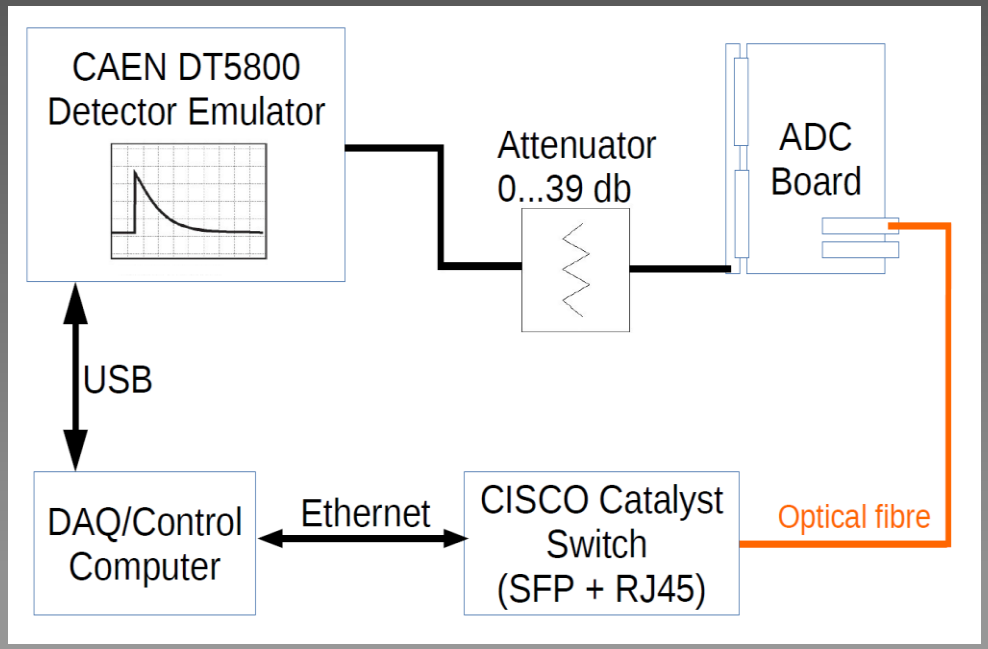
Partly based on firmware written by Pawel Marciniewski

- ADC-interface,
- PLL control,
- Noise filter,
- Baseline,
- Pulse amplitude,
- Pulse integral
- CFD discrimination
- Triggering

- **1G/2.5G Ethernet PCS/PMA** (free, Xilinx IP)
- **Tri Mode Ethernet MAC** (commercial, Xilinx IP)
- **1G eth UDP/IP stack** (free, OpenCores)

ADC for EMC-Endcap

- ADC performance tests

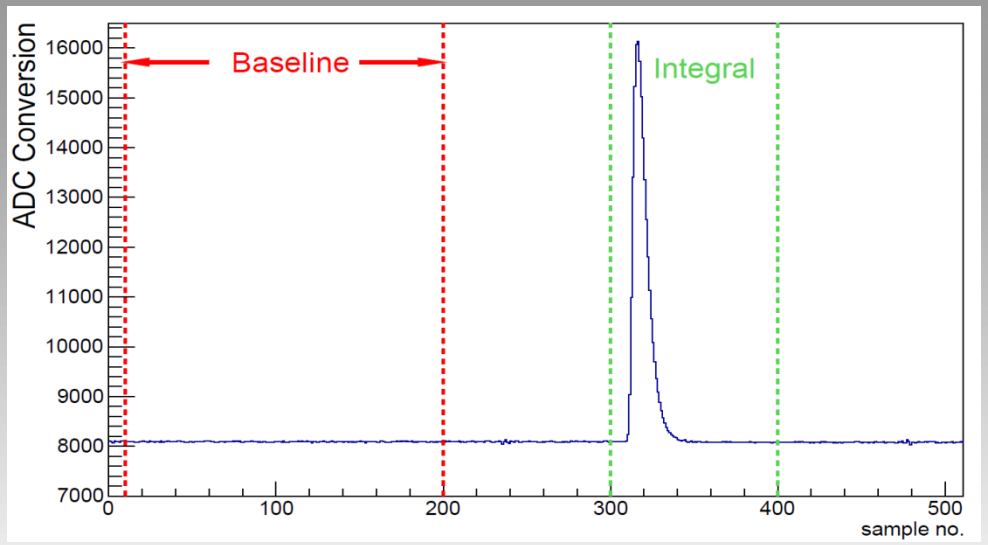


Performed at Ruhr Universität Bochum

Malte Albrecht

(Tests proposed by Pawel Marciniewski)

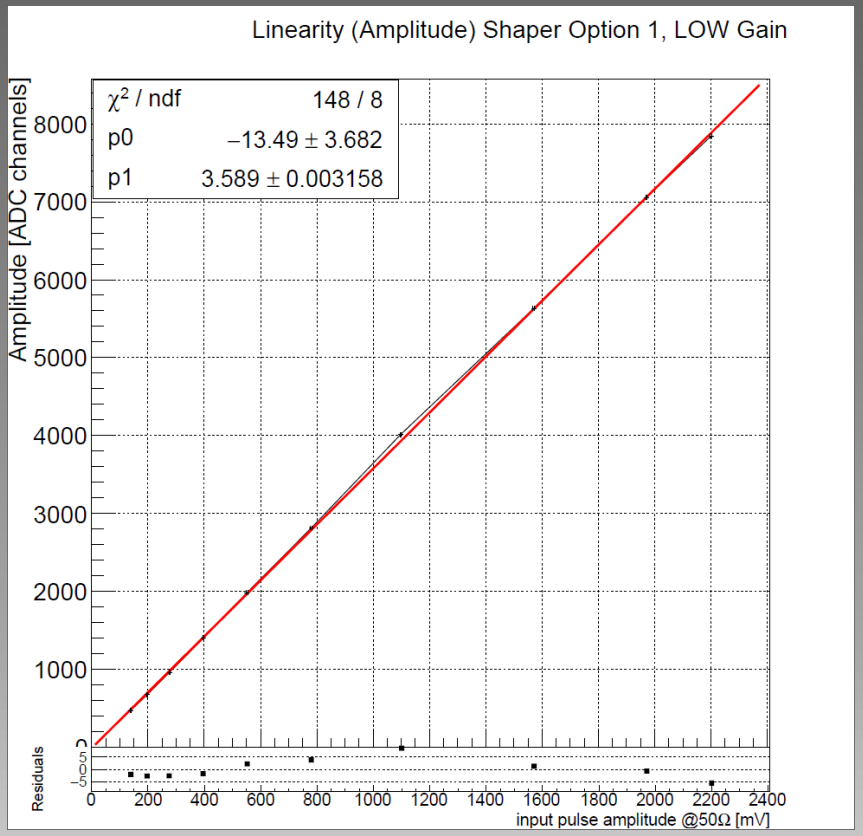
- ”Bonn” firmware
- CAEN DT5800 programmable pulse generator
- Ethernet switch

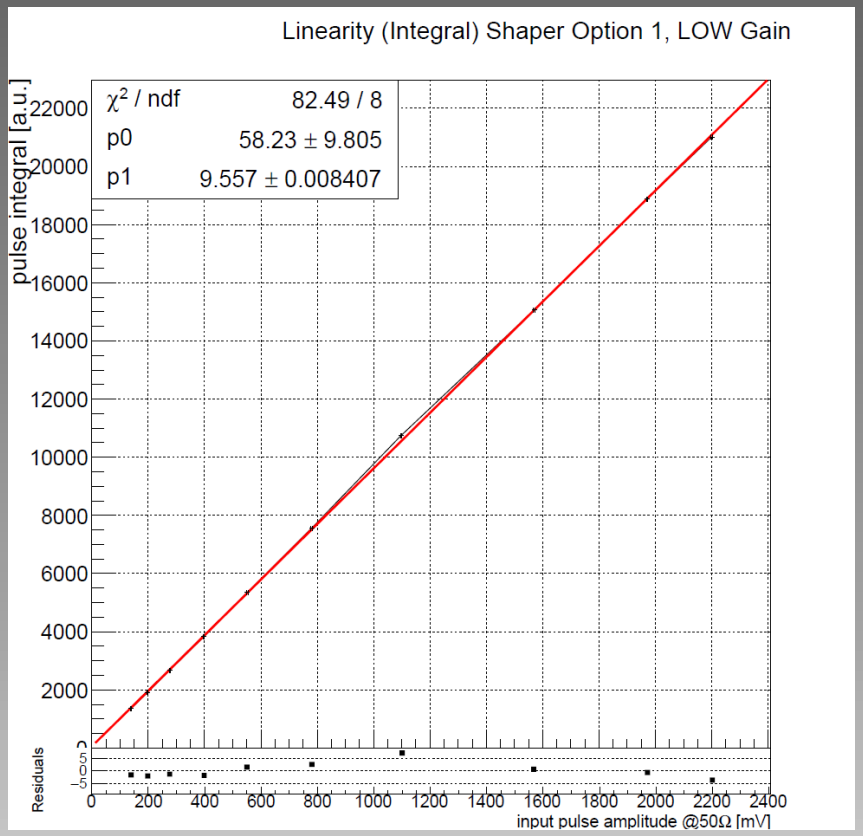


- **Noise**
- **Pulse response/bandwidth**
- **Linearity (Amplitude and Integral)**
- **Resolution**
- **Pile-up resolution (pending)**

ADC for EMC-Endcap

- Linearity

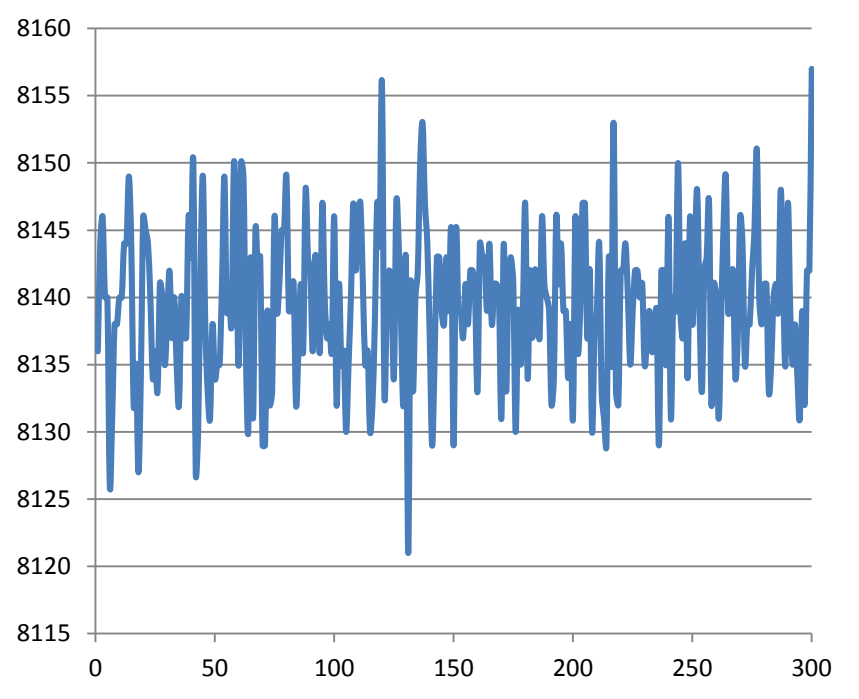


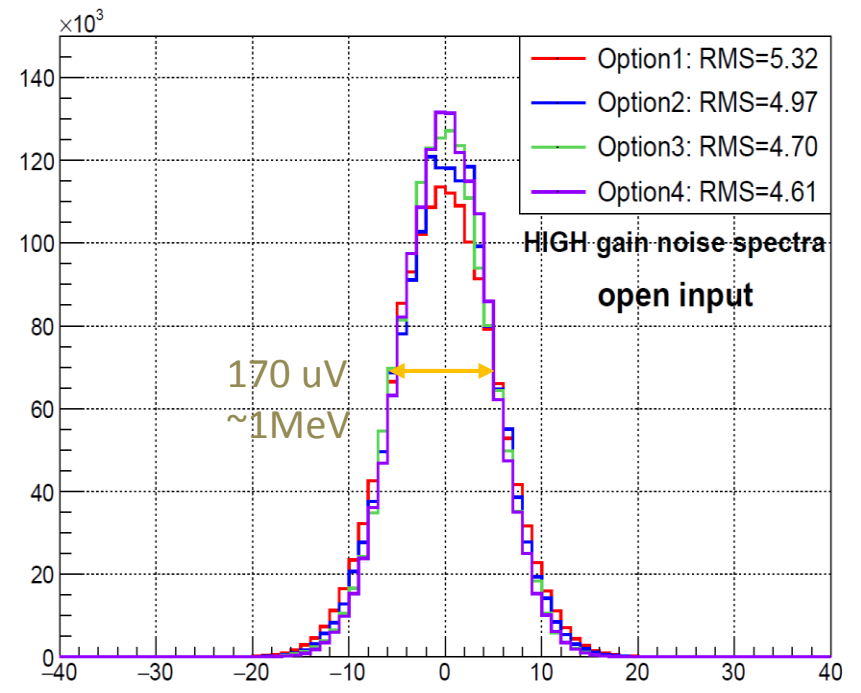


ADC for EMC-Endcap

- Noise

High gain range (-140..+140 mV)

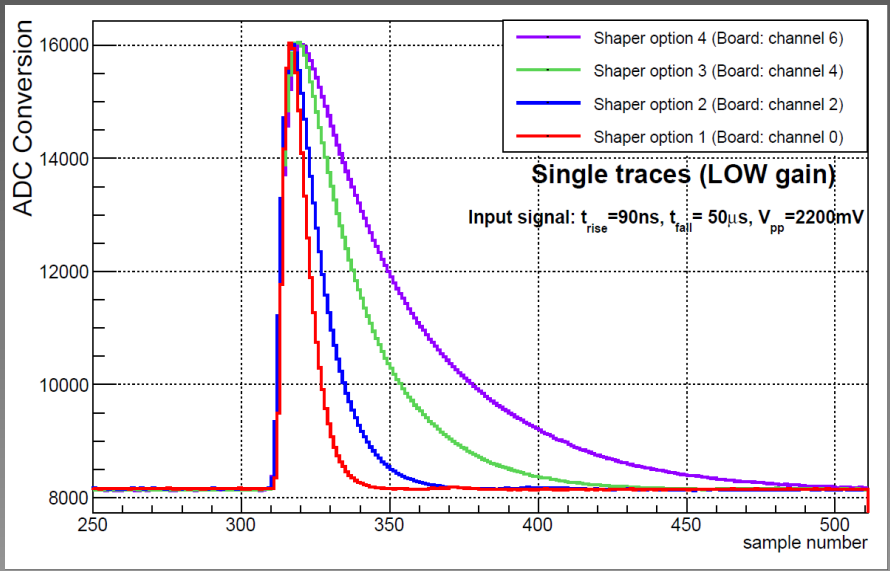


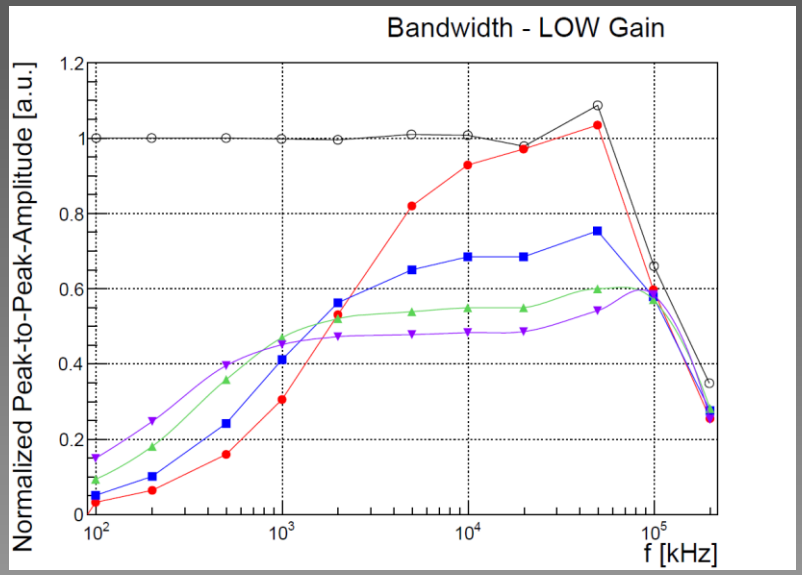


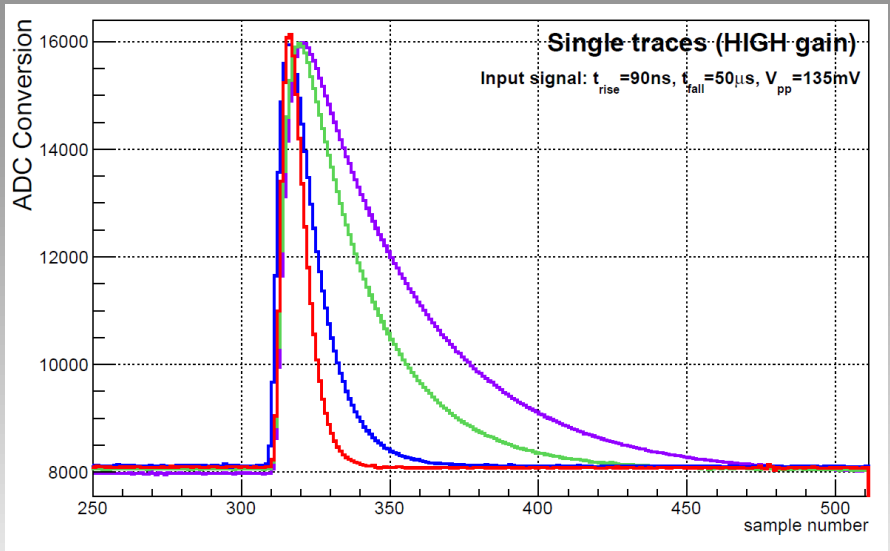
Taking the energy conversion coefficient and the overall gain of the system into account, the noise of 170 uV corresponds to 1 MeV, which fulfills the basic requirement of the experiment.

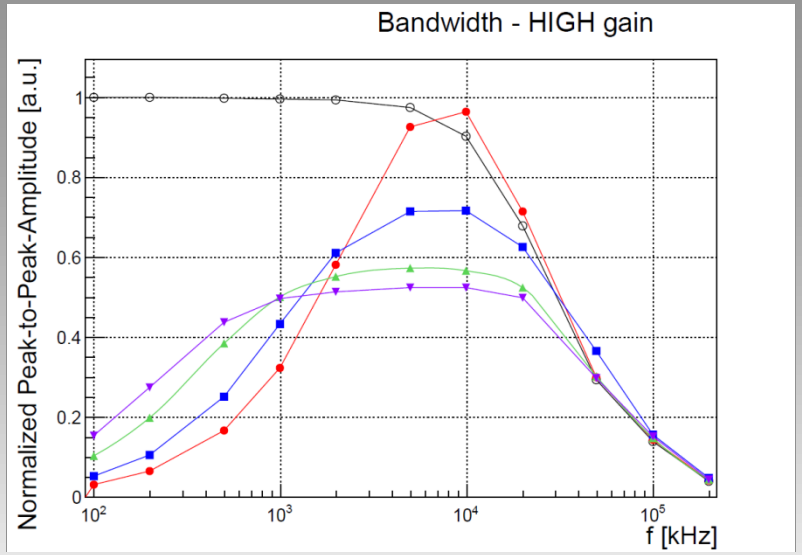
ADC for EMC-Endcap

- Signal shaping



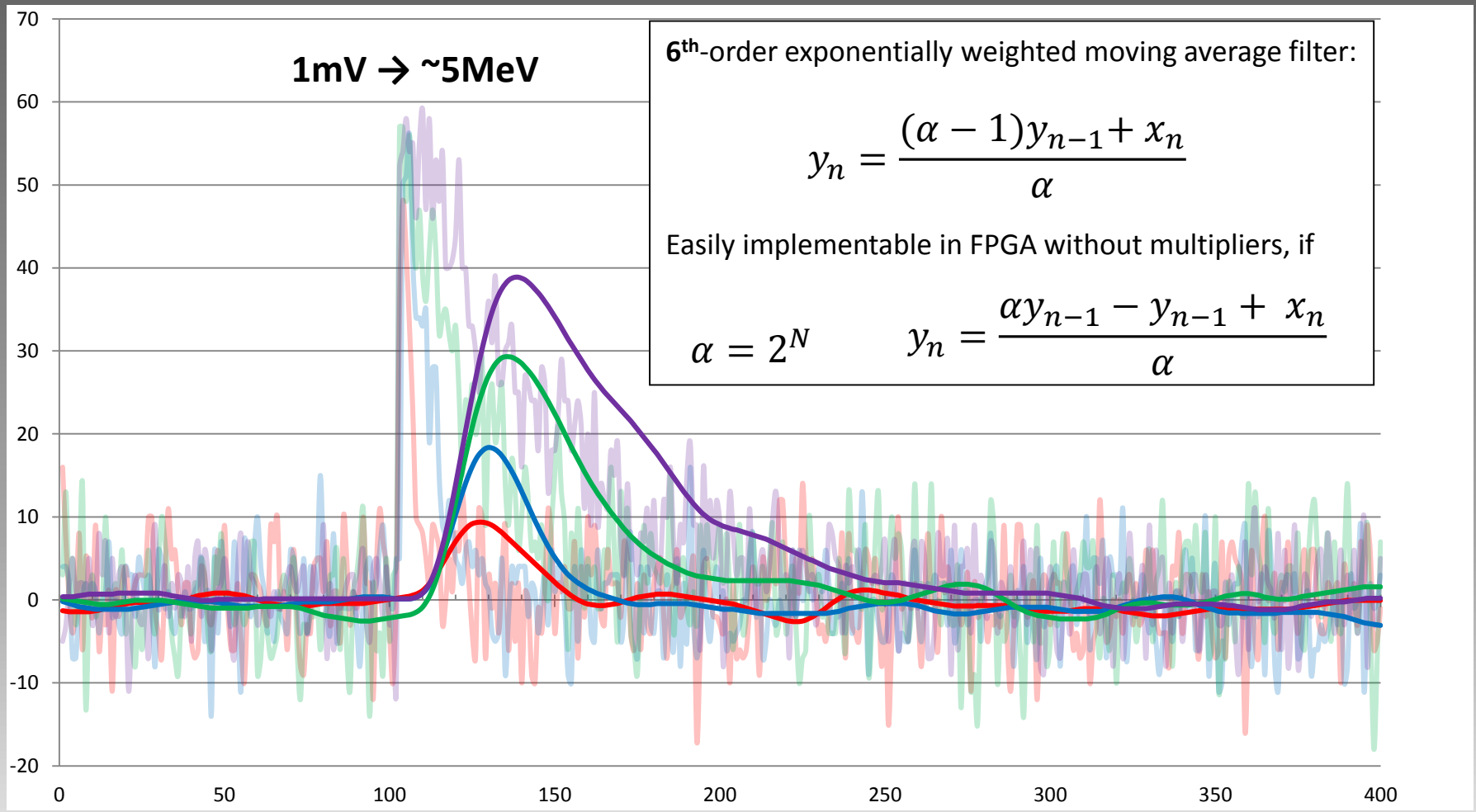






ADC for EMC-Endcap

- Signal shaping



6th-order exponentially weighted moving average filter:

$$y_n = \frac{(\alpha - 1)y_{n-1} + x_n}{\alpha}$$

Easily implementable in FPGA without multipliers, if

$$\alpha = 2^N \qquad y_n = \frac{\alpha y_{n-1} - y_{n-1} + x_n}{\alpha}$$

ADC for EMC-Endcap

- Signal tail reconstruction

Exponential decay

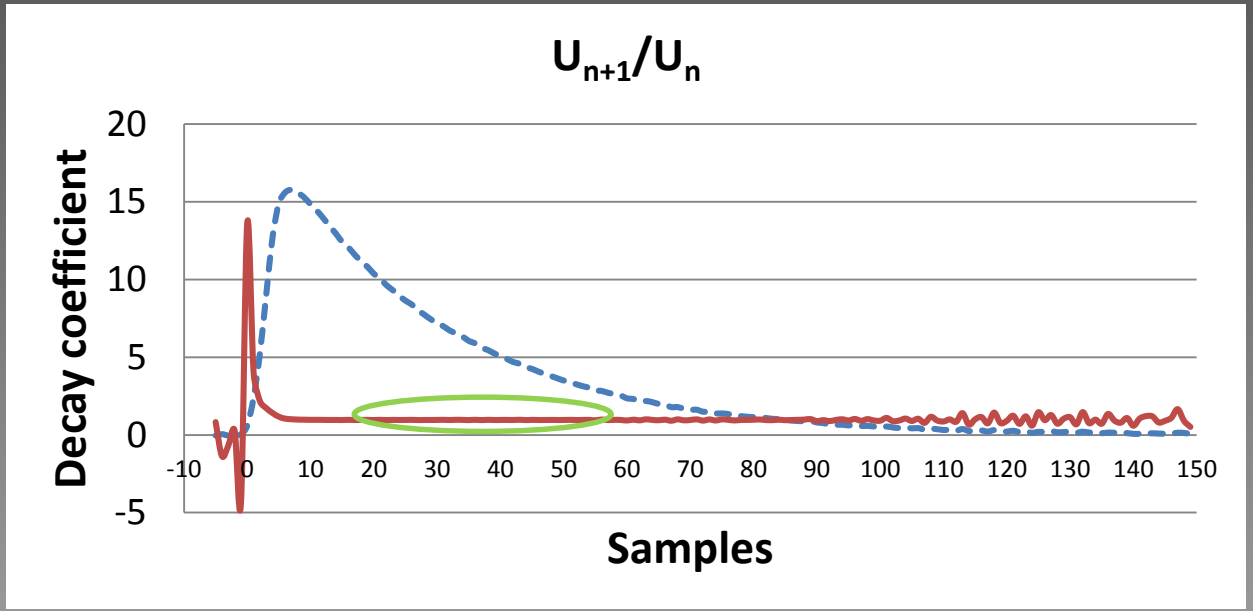
$$U_n = Ae^{-\frac{n}{\tau}}$$

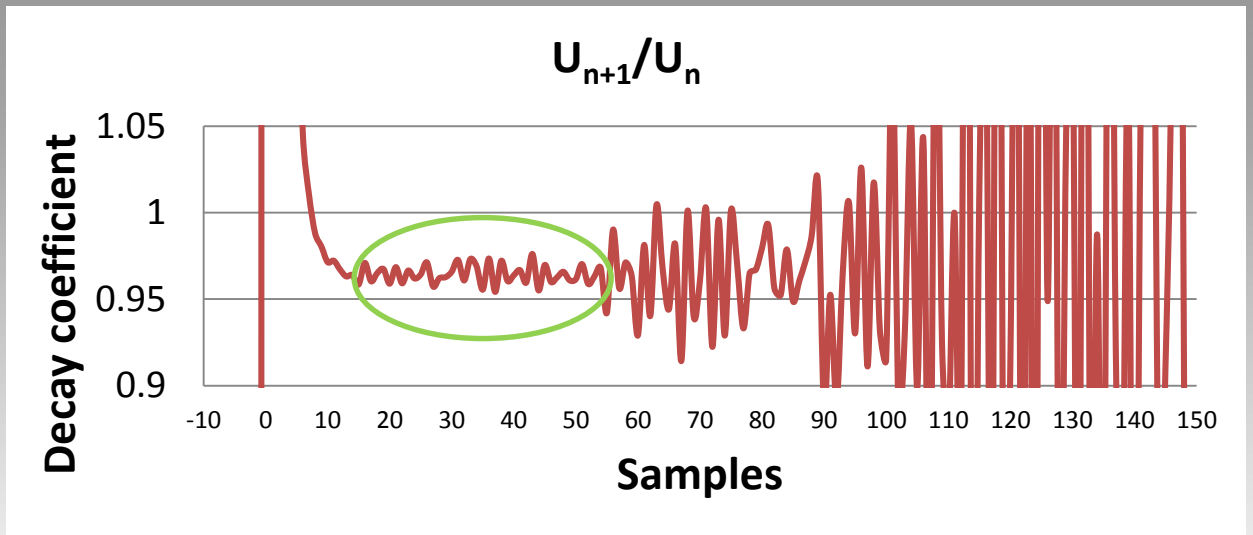
$$U_{n+1} = Ae^{-\frac{n+1}{\tau}}$$

$$\frac{U_{n+1}}{U_n} = e^{-\frac{1}{\tau}}$$

Decay coefficient

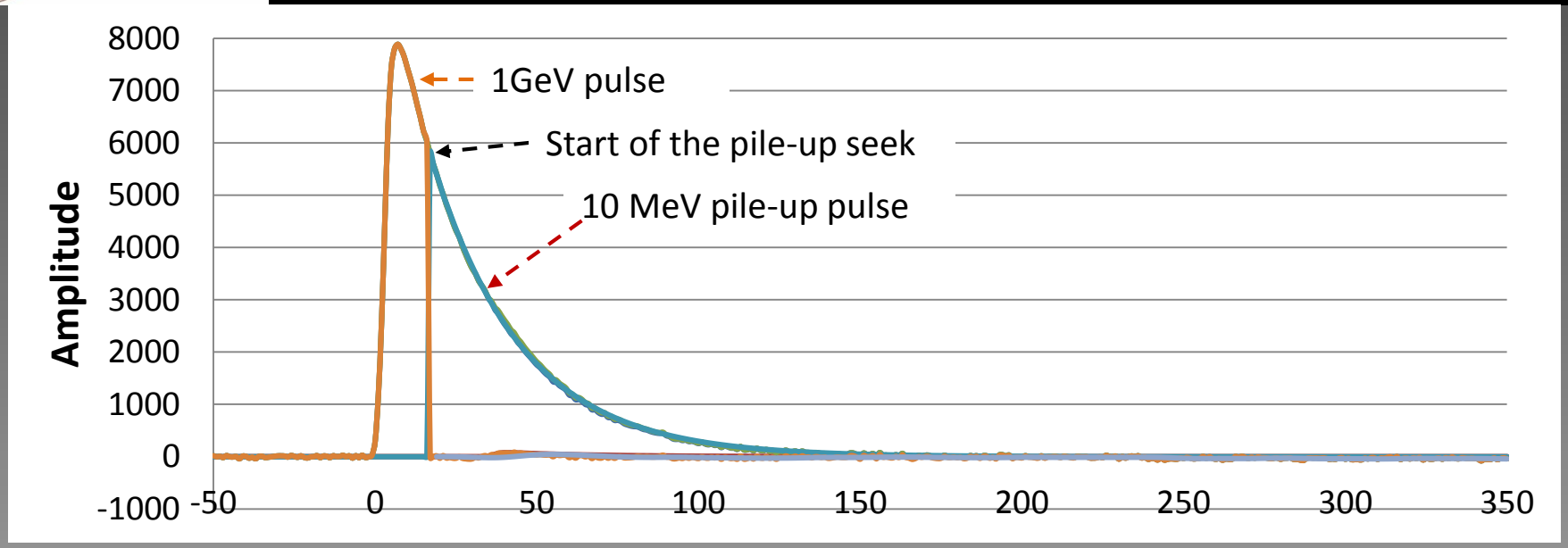
$$\frac{U_{n+1}}{U_n} = 0{,}96478$$

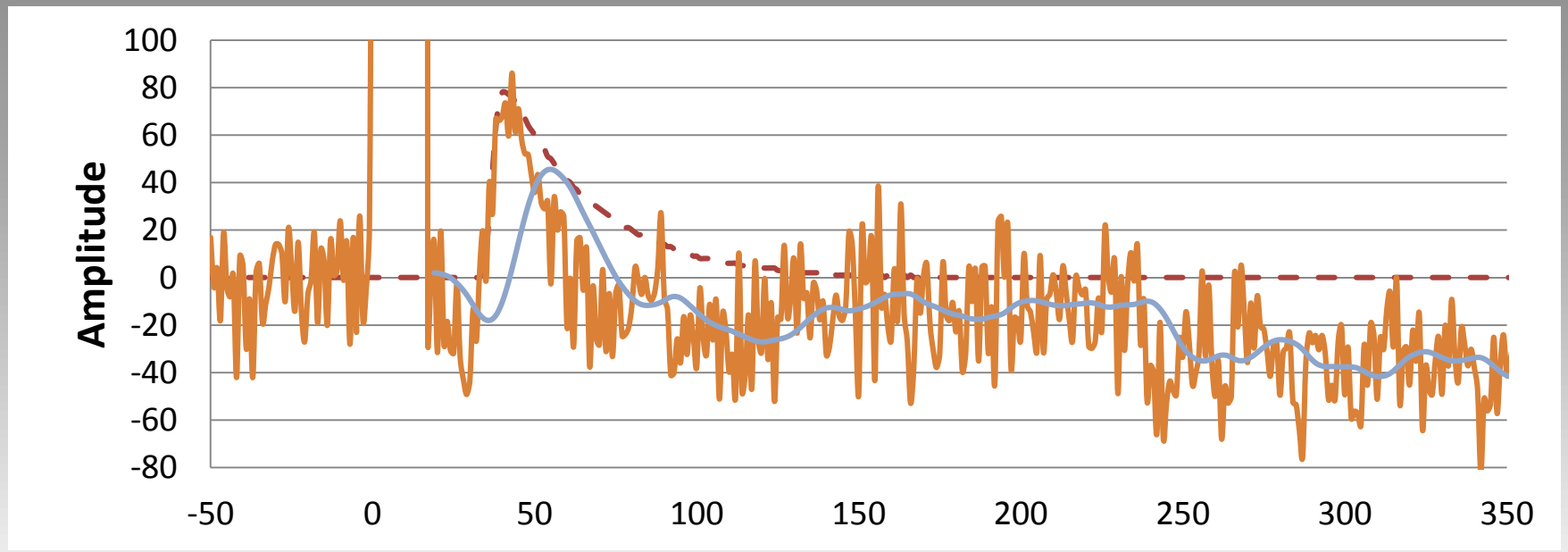




ADC for EMC-Endcap

- Pile-up recognition

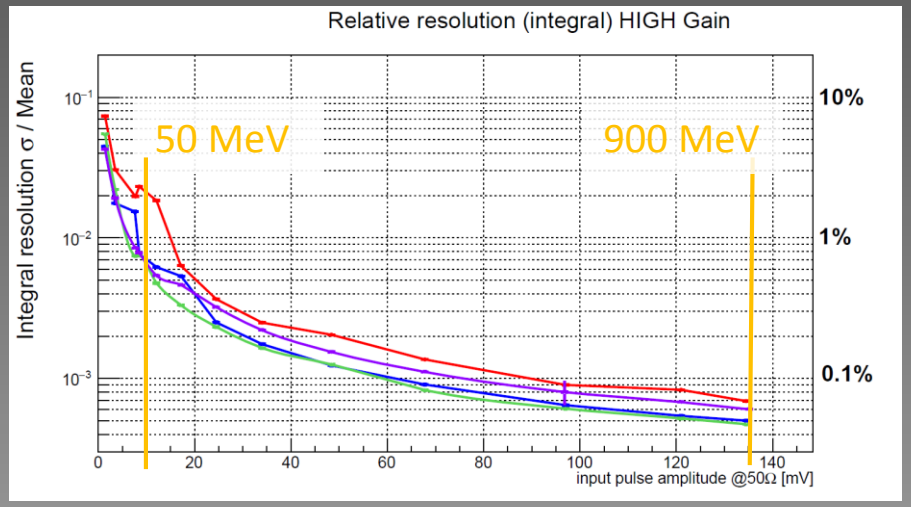


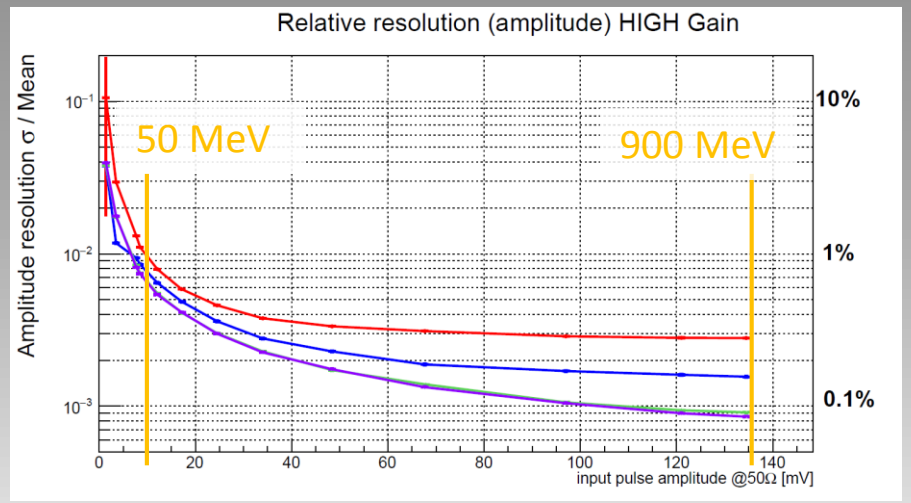


ADC for EMC-Endcap

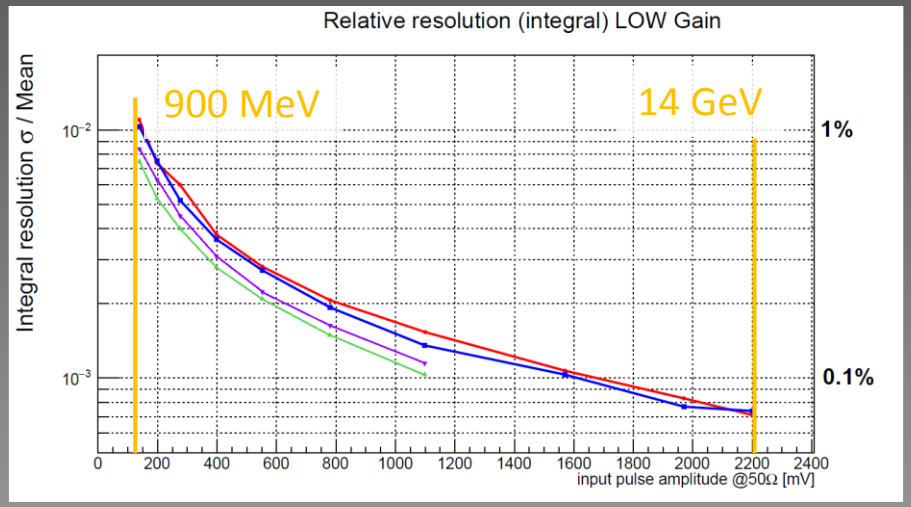
- Charge and amplitude resolution

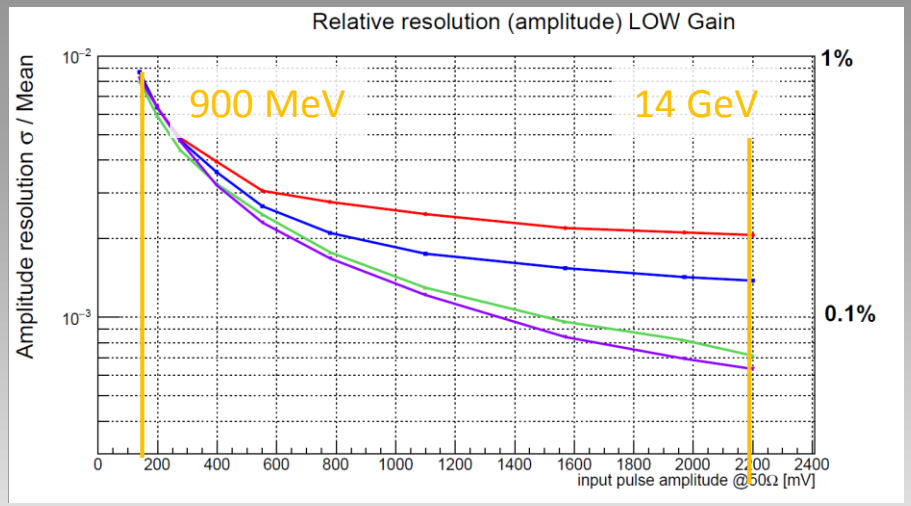
High gain range (-140..+140 mV)





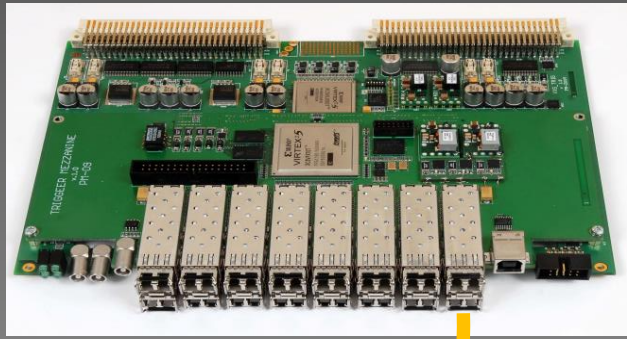
Low gain range (-2.2..+2.2 V)





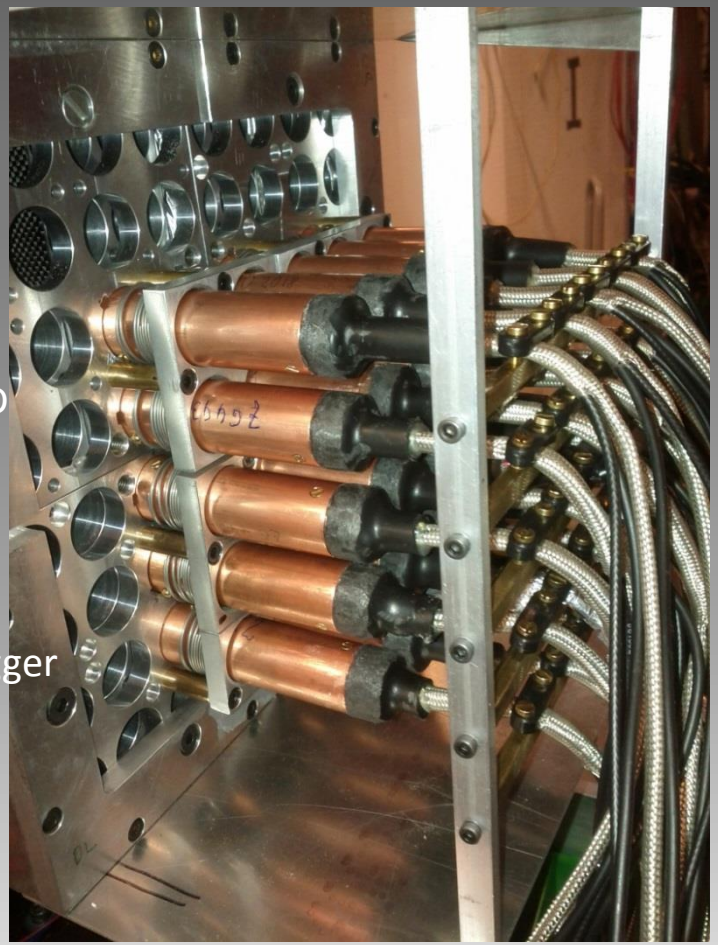
ADC for EMC-Endcap

- $PbWO_4$/VPTT tests at Max Lab



ATLB (VME Optical Data Concentrator)

$PbWO_4$ + VPTT
100uV/MeV



Data Format

- Event No
- Trigger Time Stamp
- Ch. No
- Ch. Time Stamp
- Ch. Amplitude
- Ch. Integral
- Ch. Raw Data 0
- .
- Ch Raw Data 63

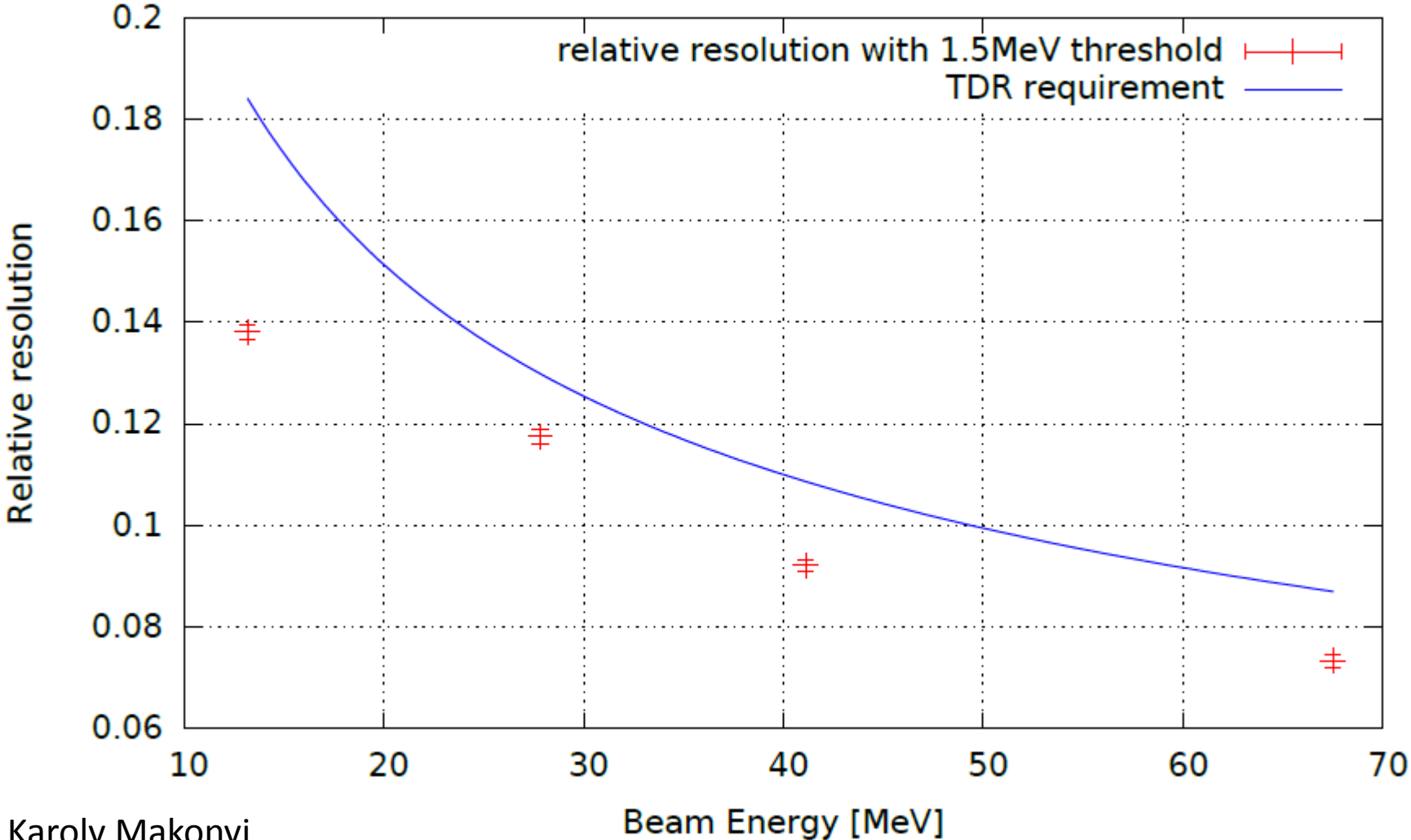
X9

Read Word Count

ADC for EMC-Endcap

- $PbWO_4$/VPTT tests at Max Lab

Relative Energy Resolution

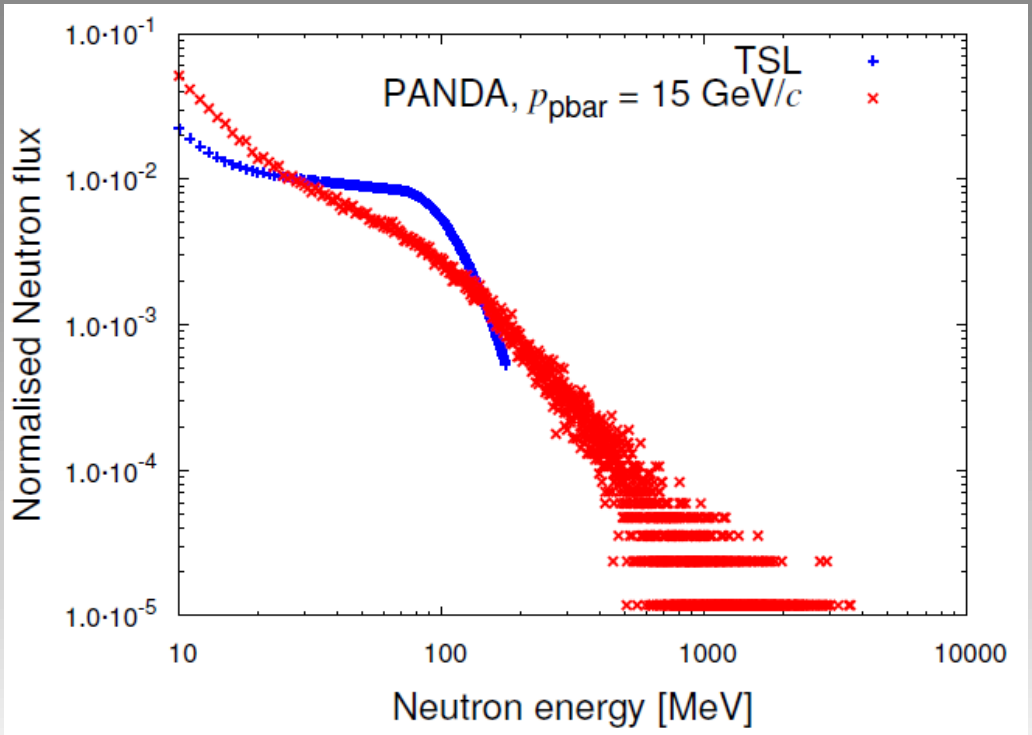


Karoly Makonyi

ADC for EMC

- Neutron irradiation

- The board was irradiated in June 2016 at the The Svedberg Laboratory (TSL) in Uppsala.
- Board placed in the Standard User Position (SUP), beam perpendicular to the board. One FPGA read out.
- Neutron flux between $5 \cdot 10^5$ and $1 \cdot 10^6$ s^{-1} cm^{-2} (>10 MeV).



ADC for EMC

- Neutron irradiation of the ADC_64K_2

The cross section for an SEU is given by:

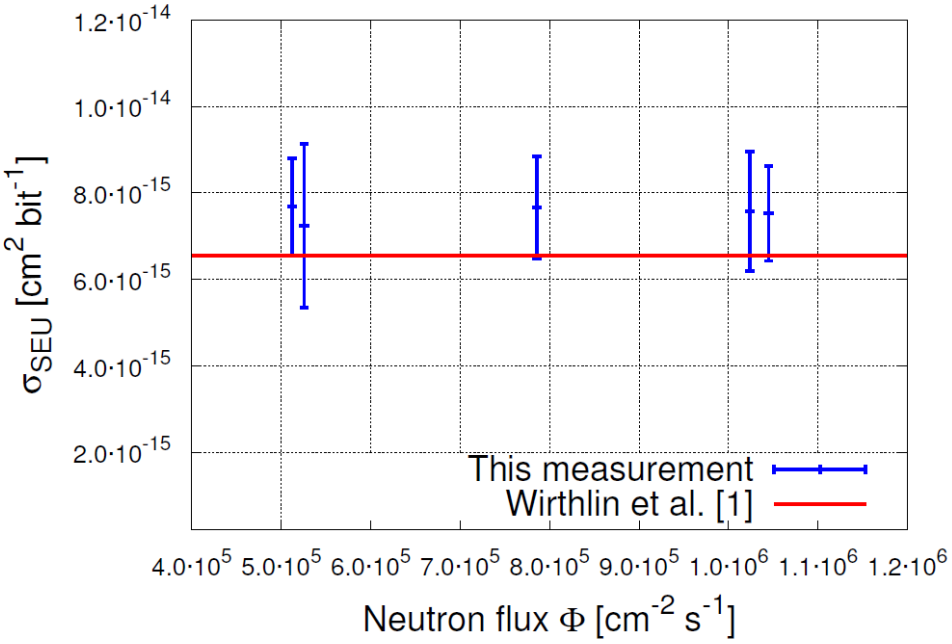
$$\sigma_{\mathrm{SEU}} = \frac{N_{\mathrm{SEU}}}{T_{\mathrm{meas}} \cdot \Phi_{\mathrm{n}} \cdot N_{\mathrm{bits}}}$$

Number of SEU

Measurement duration

Neutron flux

Total number of bits



[1] Wirthlin, M. J. et al. (2014) *JINST*. **9** C01025. ← Larger Kintex-7 @ TSL

- Neutron irradiation of the ADC_64K_2

MTBF calculation

$\sigma_{SEU} = 7.58 \cdot 10^{-15}$ (± 7%) $cm^2\ bit^{-1}$
$pp_{bar} = 15$ GeV/c
$L = 2 \cdot 10^{32}\ cm^{-2}\ s^{-1}$

Scaled Neutron Flux:
$\Phi_n = 150\ cm^{-2}\ s^{-1}$ (at position of digitisers)

Per digitizer board:

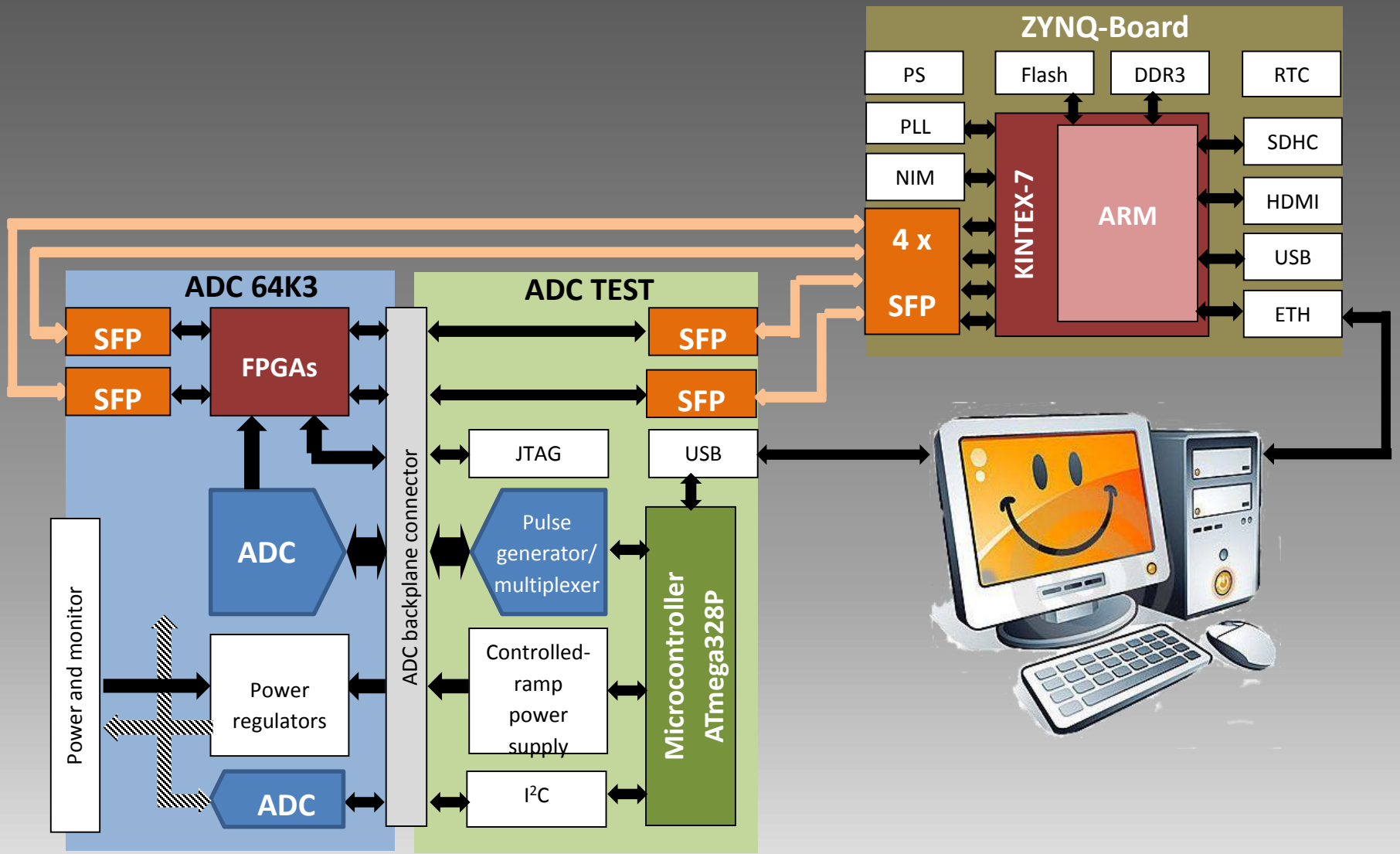
$r_{SEU} = 1.0 \cdot 10^{-4}\ s^{-1}$ → MTBF = **2.7 h** automatically correctable
$r_{SEU} = 3.5 \cdot 10^{-6}\ s^{-1}$ → MTBF = **90 h** needing reconfiguration (<200 ms)

Entire system (600 digitizers)

$r_{SEU} = 0,056\ s^{-1}$ → MTBF = **17,8 s** automatically correctable
$r_{SEU} = 0,002\ s^{-1}$ → MTBF = **529 s** needing reconfiguration (<200 ms)

ADC for EMC-Endcap

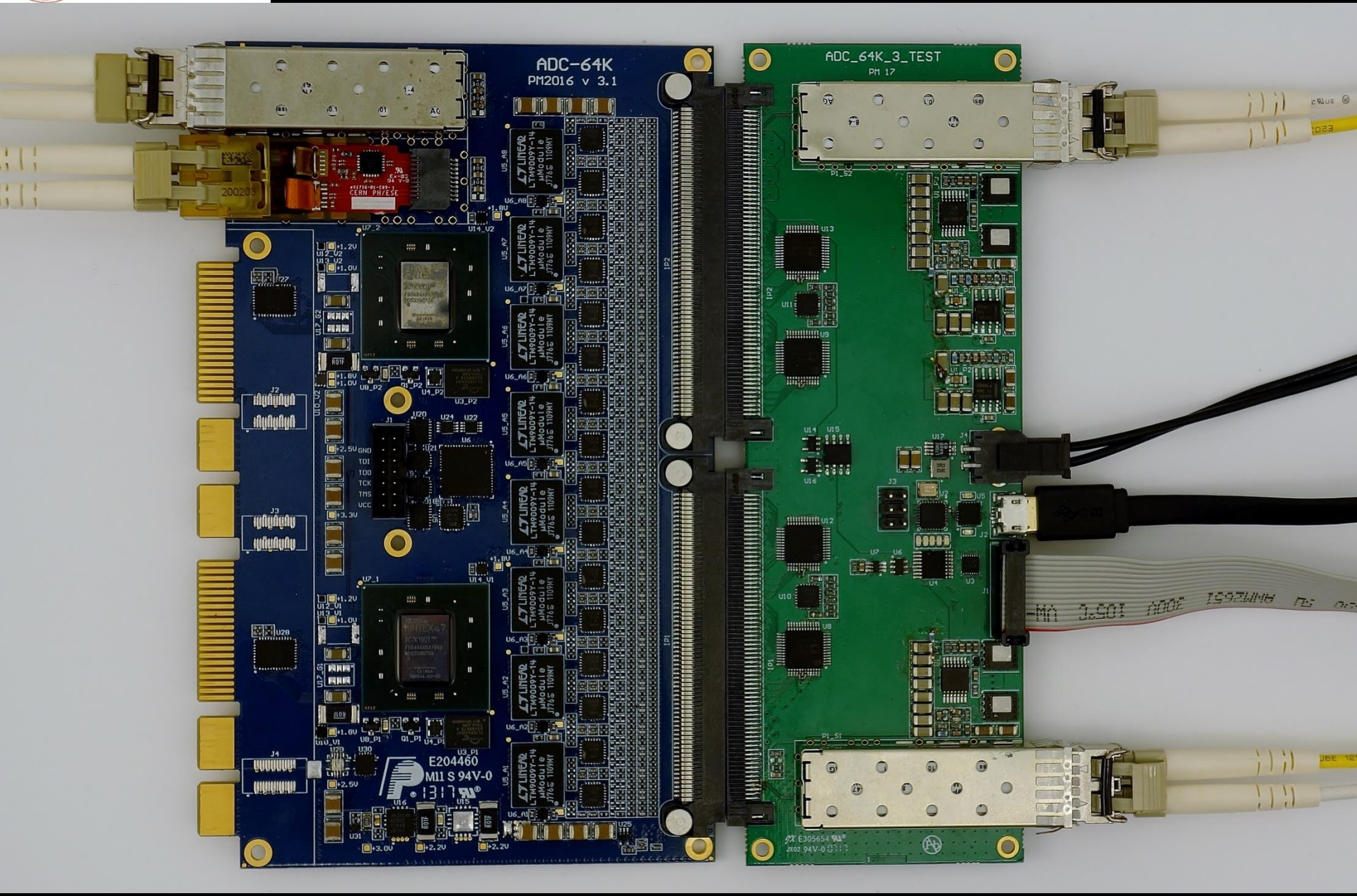
- Post-production functional tests



UPPSALA UNIVERSITET

ADC for EMC-Endcap

- Post-production functional tests

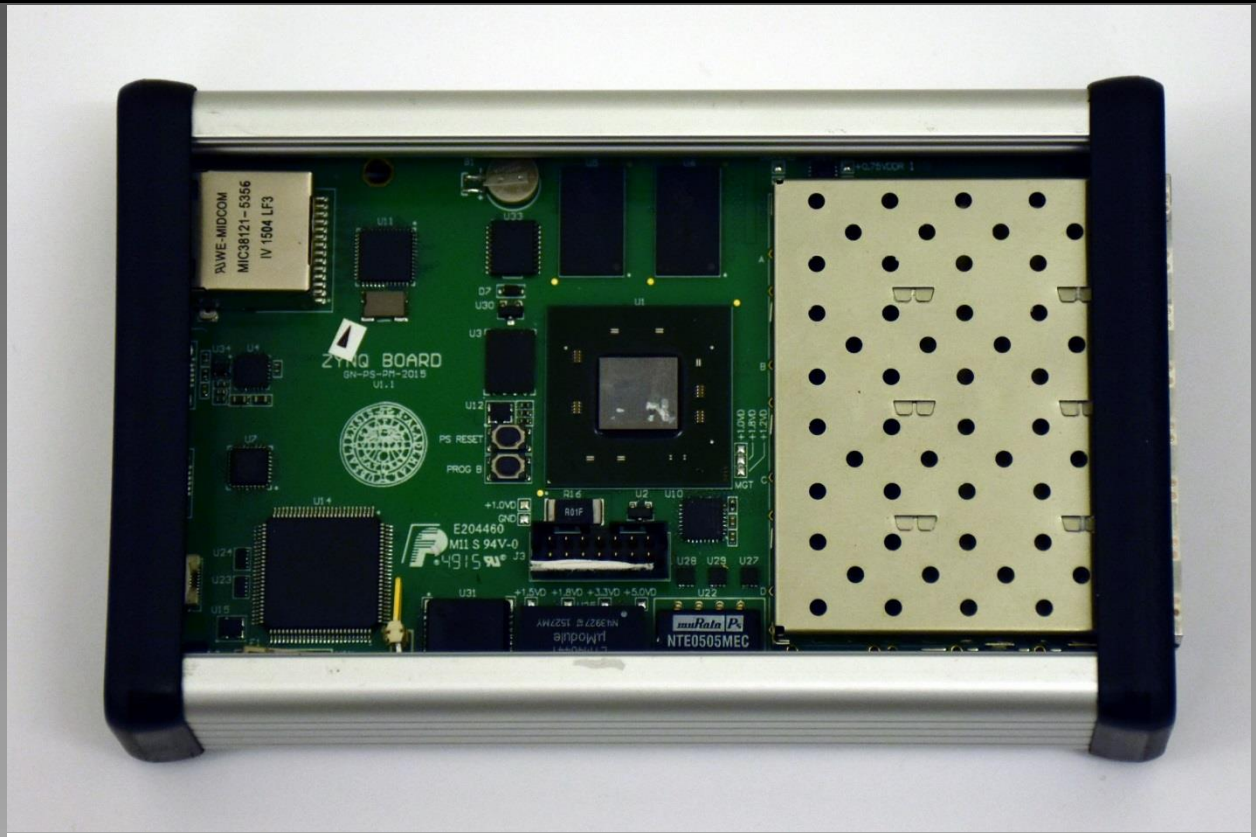


ADC for EMC-Endcap

- ZYNQ Board

ZYNQ-Board – Data Readout Module

- Tested
- Running Linux
- Communicating over Ethernet
- Prepared for data taking with any data format



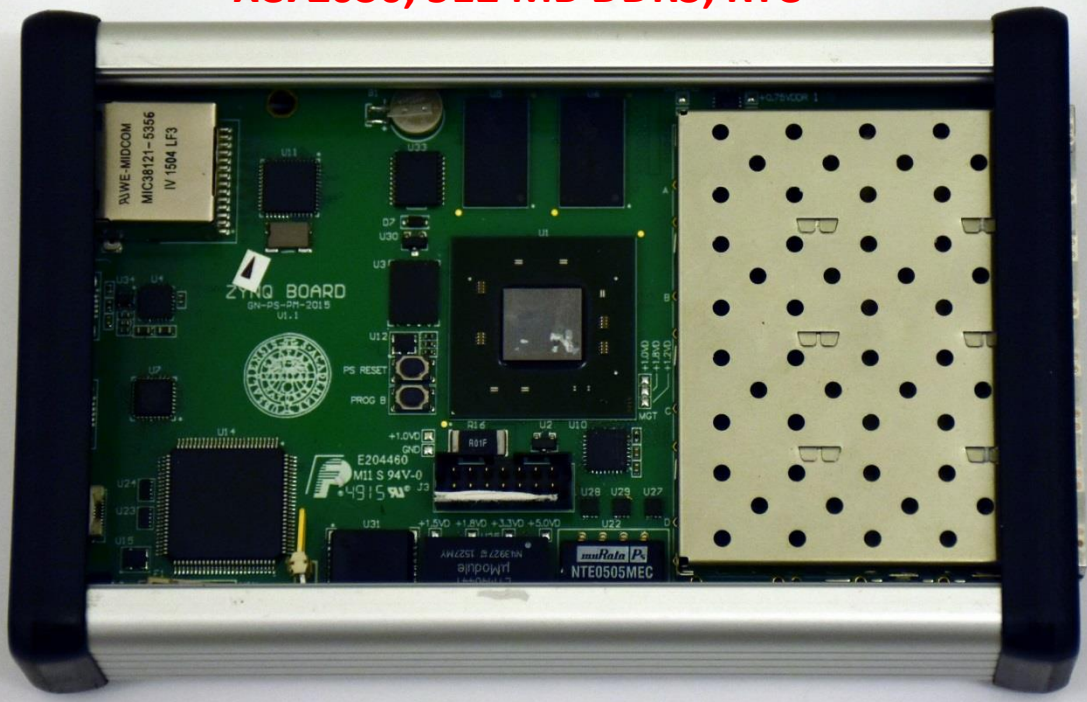
ADC for EMC-Endcap

- Final ADC Tests -ZYNQ Board

ZYNQ-Board – Data Readout Module

- Tested
- Running Linux/PetaLinux
- Communicating over Ethernet
- Prepared for data taking with any data format

XC7Z030, 512 MB DDR3, RTC



4xSFP+ (6.6 Gb/s)

4xNIM(I/O)

GbE, USART, USB, HDMI

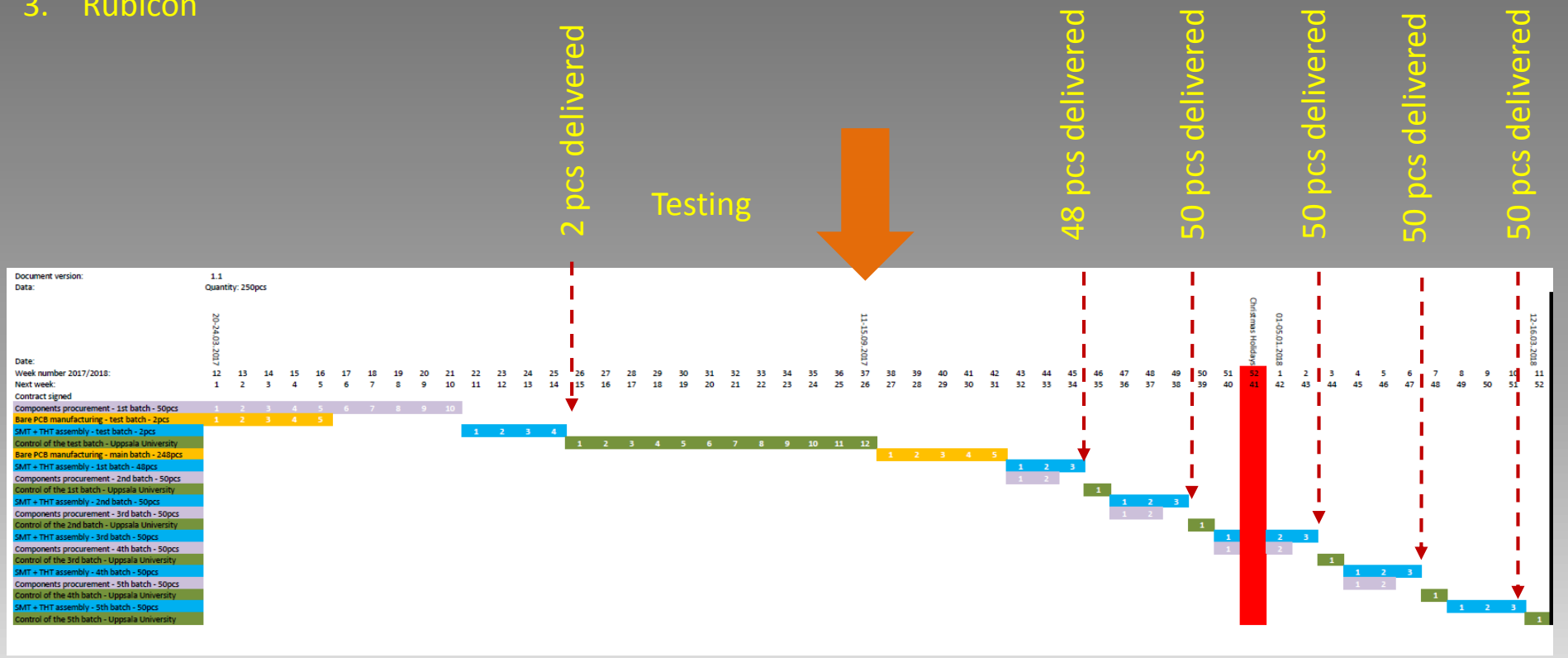
SDHC

- Production of 250 pcs for EMC Forward Endcap

Official Tender - finished!

Over 20 companies registered, 3 offers:

1. Syntronic
2. Semicon (winner)
3. Rubicon



ADC for EMC-Endcap

- Manpower

Uppsala

Hardware design - Pawel Marciniewski

Test software - Filza Saleem

Stockholm

Software/analysis - Markus Preston, Karoly Makonyi

KVI Groningen

Firmware/software - Peter Schakel, Myroslav Kavatsyuk

Uni Bonn

Firmware/software - Johannes Muellers

Uni Bochum

Software -/analysis - Malte Albrecht

Thank You !