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A Compact Size, 64-Channel, 80 MSPS, 14-Bit Dynamic Range ADC Module for the PANDA Electromagnetic Calorimeter

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A compact-size, 64-channel, 80 MSPS, 14-bit dynamic range ADC module for the scintillating electromagnetic calorimeter of PANDA was developed, tested in various detector readout set-ups and are currently in mass production phase. The module performs signal filtration, extract important signal parameters and allow for resolving and parametrizing overlapping pulses. Processed data are pushed to optical links running at 2 Gbit/s. The ADC module is equipped with a PLL phase noise cleaner and allows for defined latencies. 225 of these modules will be placed inside of the PANDA detector volume, exposed to magnetic field of up to 2T and a non-negligible radiation flux.

Summary

The Electromagnetic Calorimeter (EMC) of the Anti-Proton Annihilation at Darmstadt (PANDA) detector at the Facility for Antiproton and Ion Research (FAIR) consists of over 15000 PbWO4 crystals and is designed for detection and parametrization of particles with kinetic energies up to 15 GeV [1]. For accurate reconstruction of events in the PANDA, a correct merging of energy spills as low as 1 MeV per crystal is desired. Since all EMC crystals will be equipped with double photo-sensor readout and a 14-bit dynamic range is obtained in a dual-range ADC structure, the total number of digitizer channels placed inside of the detector volume will exceed 60000, requiring highly compacted electronics.

The signals entering the ADC are shaped using analog filters and then processed by a set of 8-channel 14-bit, 80 MSPS analog-to-digital converter circuits. Digitized samples are sent to 2 FPGAs via 128 LVDS links running at 560 Mbit/s each. The FPGAs allow for signal filtration, and extracting of important signal parameters, such as time of arrival, pulse amplitude and pulse integral. Analog and digital signal filtration parameters and algorithms were optimized to fulfill the required dynamic range and provide acceptable pile-up resolution at the anticipated maximum hit rate of 500 kHz per channel.

The processed data are pushed to optical links via multi-gigabit transceivers (GTX) running at 2 Gbit/s. The implemented UDP/IP core leads to a great simplification of lab setups allowing the SADC data to be directly transferred to a PC for test purposes.

The ADC modules are equipped with PLL phase noise cleaners and allow for defined latencies. The ADC module is compliant with the SODA System, for which the reference clock is distributed by a detector synchronization system (SODA), using the down-link part of the ADCs optical transceiver [2].

In order to test the endurance of the ADC in a radiation environment, the device was irradiated with a neutron beam at The Svedberg Laboratory (TSL), Uppsala University in June 2016 and with a proton beam delivered by the AGOR cyclotron at KVI, Groningen in November 2016.

During the experiment, the Xilinx Soft Error Mitigation (SEM) Controller was placed in the FPGA.

During the a test beam-time at Max Lab in Lund, 2014, the ADC was used in a detector setup for testing response of EMC Forward End-Cap PbWO4 crystals to photons with energies of 11, 26, 38 and 62 MeV. After off-line energy reconstruction, the relative energy resolution was found to be fulfilling the Technical Design Report requirements of the PANDA EMC with a safety margin.

The dimensions of the 64-channel modules amount to 100x150 mm. Despite a high channel density, no measurable crosstalk has been observed. The power consumption amounts to 22W. This requires efficient cooling, which will be accomplished by liquid-cooled aluminum encapsulations in the PANDA.

[1] PANDA EMC Technical Design Report, arXiv:0810.1216v1, (2008).
[2] I. Konorov et al., Conference Record, 2009 IEEE NSS, Orlando, Florida, USA.

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