Compact Muon Solenoid experiment at CERN's LHC

TWEPP2017

Quality control considerations for the development of the front end hybrid circuits for the CMS Outer Tracker upgrade

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on behalf of the CMS Outer Tracker Upgrade collaboration

Outline

Introduction to the project

Description of the problem

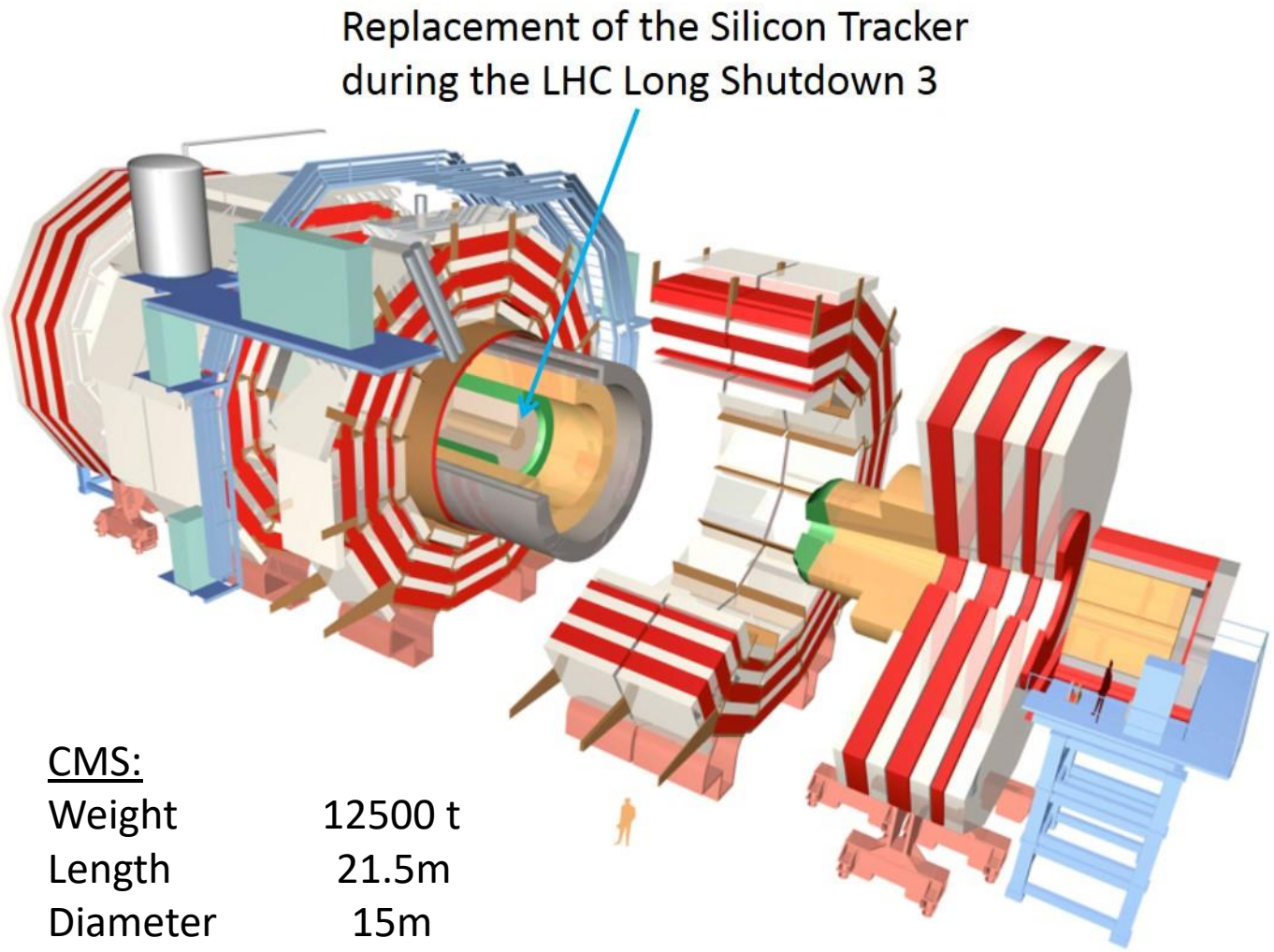
Active test methods

Verification platform

Test results

Cold Box

Introduction – CMS Tracker Upgrade

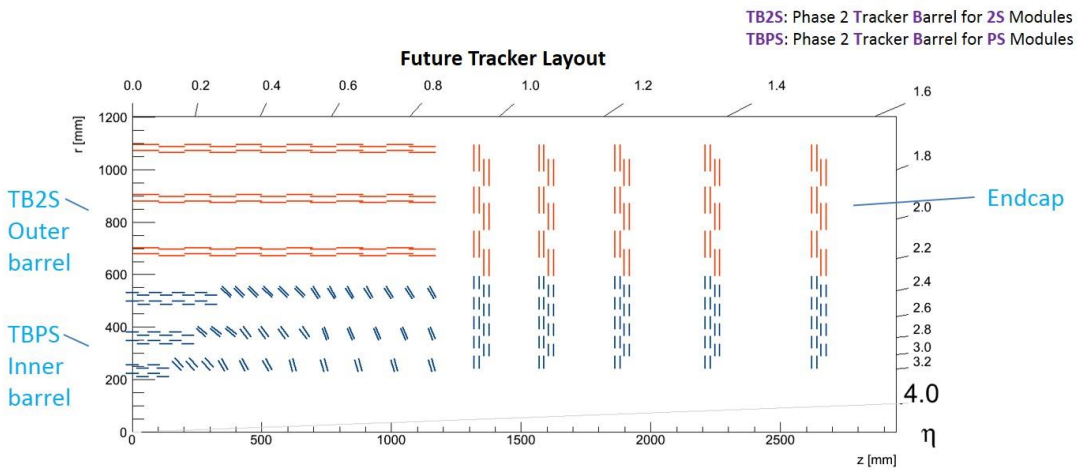


CMS:

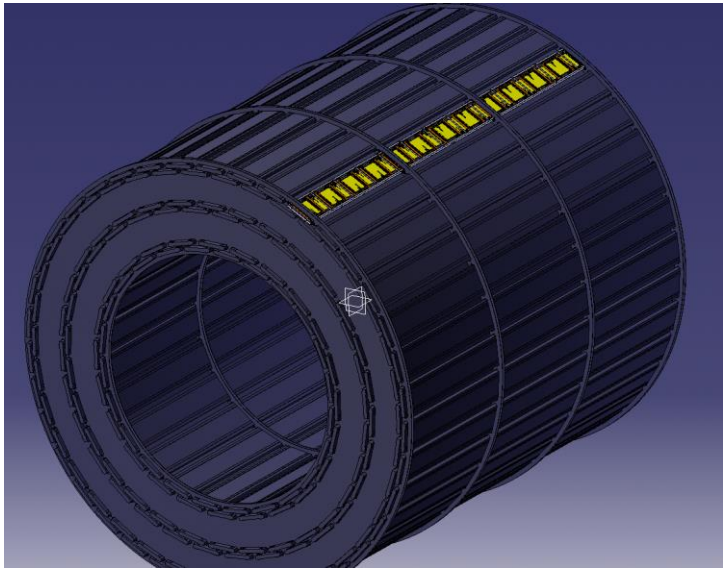
Weight	12500 t
Length	21.5m
Diameter	15m

Introduction – CMS Outer Tracker's building blocks

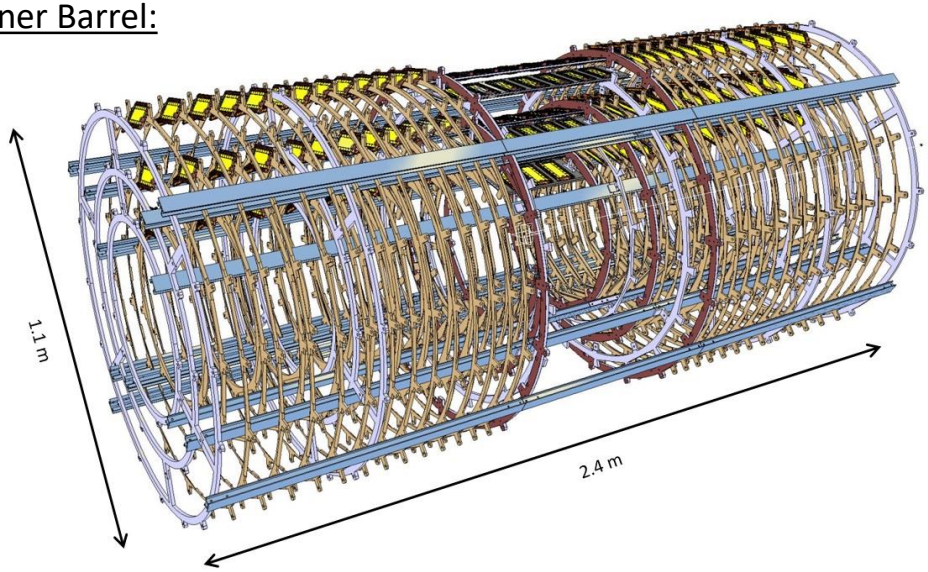
Cross-section of 1 quarter of the CMS Outer Tracker:



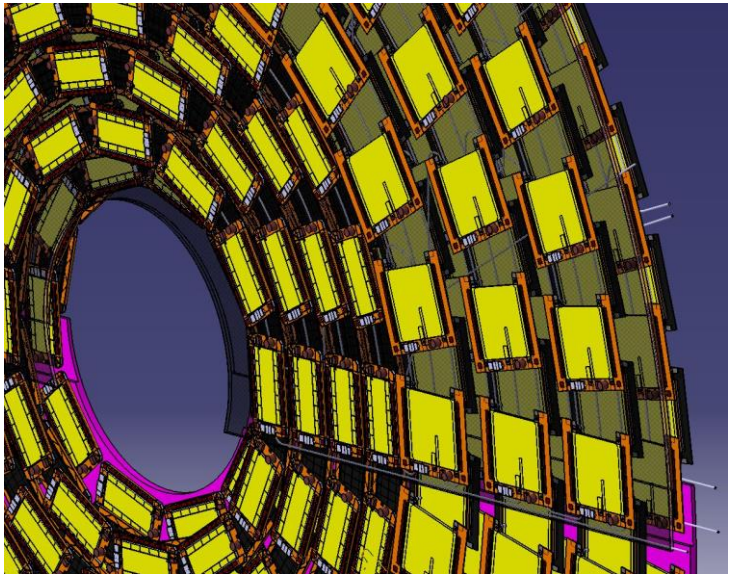
Outer Barrel:



Inner Barrel:



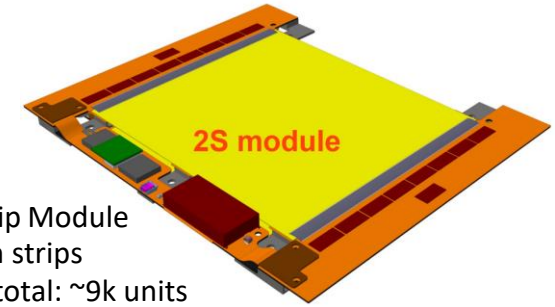
Endcap disc:



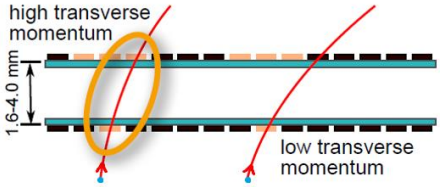
Introduction – Modules and Hybrids

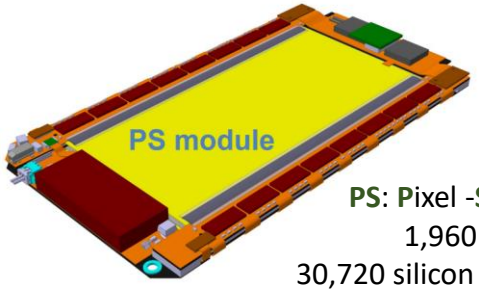
Front End Modules:

- Two types: 2S and PS,
- Double-sensor,
- Different heights,
- High momentum discrimination.



2S: **S**trip-**S**trip Module
4,064 silicon strips
Production total: ~9k units

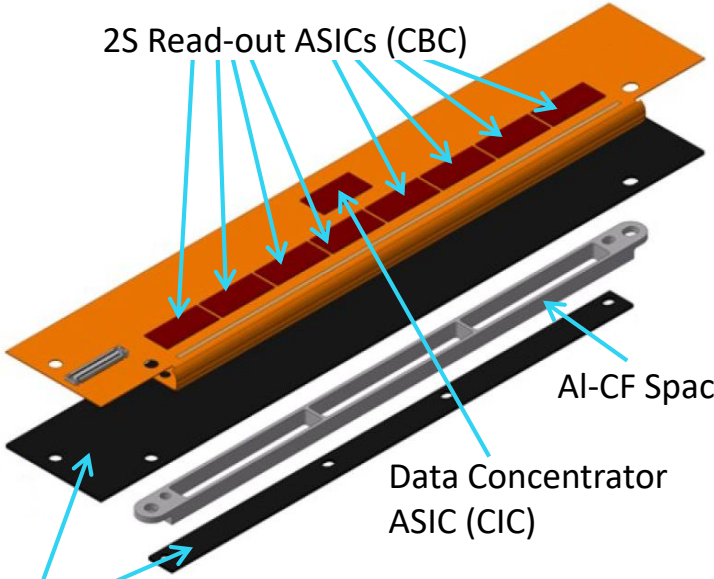


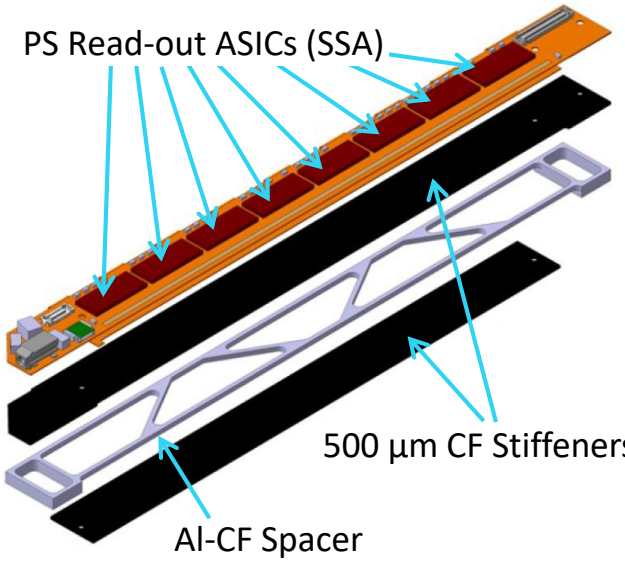


PS: **P**ixel -**S**trip Module
1,960 silicon strips
30,720 silicon macro pixels
Production total: ~6k units

Front End Hybrids (FEHs):

- HDI flexible circuit,
- Stiffeners and spacers,
- ASICs,
- Passives.





HDI – High Density Interconnect
CF – Carbon Fibre
Al-CF – Aluminium Carbon Fibre

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Quality control – why and how?

Need for FEH's quality control

- ~4000 wire bonds per module
- reworks unlikely during production phase
- 1 bad ASIC assembly = lost module
- High yield of modules = use of known good FEHs

Optical inspection

- Set of dimensions and surface quality measurements
- Weighing
- High voltage breakdown test
- Adhesive check
- Solder joints check (passives)
- And many more…

Set of active tests

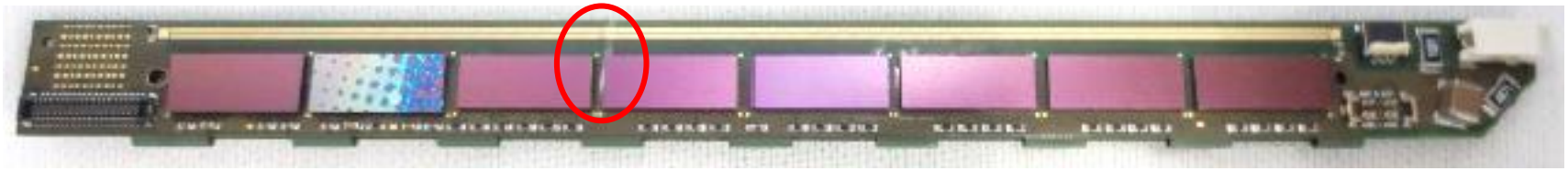
- Check of proper interconnectivity of FEH's components
- Verification of FEH's functionality
- Readout chain required
- Room temperature tests
- Low temperature tests (cold box)

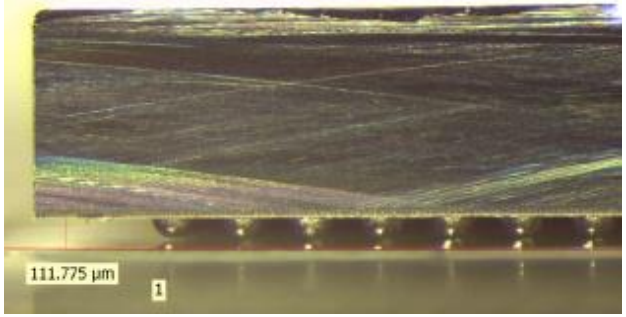
FEH – Front End Hybrid

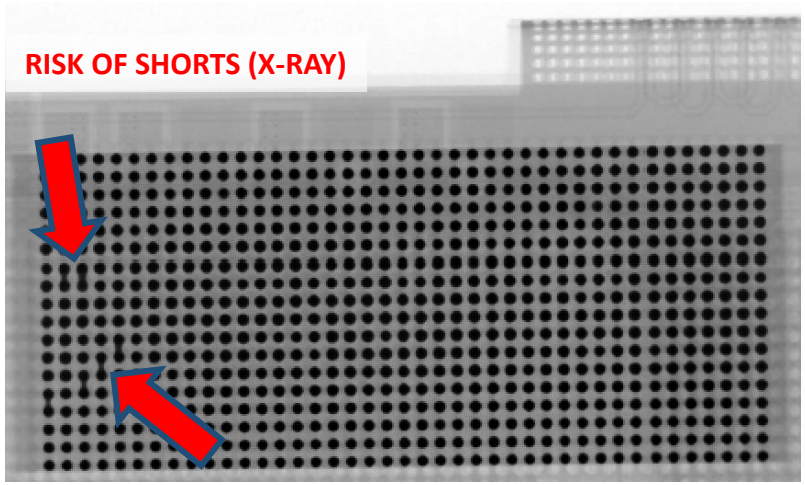
Main source of troubles: non-flatness of the circuit under ASICs (+ not ideal bumps)

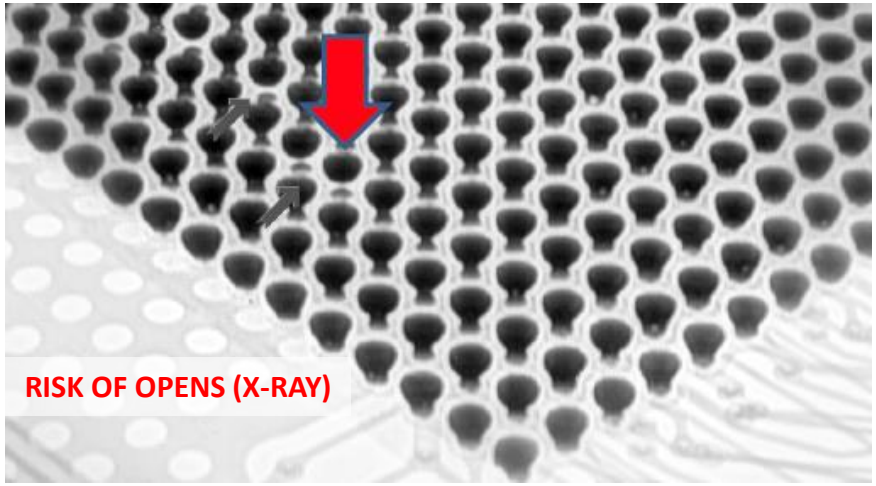
Root causes:

- differences in C(s)TE of the hybrid's components (impact during reflow),
- circuit design constraints (imbalanced, non-symmetric copper distribution).



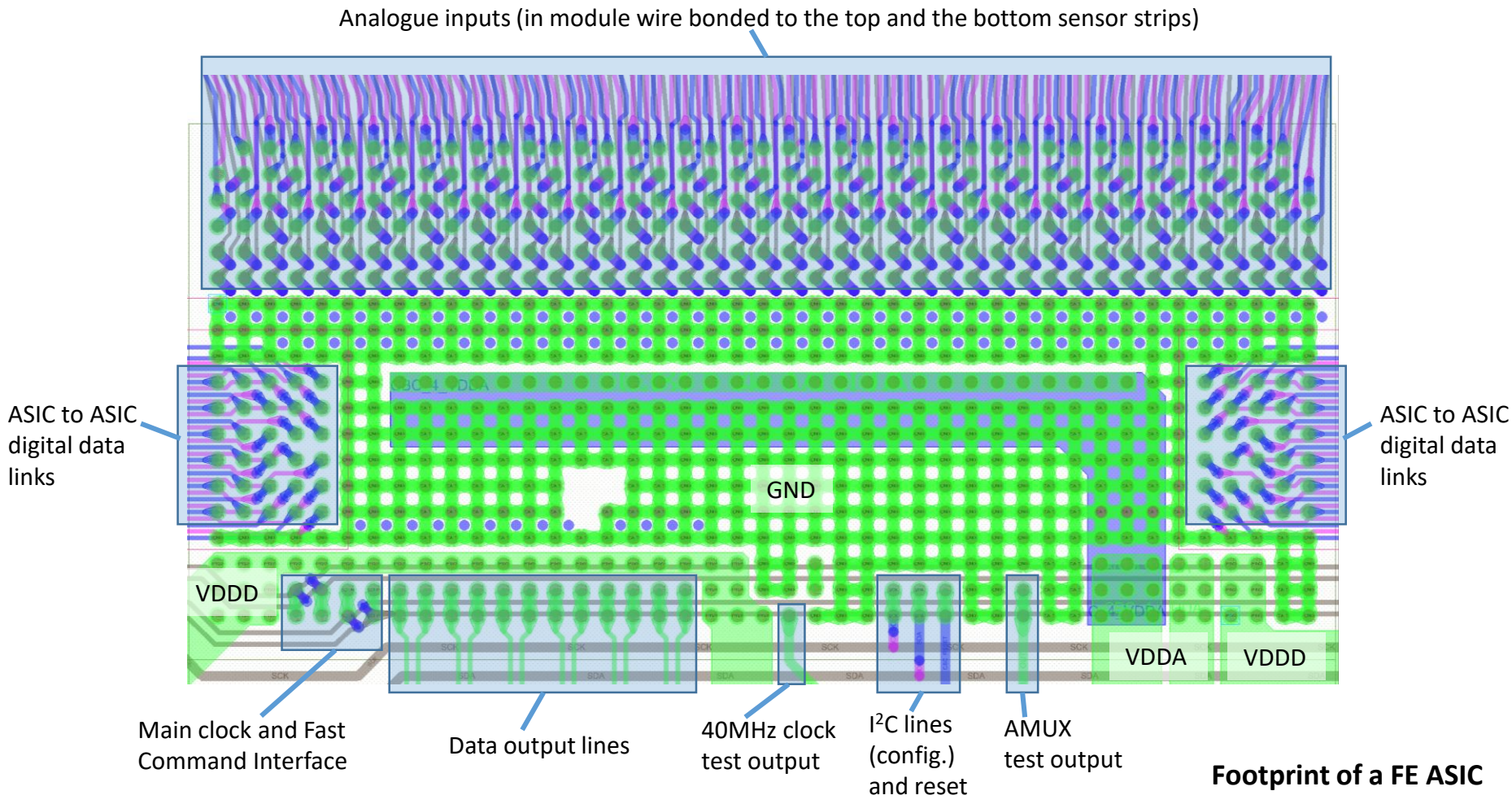






An example of a Front End ASIC footprint and interconnections

- Hybrid's assembly problems (so far) affect exclusively the ASICs to flex connectivity.
- ASIC's connectivity verification became a priority.
- Different active methods apply to 3 different I/O types.



Footprint of a FE ASIC

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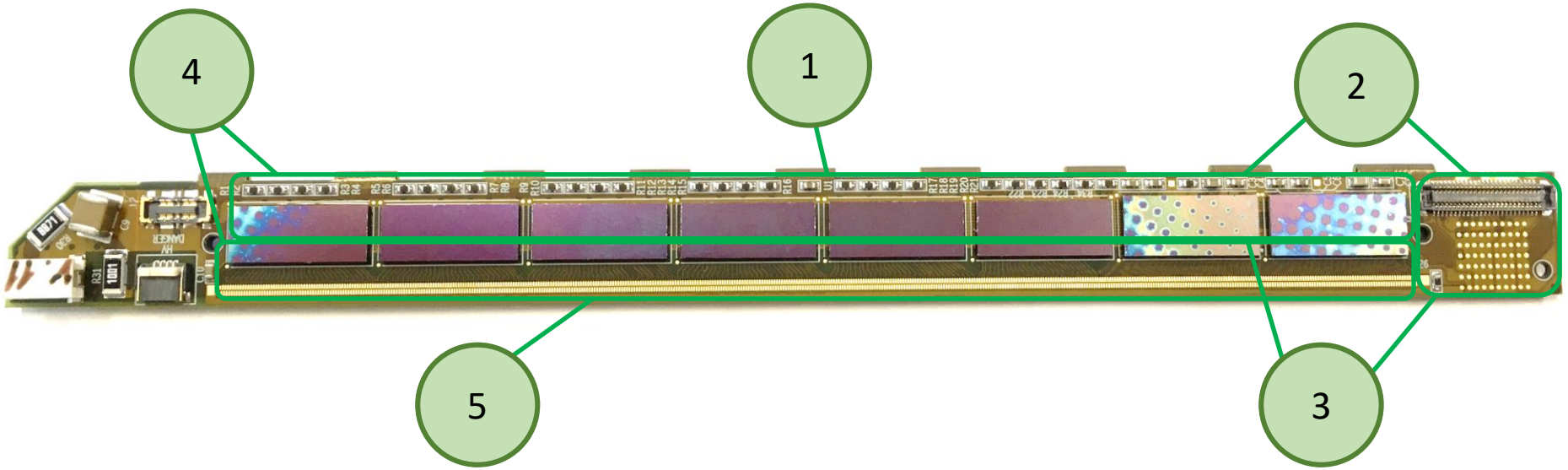
Set of active test methods (in that order)

1. Power consumption.
2. Slow control interface & configuration registers.
3. Clock, fast commands and data interfaces.
4. Calibration of analogue FE channels & noise-driven hit counts.
5. **Specific tests for detecting open and shorted analogue connections.**



Detection of opens in analogue connections

- Active testing of the connectivity of analogue inputs requires their stimulation.
- Temporary bonding impractical (2032 wires needed).
- Need for fast and contactless method.
- Stimulating signals can be injected externally (capacitively).
- Incomplete or grounded signal path »»» absence/weak response to the stimulation
- Signal is injected to groups of neighbouring channels »»» cannot reveal shorts.

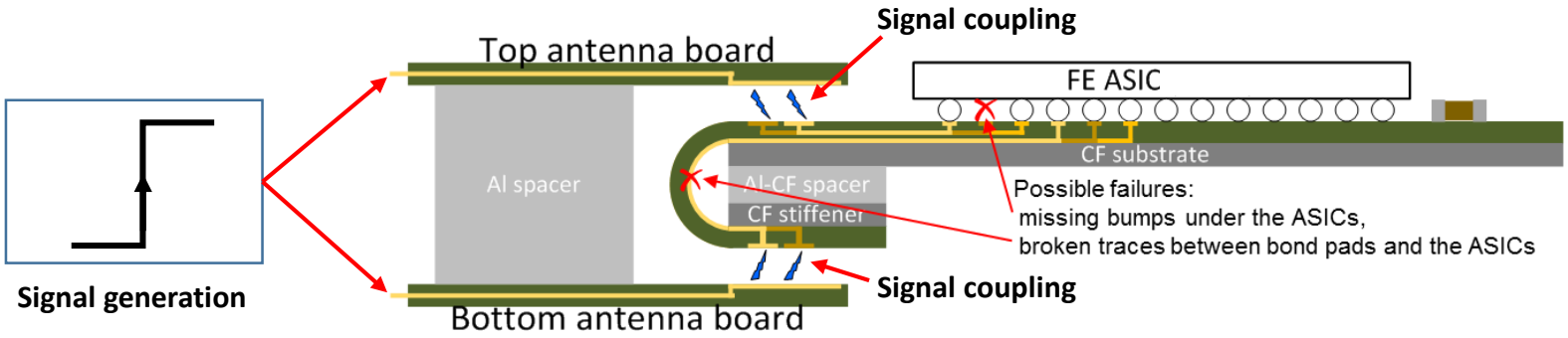


Figure: A cross-section sketch of signal injection into a folded front end hybrid

Examples of charge injection circuits

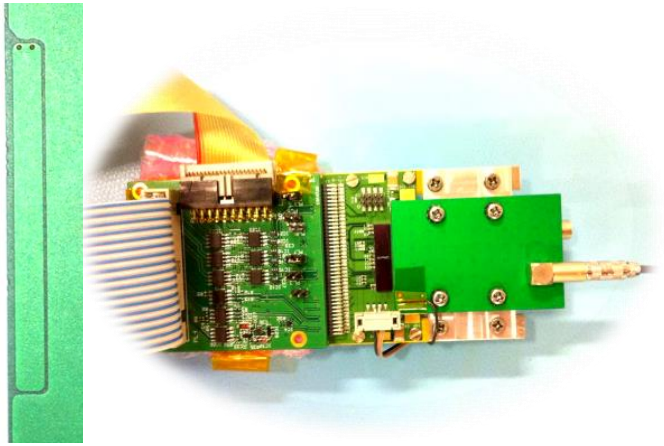


Figure: Photo of a setup with two single-strip antenna boards for 2CBC2 hybrid testing

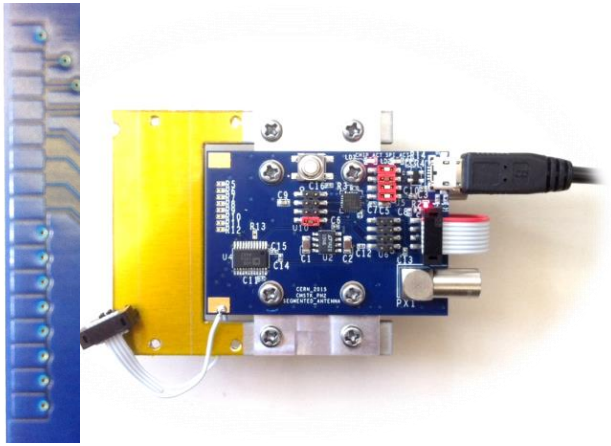


Figure: Photo of a setup with two segmented antenna boards for 2CBC2 hybrid testing

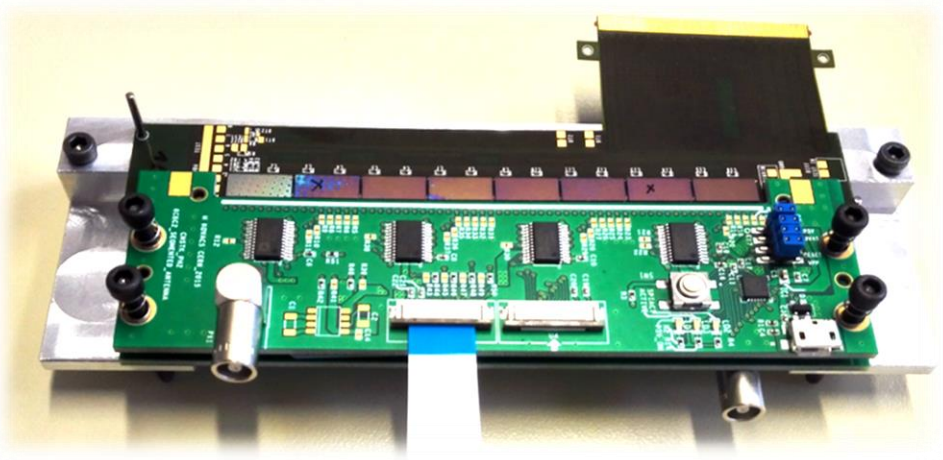


Figure: Photo of a setup with two segmented antenna boards for 8CBC2 hybrid testing

Example of opens detection

Example of use - 2CBC2 hybrid with cut bumps

Output of the open connections scan algorithm:

antenna_test.txt

```
1  Antenna scan test results (channels numbering starts with 0).
2  Rejection threshold 10%:
3  Malfunctioning Channels on the TOP side : 0, 1, 251, 253,
4  Malfunctioning Channels on the BOTTOM side : 0, 1, 253,
5
6  Rejection threshold 80%:
7  Malfunctioning Channels on the TOP side : 0, 1, 251, 253,
8  Malfunctioning Channels on the BOTTOM side : 0, 1, 253,
```

Occupancy histogram obtained during the scan:

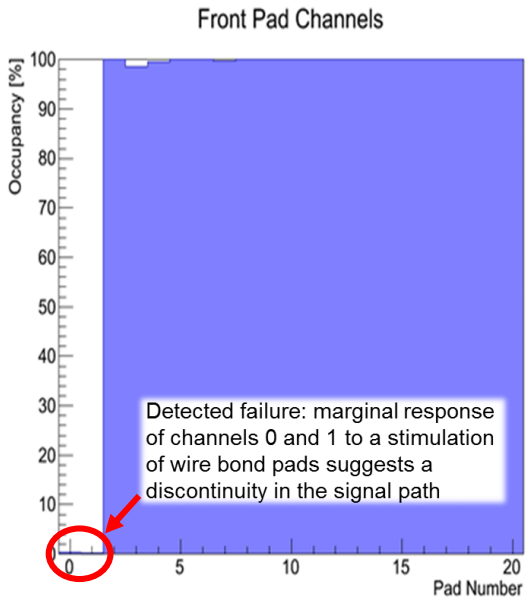


Figure: Front channels histogram obtained during 2CBC2 antenna test (zoomed at 21 ch.)

Detection of shorts in analogue connections

- Stimulating signals can be injected internally in the ASIC (test or calibration pulse)
- Short between channels »»» activity of channels which should not be stimulated
- Short to ground »»» no activity of channels which should receive test pulses

(test pulse cap. 20 fF, charge step range 10 fC)

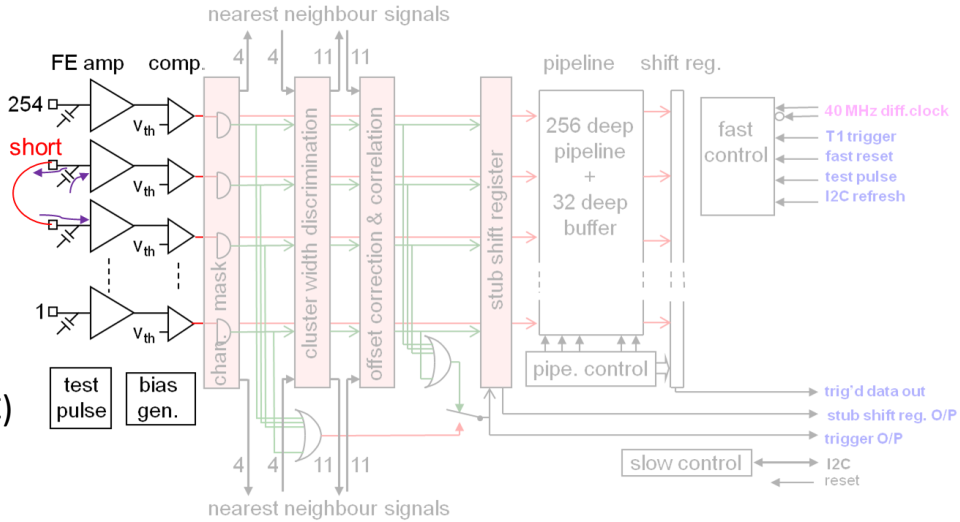


Figure: CBC2 signal path with shorted channels 253 and 252

Module's case:

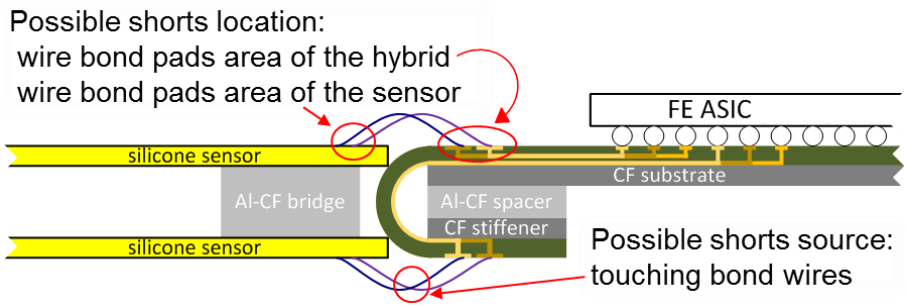


Figure: A sketch of an 8CBC2 hybrid wire-bonded to sensors

Hybrid's case:

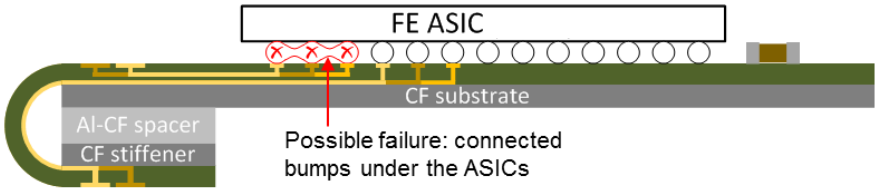


Figure: A cross-section sketch of a folded 8CBC2 hybrid with shorted bumps

Example of shorts detection

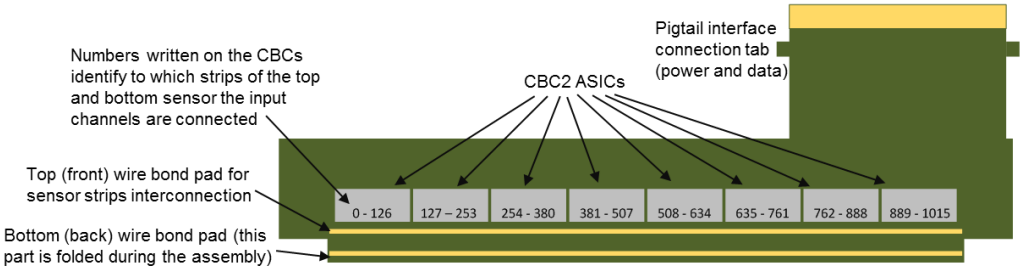


Figure: An explanatory sketch of an unfolded 8CBC2 hybrid components

Example of use - 8CBC2 prototype (a short between bumps under CBC)

```
Shorted channels searching procedure
Sides: Front - 0  Back - 1 (Channel numbering starts from 0)

 Side   | Channel_ID   | Group_ID     | Shorted_With_Group_ID
-------------------------------------------------------------
   0    |       886    |       4      |       1
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
   0    |       883    |       1      |       4
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
```

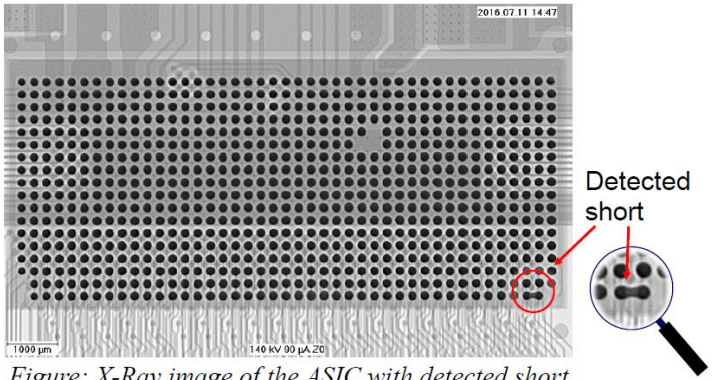


Figure: X-Ray image of the ASIC with detected short

Example of use – 2S module prototype number 3 (a short between wire-bond pads on the sensor)

```
Shorted channels searching procedure
Sides: Front - 0  Back - 1 (Channel numbering starts from 0)

 Side   | Channel_ID   | Group_ID     | Shorted_With_Group_ID
-------------------------------------------------------------
-------------------------------------------------------------
   1    |       1012   |       3      |       2
-------------------------------------------------------------
   1    |       1011   |       2      |       3
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
```

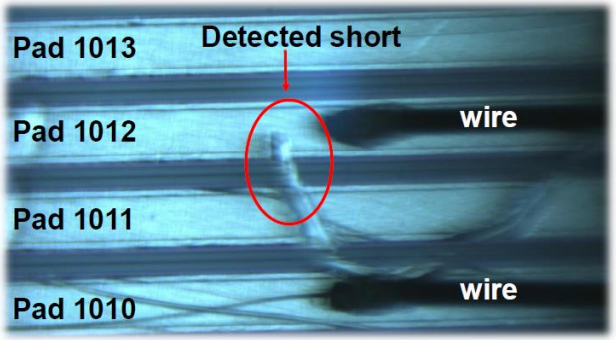
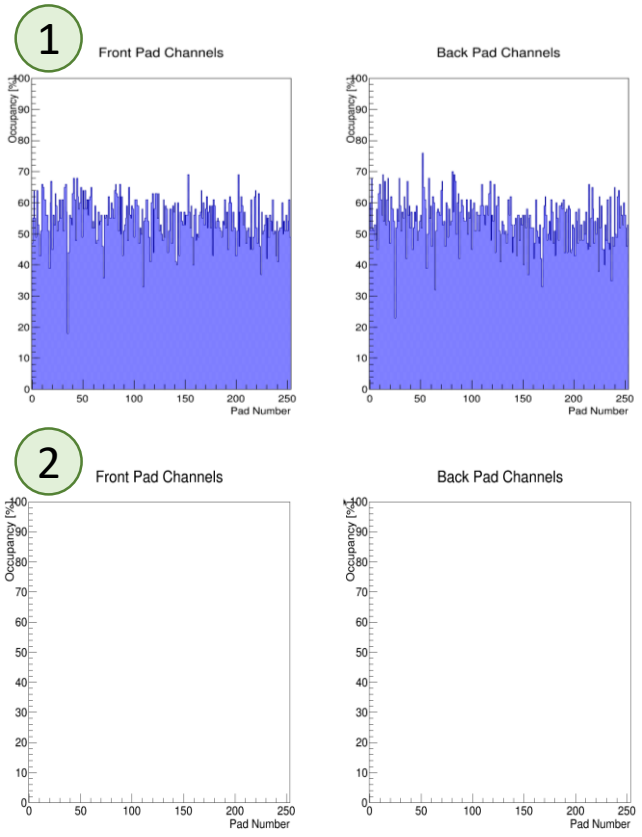
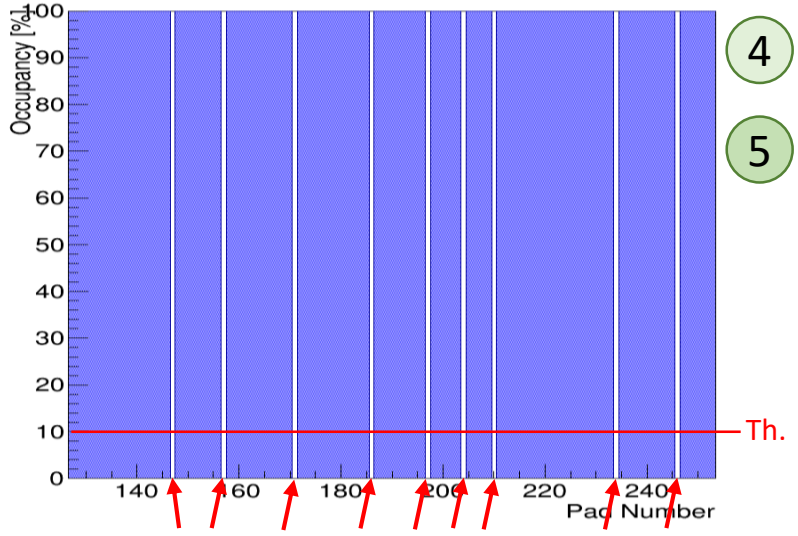


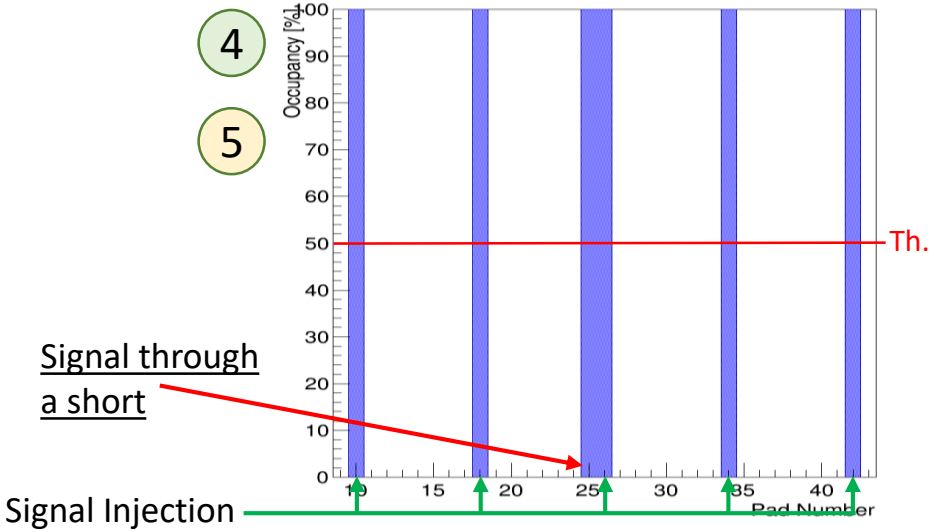
Figure: A microscope image of the short between pads on the silicon sensor detected by the algorithm

OPENS detection algorithm	SHORTS detection algorithm
1. Calibrate	
2. Adjust comparators threshold	
3. Inject signals…	
…externally, to groups/all channels	…internally, to isolated channels
4. Get hit counts (occupancy of FE channels)	
5. Set decision threshold, channels below are disconnected or grounded	5. Set decision thresholds, not stimulated ch. above threshold are shorted, stimulated ch. below th. are grounded





Signal below threshold = open/grounded connection



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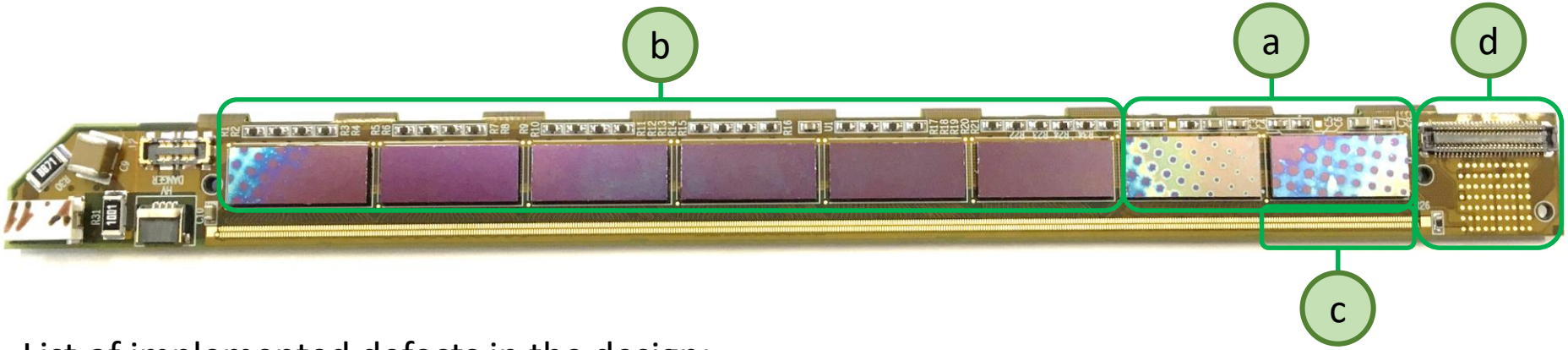
Hybrid for the evaluation of test algorithms

A hybrid was designed with deliberately implemented failure modes to verify test methods:

a) 2 functioning ASICs,
b) 6 dummy chips,
c) Charge injecting pads buried in the circuit (for one ASIC),
d) Temporary interconnection to interface boards via mezzanine connector or probe pads,
e) 3 different companies (X, Y, Z) were identified to produce the hybrids,
f) X and Y delivered 2 batches.



List of implemented defects in the design:

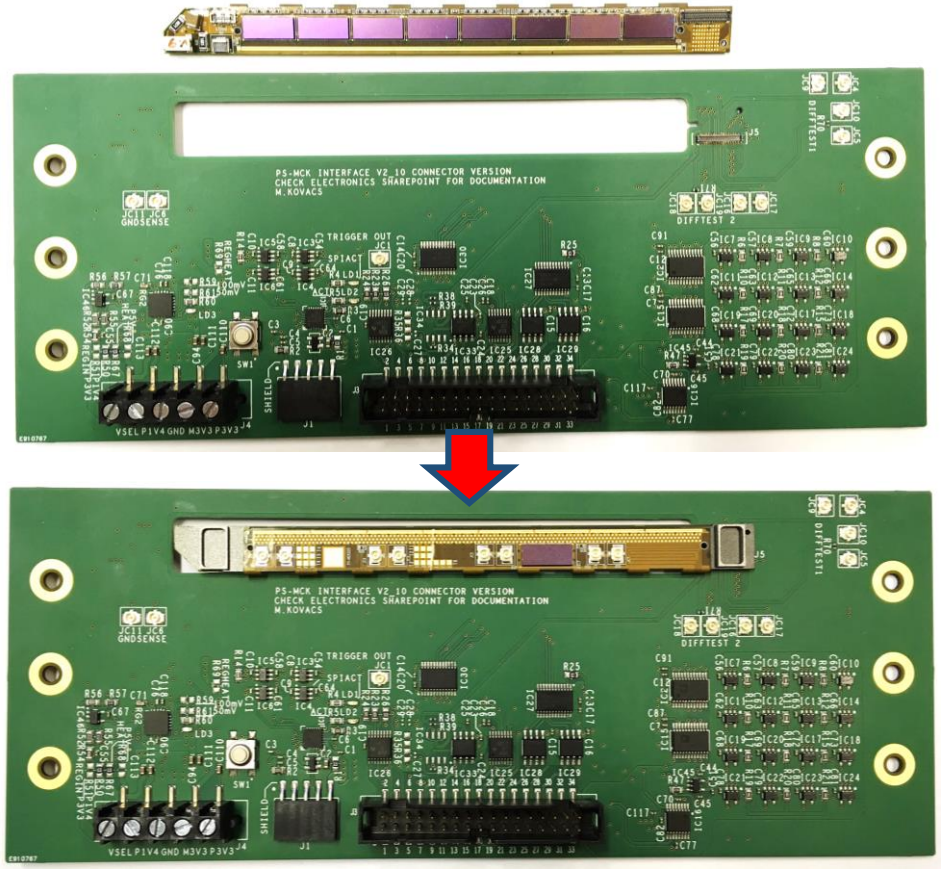
- 7 shorts per ASIC between pairs of analogue front end channels,
- 3 shorts per ASIC between a front end channel and GND net per ASIC,
- 8 opens in the second chip (3 broken traces + 5 missing vias).

For more details on this hybrid please follow a dedicated talk on Thursday by Mark Kovacs

Hybrid for the evaluation of test algorithms - interface

Two types of interface card were produced:

- 1 for the bench top use with a mezzanine connector,
- 1 for the cold box use with a spring loaded pins socket,
- Conversion of signals from a hybrid to an FPGA-based readout,
- Software controlled charge injection and trigger generation circuit on board.



Interface card for a bench top use

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X hybrids - evaluation results

- 14 hybrids from vendor X were produced and tested
- Execution of all test methods ~42 s/hybrid, 100% repeatability and accuracy*

X PS-MCK hybrids - summary table of active tests.

Hybrid ID	Current consumption [AVG: 105.5mA / 151.5mA]	Data links and config. registers diagnosis	Analogue shorts detection mutual, to GND, [+ additional]	Analogue opens detection Implemented, [+ additional]
P.1	OK	OK	9/14, 4/6, [+ 0/0] too many missing shorts	9/11, [+ 53/0]
P.3	OK	OK	OK	9/11, [+ 0/0]
P.4	idle: excessive, busy: OK	OK	OK	9/11, [+ 1/0]
P.5	OK	OK	OK	9/11, [+ 8/0]
P.6	OK	OK	13/14, 6/6, [+ 0/0]	9/11, [+ 3/0]
P.7	OK	OK	OK	9/11, [+ 0/0]
P.8	OK	OK	OK	9/11, [+ 0/0]
P.9	OK	OK	OK	9/11, [+ 0/0]
P.10	OK	OK	OK	9/11, [+ 0/0]
P.11	OK	OK	OK	9/11, [+ 0/0]
P.12	OK	OK	OK	9/11, [+ 0/0]
P.13	OK	OK	OK	9/11, [+ 0/0]
P.14	OK	OK	12/14, 6/6, [+ 0/0]	9/11, [+ 7/0]
P.15	idle: too low, busy: too low	No communication	No communication	No communication

NOTE:

- No additional shorts detected other than the implemented ones.
- Many undesired opens in the analogue paths, X confirmed assembly problems.
- *Two opens (always the same ones) cannot be detected due to the design issue.

Y hybrids - evaluation results

- 14 hybrids from vendor Y were produced and tested
- Execution of all test methods ~42 s/hybrid, 100% repeatability and accuracy*

Y PS-MCK test summary table.

Hybrid ID	Current consumption [AVG: 105.4mA / 151.5mA]	Data links and config. registers diagnosis	Analogue shorts detection mutual, to GND, [+ additional]	Analogue opens detection implemented [+additional]
1. 5 T	OK	OK	OK	9/11 + 0/0
2. 5 C	OK	OK	OK	9/11 + 0/0
3. 1 U	OK	OK	OK	9/11 + 0/0
4. 4 A	OK	OK	OK	9/11 + 0/0
5. 4 P	OK	OK	OK	9/11 + 1/0
6. 4 J	OK	OK	OK	9/11 + 0/0
7. 0 Q	OK	OK	OK	9/11 + 0/0
8. 4 C	OK	OK	OK	9/11 + 0/0
9. 7 W	OK	OK	OK	9/11 + 0/0
10. 1 T	OK	4 R/W/T errors (I^2C) single retry	OK	9/11 + 0/0
11. 1 R	OK	OK	OK	9/11 + 0/0
12. 0 S	OK	12 R/W/T errors (I^2C) single retry	OK	9/11 + 0/0
13. 4 D	OK	OK	OK	9/11 + 0/0
14. 4 F	OK	OK	OK	9/11 + 0/0

NOTE:

- There were no additional shorts detected other than the implemented ones. All implemented shorts were found.
- *Two opens (always the same ones) cannot be detected due to the design issue.

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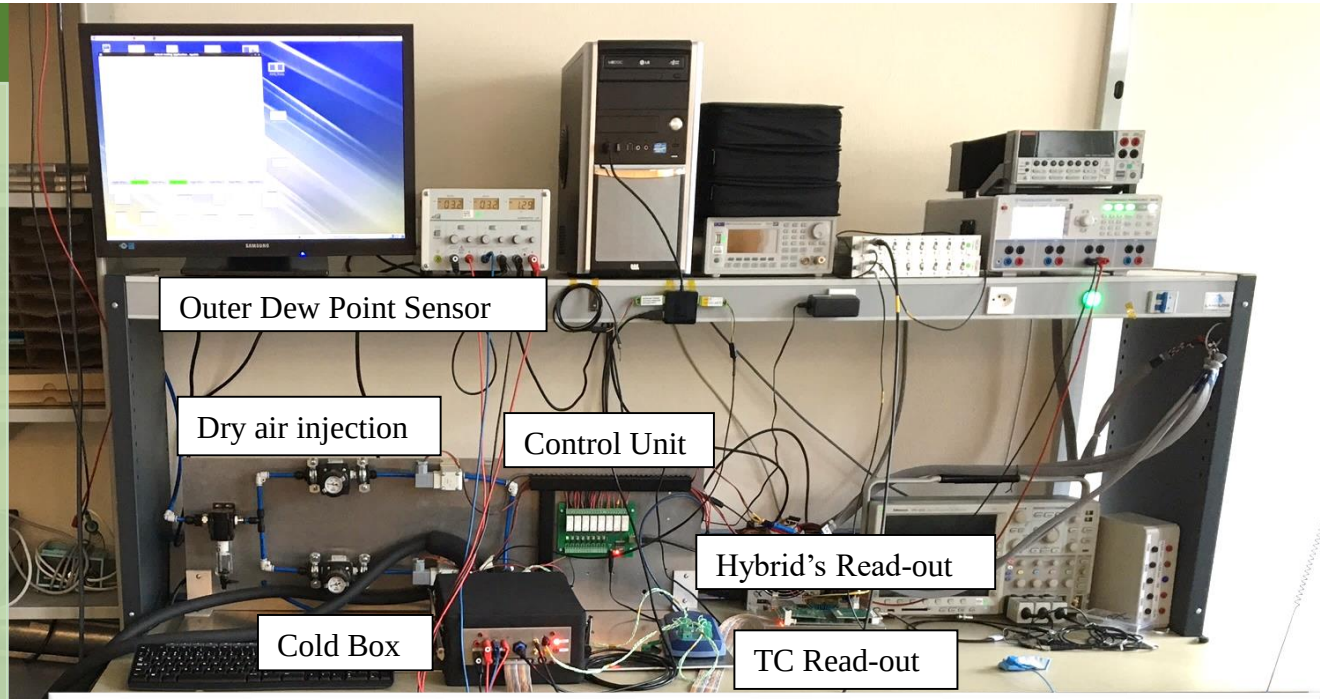
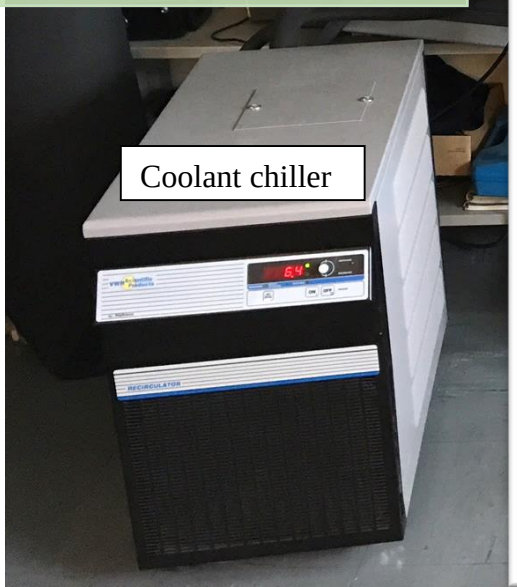
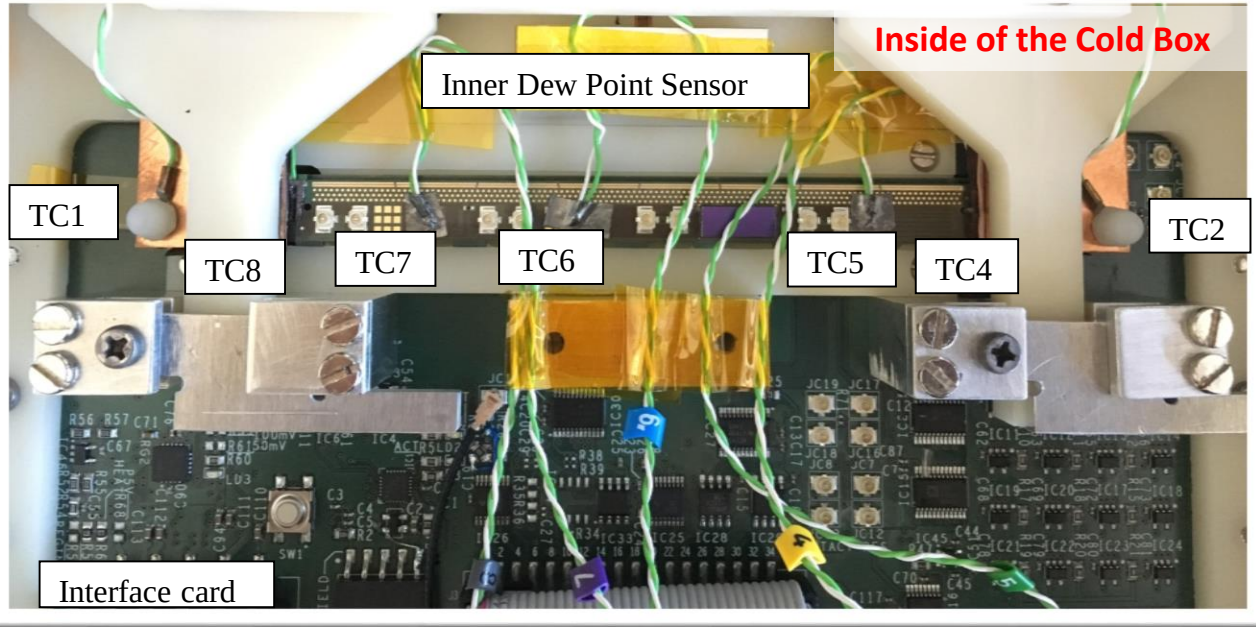
Cold Test Setup

Re-test in cold:

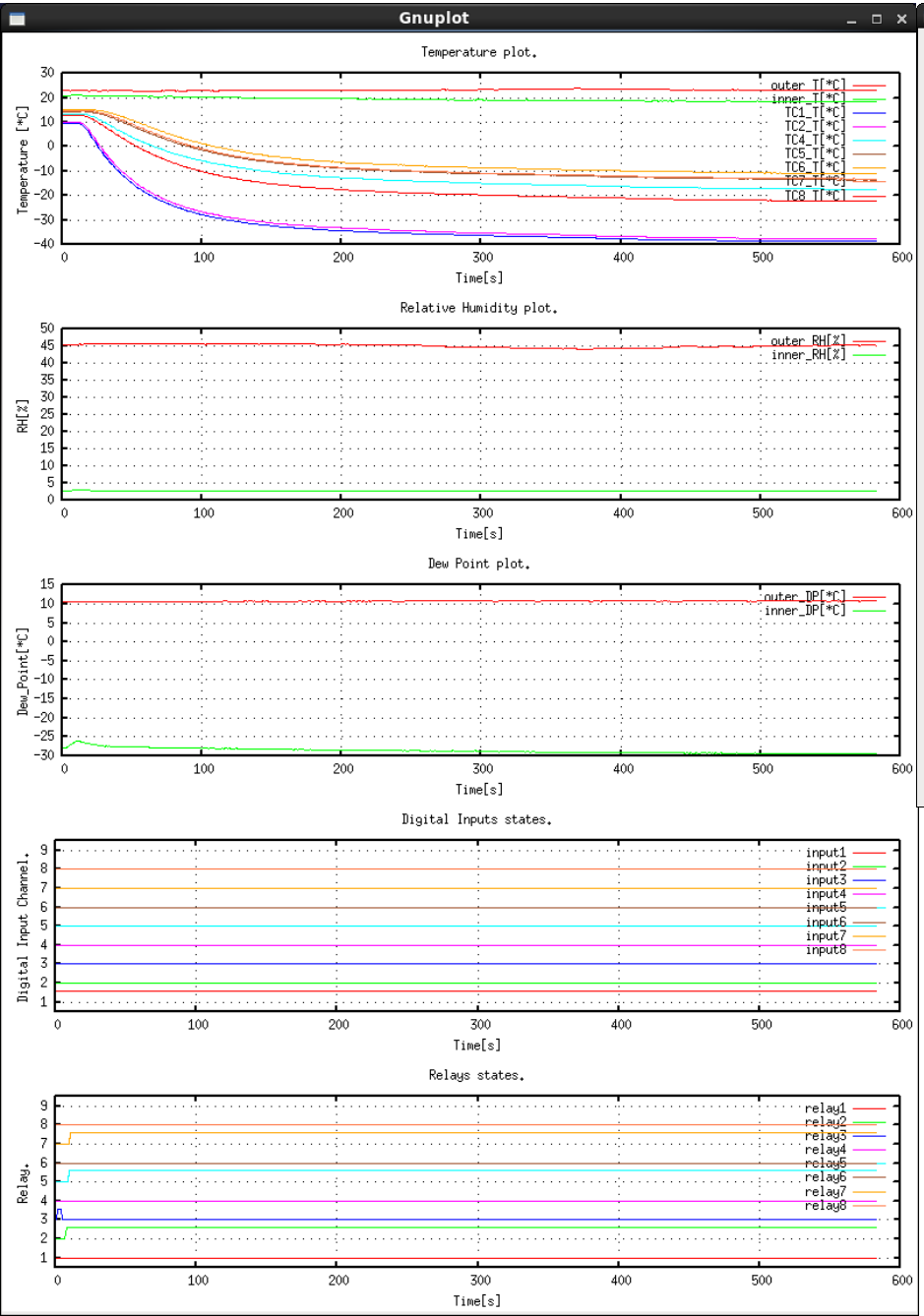
- Hybrid's operation at planned coolant temperature in the detector (-35°C),
- Validation of test methods at low temperature,
- Study on the impact of the temperature on the detectability of defects.

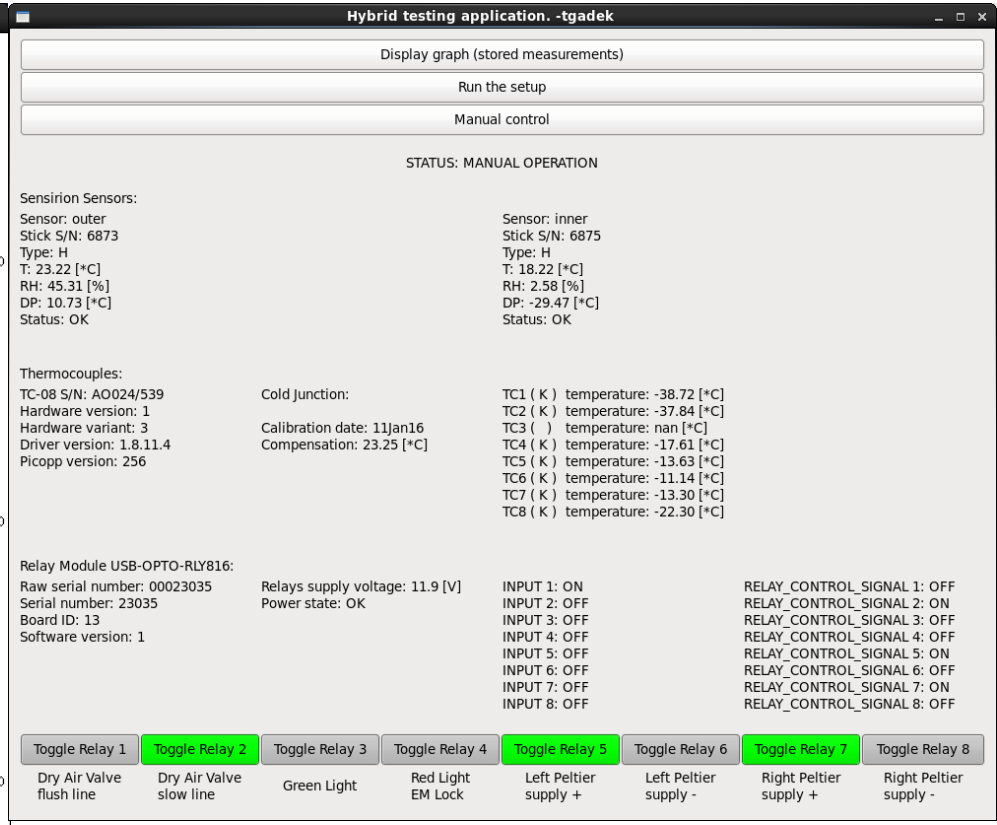




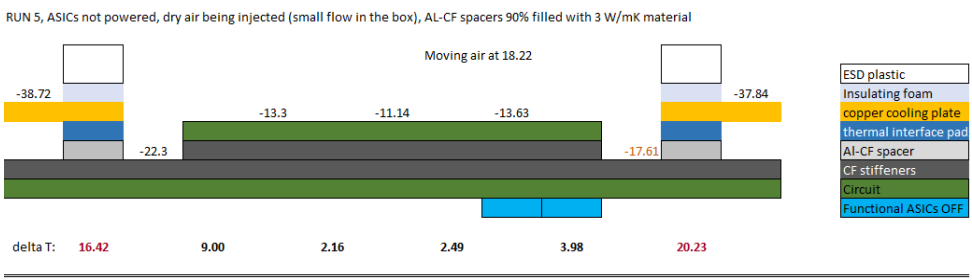


Cold Test Setup – control software





One of the first runs with the validation hybrid:



Note: T < DPT (unsafe operation)

Summary

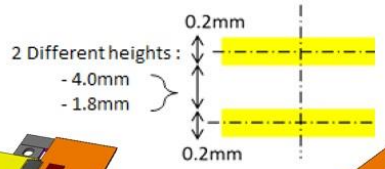
- 30,000 FEHs required for CMS Outer Tracker Upgrade.
- Several test methods proposed for optical inspection and active testing.
- 28 hybrids with implemented failure modes were delivered by 2 vendors.
- Quality control was able to successfully detect the implemented flaws.
- Test methods are reliable.
- A prototype cold box is being constructed to conduct tests at low temperature.
- First tests at low temperature gave identical outcome as the room temperature ones.

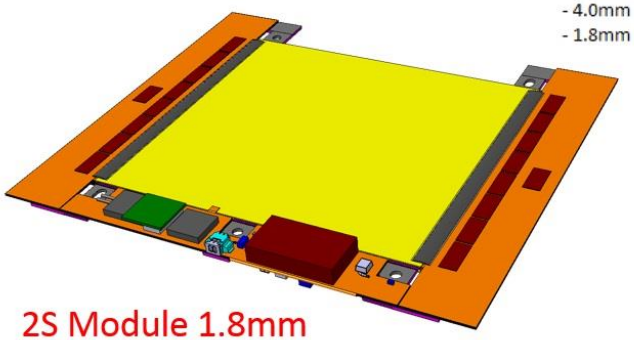

рахмат
danke
謝謝
ngiyabonga
teşekkür ederim
spas
Баярлалаа
mersi
kia ora
barka
welalin
tack
mahalo
tapadh leat
спасибо
faafetai lava
vinaka
спасибі
blagodaram
dank je
misaotra
matondo
paldies
grazzi
kiitos
dankie
nanni
nandri
dhanyavad
thank you
gracias
хвала
asante
manana
obrigada
tenki
bedankt
bayarlalaa
gràçie
hvala
mauruuru
köszönöm
dankon
ačiū
akun
enkosi
djiere dieuf
tau
mochchakkeram
murakoze
дякую
mamnun
chokrane
dziękuję
chnorakaloutioun
gratias ago
gràcies
sulpáy
go raibh maith agat
sobodi
dėkuji
sagolun
sukriya
kop khun krap
taiku
obrigado
arigatô
takk
dakujem
trugarez
mèsi
didi madloba
ありがとう
najis tuke
tanemirt
grazie
terima kasih
rahmet
kam sah hamnida
rahmat
dhanyavadagalu
shukriya
mercé
мерси
diolch
ευχαριστώ
তোমাকে ধন্যবাদ
감사합니다
xièxie
merci

Time for YOUR QUESTIONS

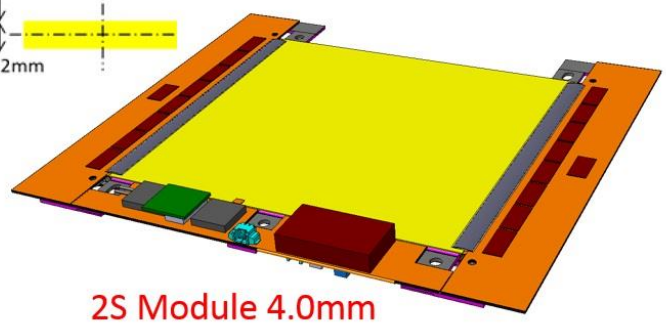
Backup slides

2S : Strip-Strip Module





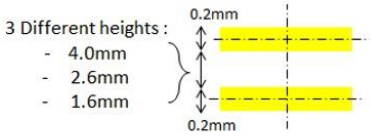
2S Module 1.8mm

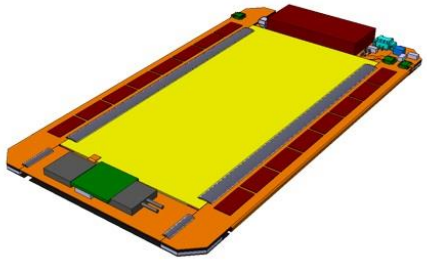


2S Module 4.0mm

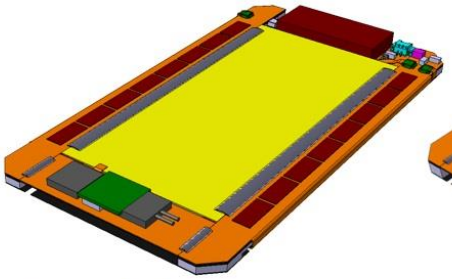
4,064 5-centimeter long silicon strips per module

PS : Pixel-Strip Module

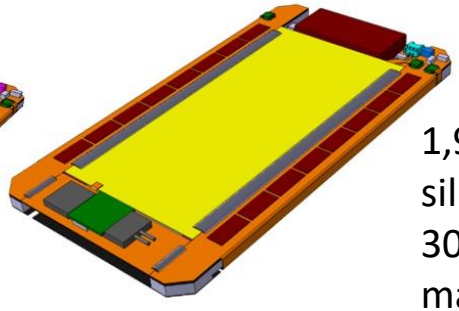




PS Module 1.6mm

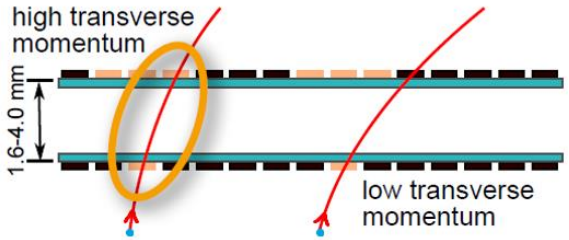


PS Module 2.6mm



PS Module 4.0mm

1,920 2.5-centimeter long silicon strips
30,720 1.4-millimeter long macro pixels per module

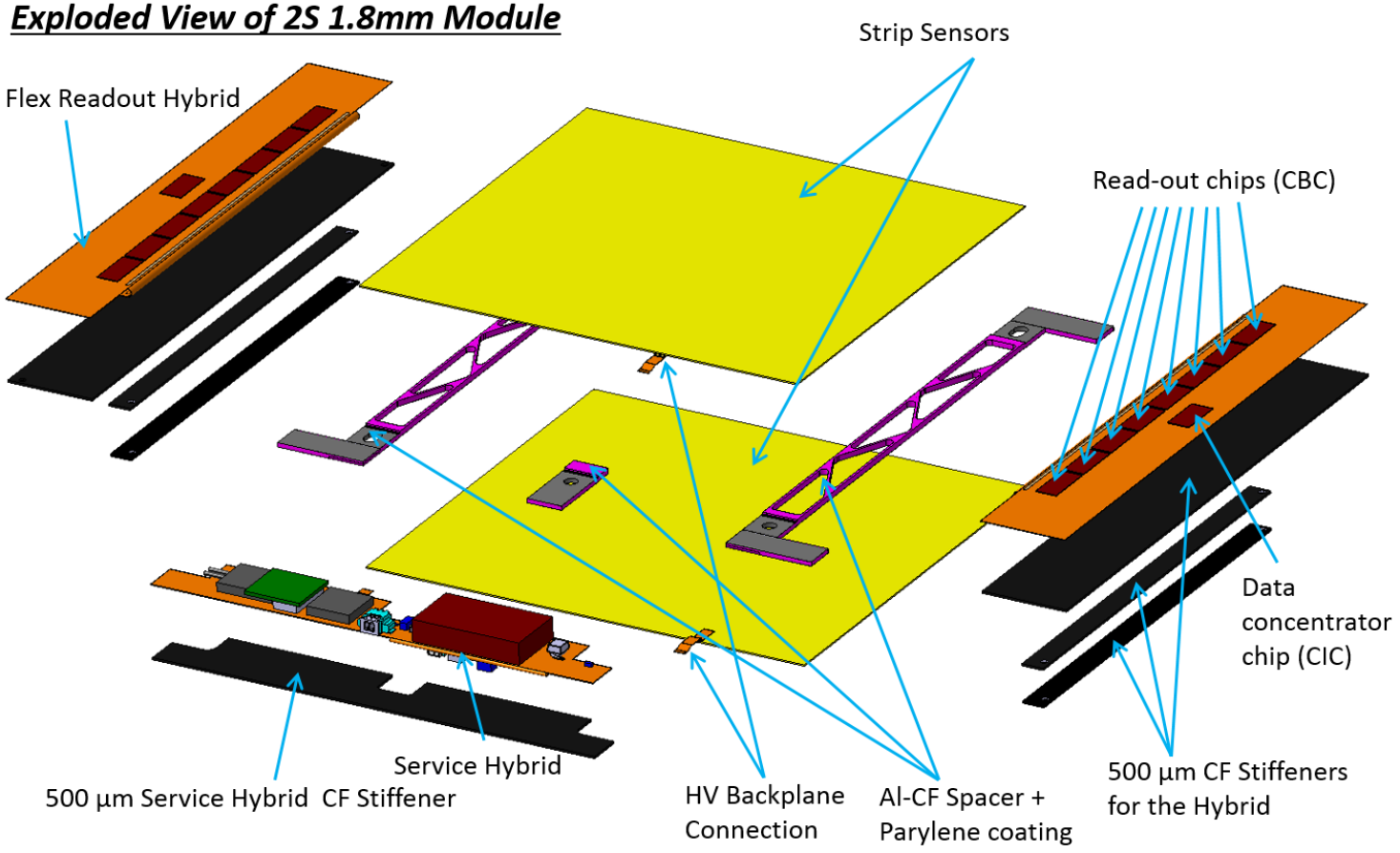


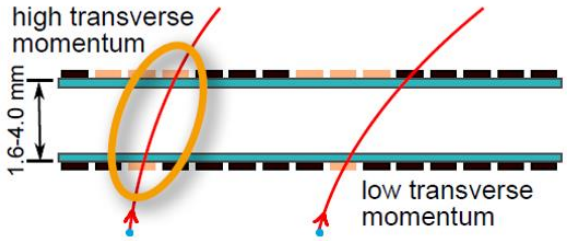
	2S Modules		PS Modules		
	1.8mm	4.0mm	1.6mm	2.6mm	4.0mm
TBPS	.	.	888	1516	504
TB2S	4464	.	.	.	.
Endcap	2976	984	.	.	2800

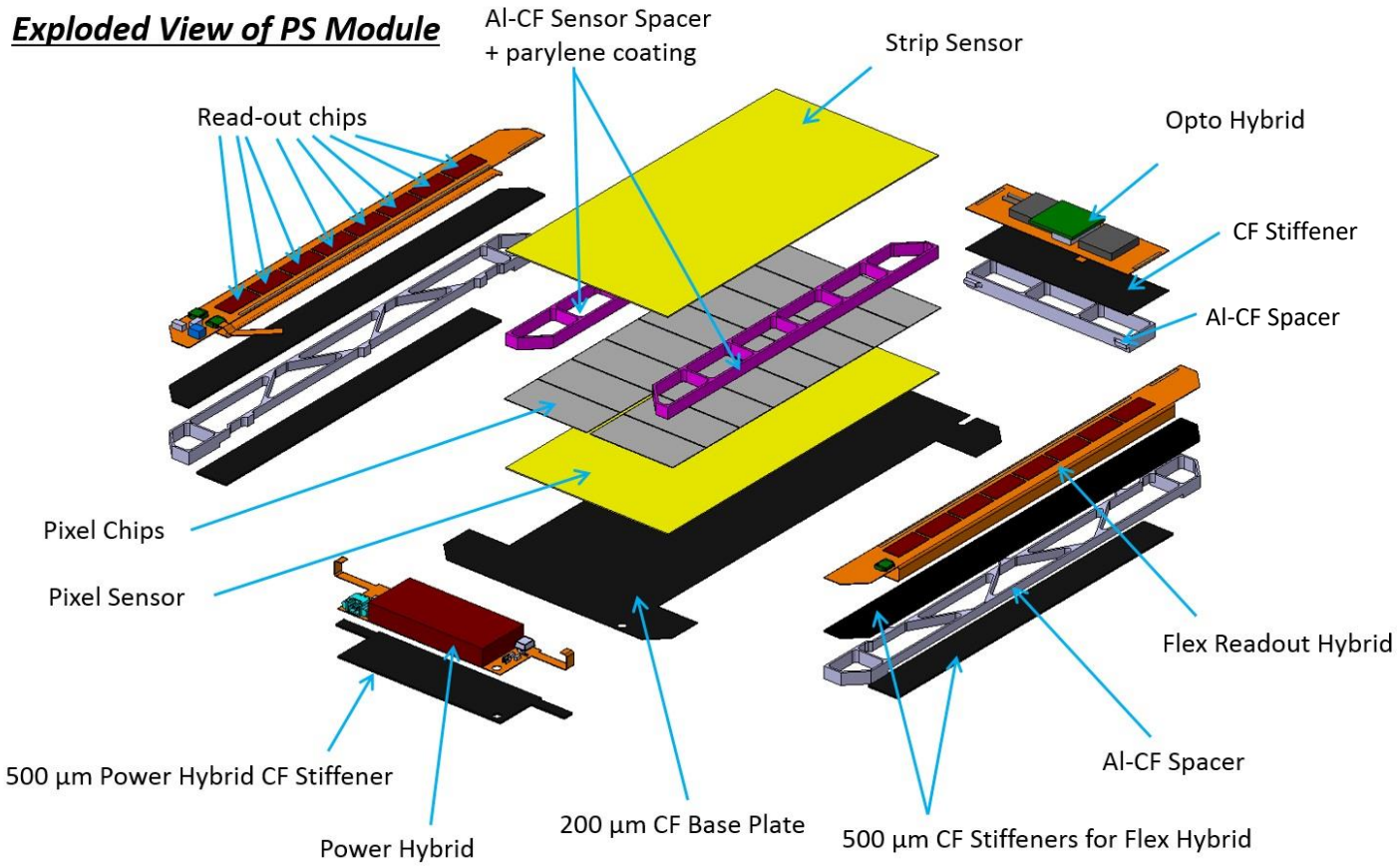
Total 2S Modules	**8424**
Total PS Modules	**5708**

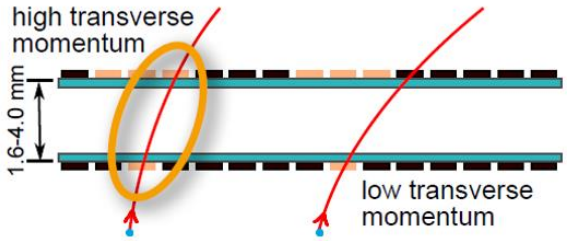
Total Modules	**14132**
Total Hybrids	**28264**

Exploded View of 2S 1.8mm Module





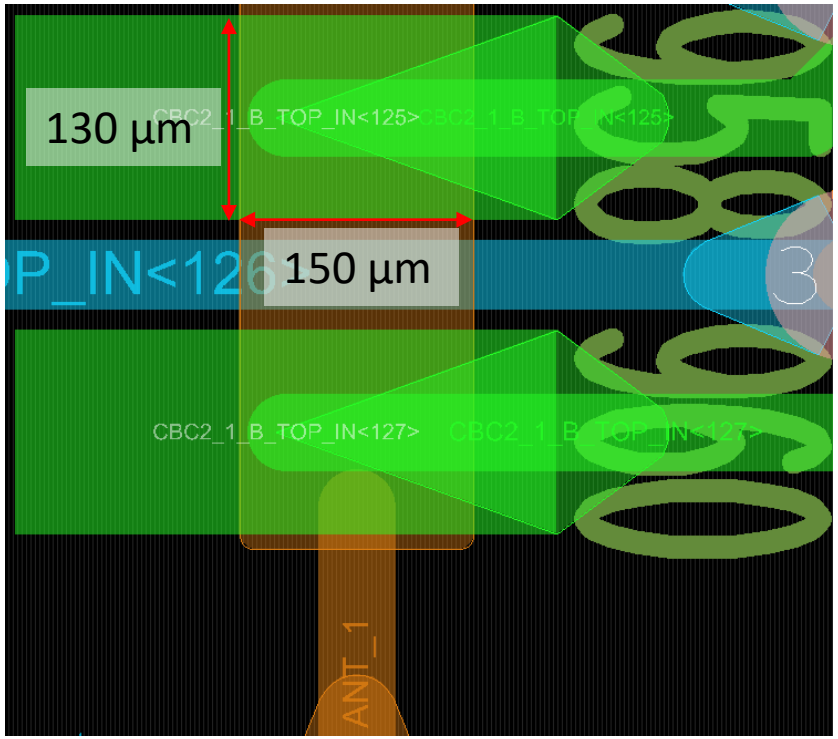

Exploded View of PS Module
Al-CF Sensor Spacer
+ parylene coating
Strip Sensor
Read-out chips
Opto Hybrid
CF Stiffener
Al-CF Spacer
Pixel Chips
Pixel Sensor
Flex Readout Hybrid
Al-CF Spacer
500 µm Power Hybrid CF Stiffener
Power Hybrid
200 µm CF Base Plate
500 µm CF Stiffeners for Flex Hybrid


high transverse
momentum
1.6-4.0 mm
low transverse
momentum

The charge injection pads are routed on the adjacent layer to the wire bond pads.

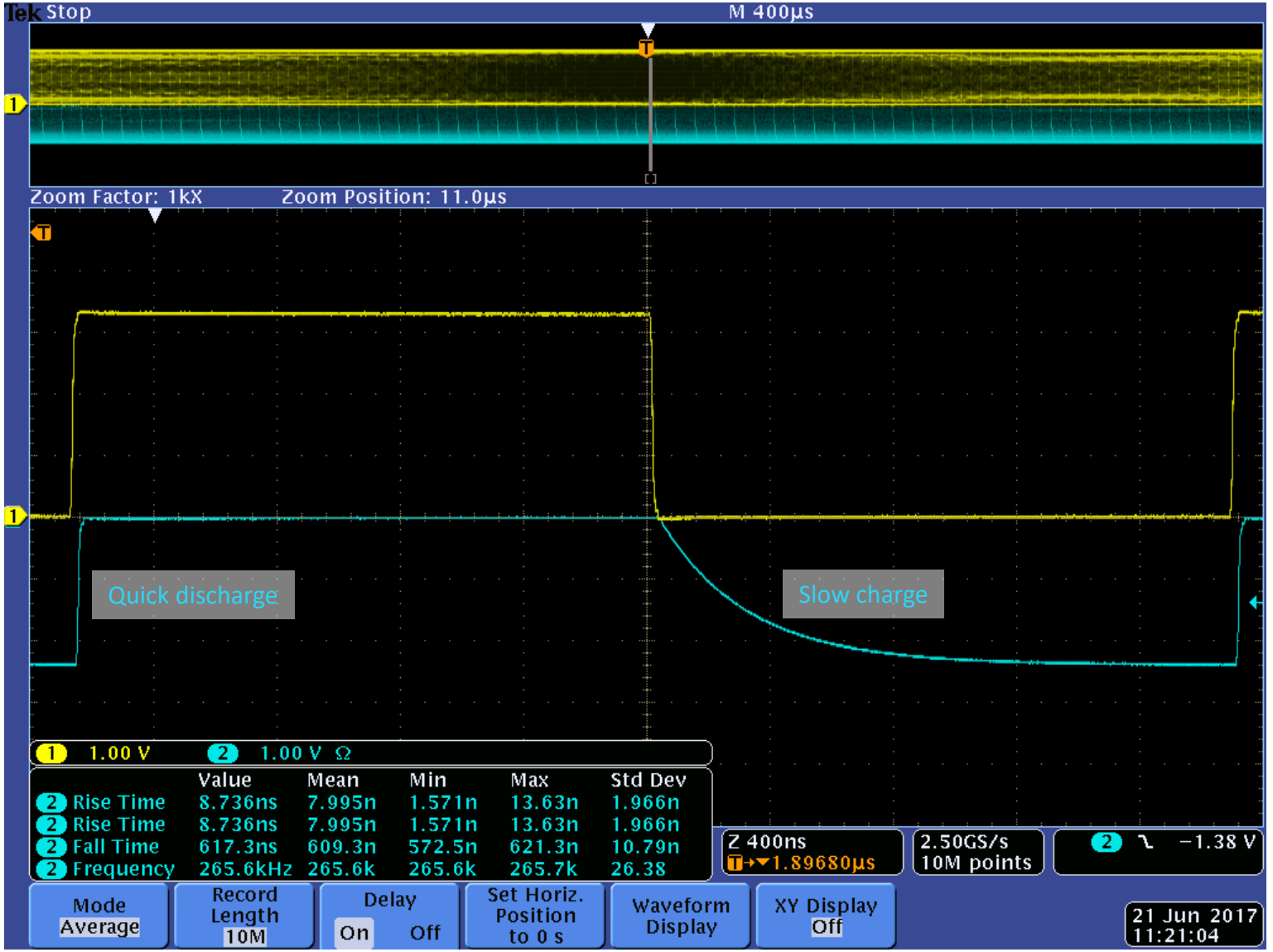
First order approximation as a parallel plate capacitor:

- Y hybrids: 20 µm spacing between the copper layers (dielectric constant ~2.9)
- Estimated capacitance w/o edge effect ~25 fF, max charge ~62.5 fC
- Estimated capacitance with edge effect ~32.7 fF, max charge ~81.75 fC
- Discharge time (from max voltage) ~8 ns
- Programmable pull-up: 10 bit steps over the range from -2.5 V to 2.5 V
- X hybrids: 15um spacing, w/o edge effect ~33.4 fF, with edge effect ~40.9 fF, max charge ~102.25 fC



Trigger signal

Injection line signal



Time consumption of the active test methods:

- 0.1 s • idle and peak current consumption
- 0 s • diagnosis of data interface together with clock and fast commands
- 5.8 s • diagnosis of configuration registers
- 0 s • diagnosis of slow control interface (I^2C)
- 31.1 s • full calibration of analogue FE channels (biases tuning per ASIC and offsets trimming for each individual channel)
- 0.8 s • post calibration data taking (distribution of noise-driven hit counts per channel)
- 2.4 s • **mapping of open analogue connections**
- 1.2 s • **mapping of shorted analogue connections**

Testing time is completely dominated by operator's manual operations and cooling

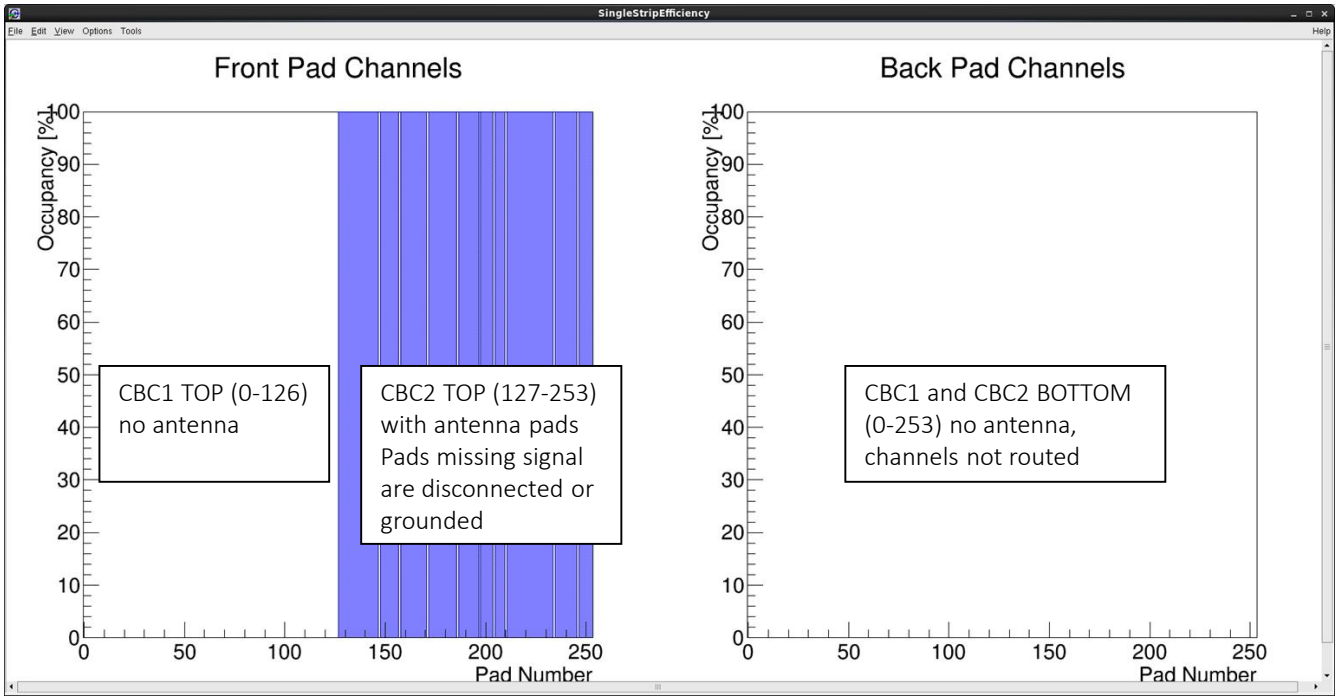
Y hybrid (0 S) analogue opens detection analysis:

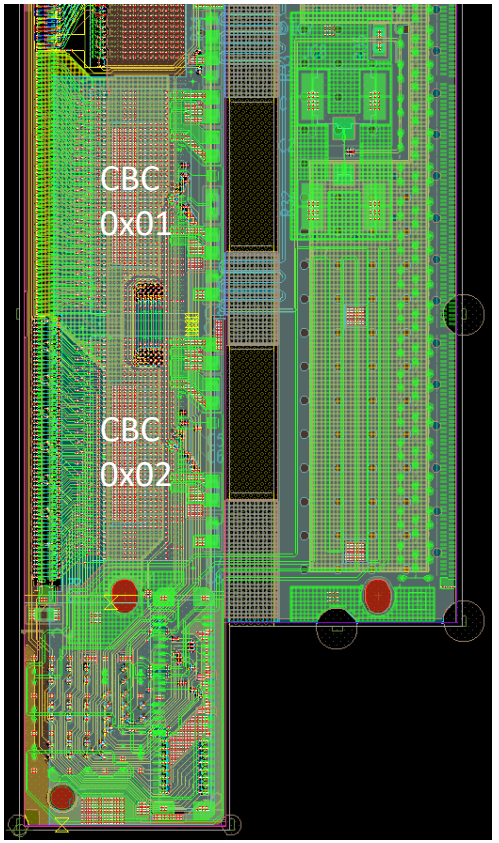
Disconnected or grounded inputs found on top side of second CBC2: 147, 157, 171, 186, 197, 204, 210, 234, 246 (in total 9)

Implemented opens in TOP side of second chip: 144, 164, 157, 234, 246, 171, 197, 210 (8)

Implemented shorts to GND: 147, 186, 204 (3)

NOT FOUND: 144, 164 (correspond to channels 18 and 38 of CBC 0x02) FOUND EXTRA: none



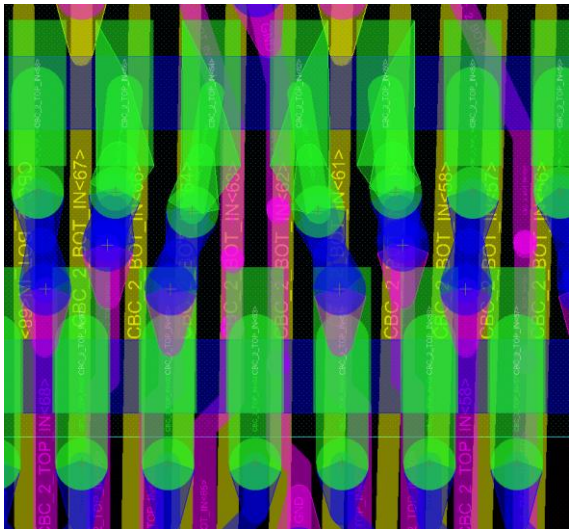


Signal injection cycle

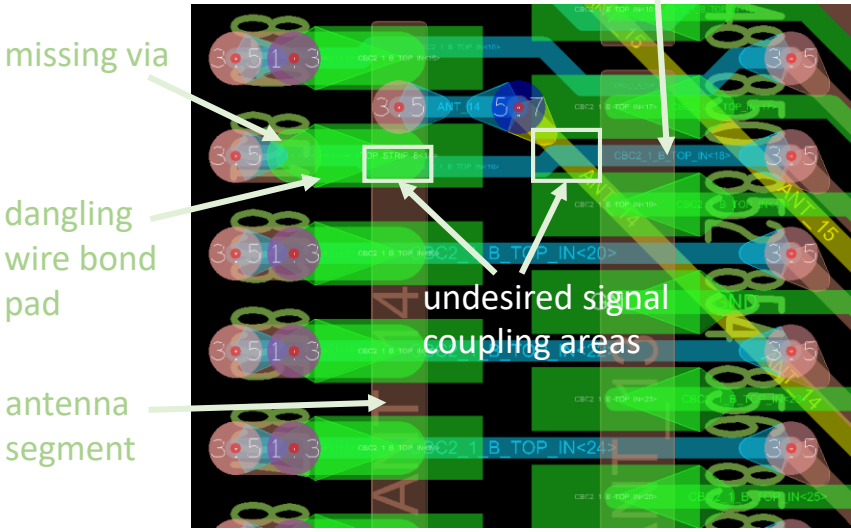
- The problem of 2 not found opens has been investigated.
- Both opens are implemented by a removal of via near wire bond pads.
- By design there is a coupling from an antenna pad and its interconnecting trace to the channel's trace
- With embedded antenna we cannot detect these type of failures in PS-MCK
- On 2CBC3 this area is routed differently

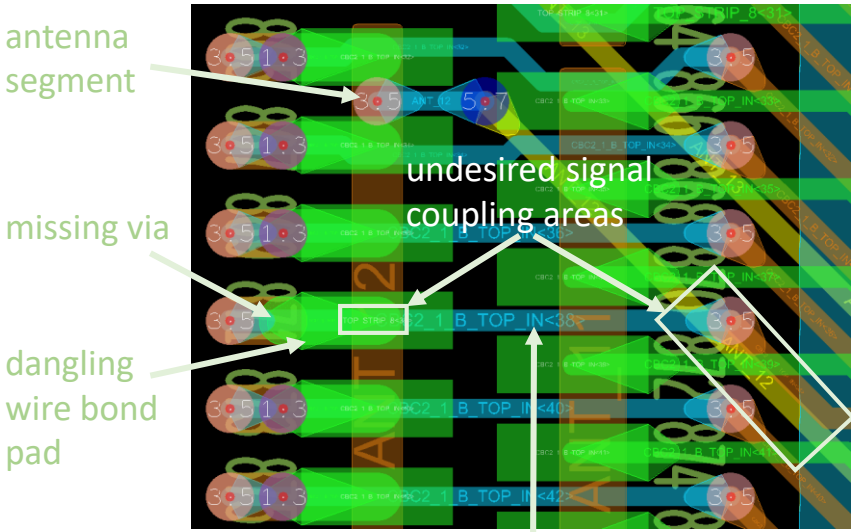
2CBC3 routing near wire bond pads:

- antenna is not segmented = no intermediate segment connection
- Input channel routing does not go around corresponding antenna pad



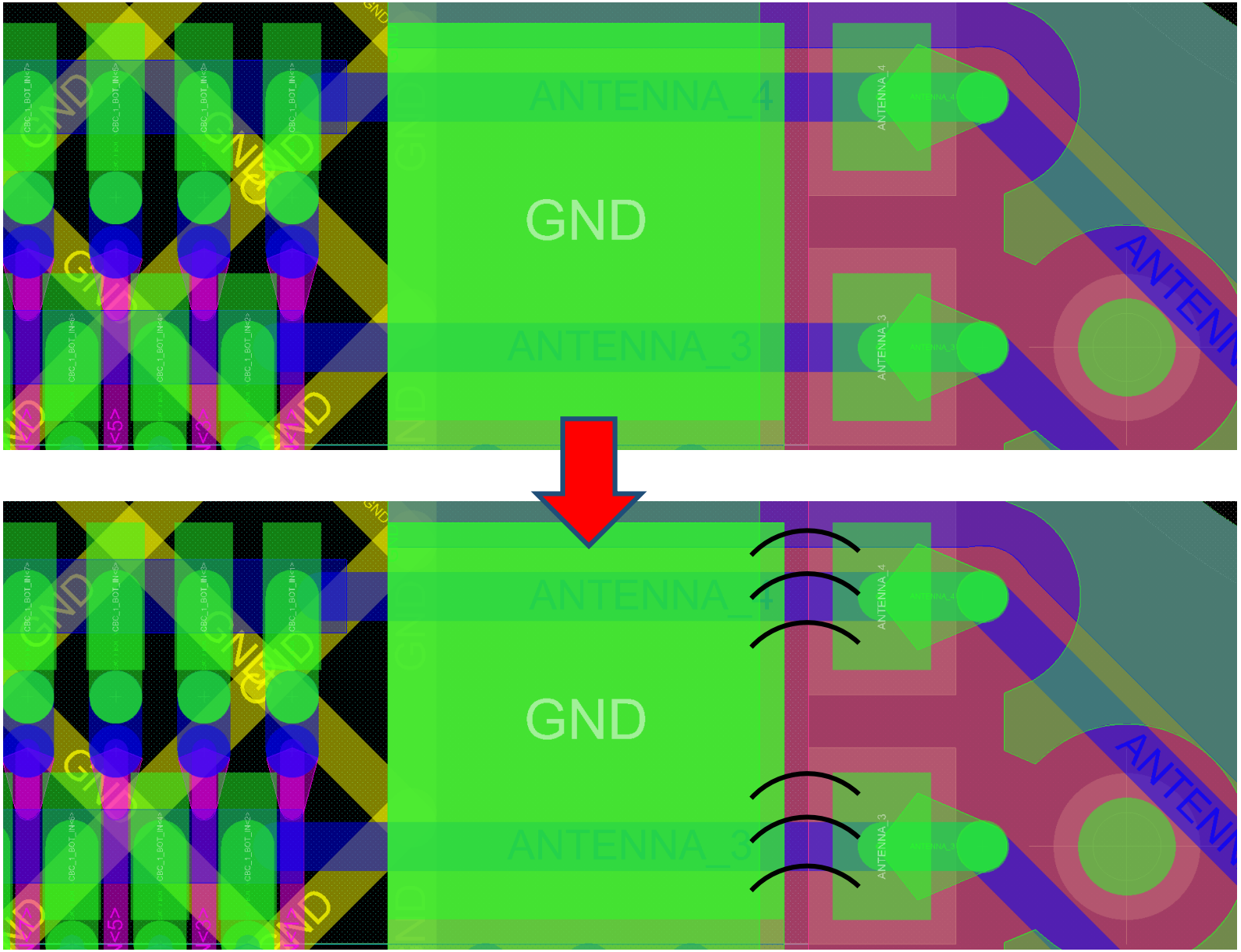
Interconnect to ch. 18 of CBC 0x02





Interconnect to ch. 38 of CBC 0x02

Grounding of antenna pads after testing



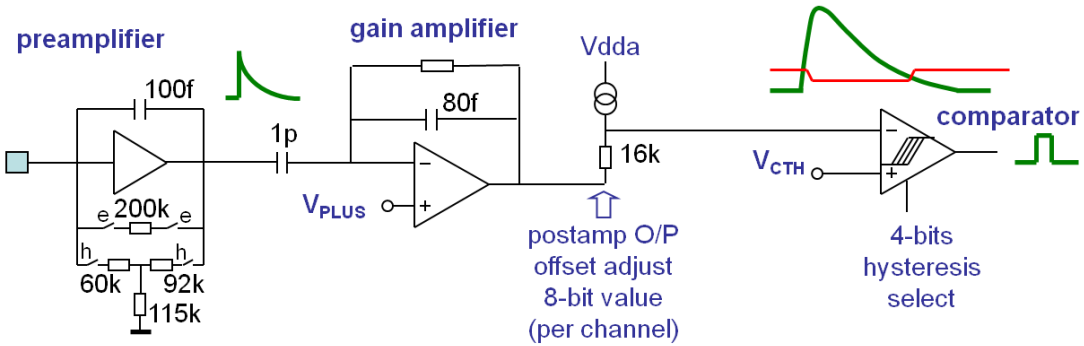
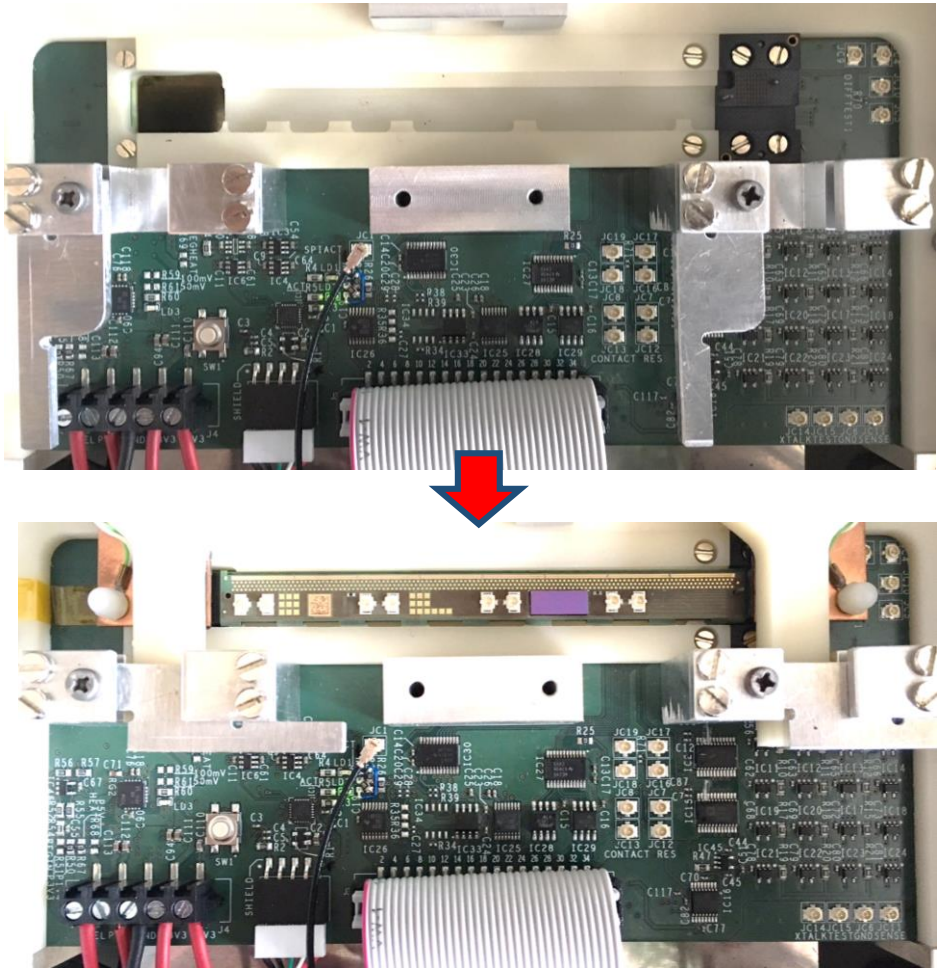
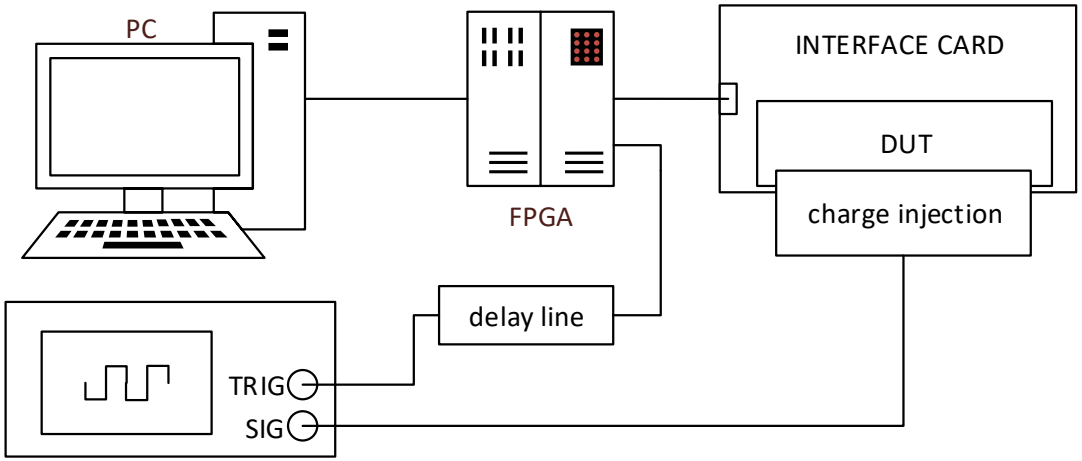


Figure 3. CBC2 Analogue Front End

Interface card for the cold box




PC
FPGA
INTERFACE CARD
DUT
charge injection
delay line
TRIG
SIG

X PS-MCK hybrids - summary table of active tests.

Hybrid ID	Current consumption [AVG: 105.5mA / 151.5mA]	Data links and config. registers diagnosis	Analogue shorts detection mutual, to GND, [+ additional]	Analogue opens detection Implemented, [+ additional]	OVERALL RESULT
P.1	idle: OK, busy: OK	Links: OK, registers: OK	9/14, 4/6, [+ 0/0] too many missing shorts	9/11, [+ 53/0]	NEG.
P.3	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
P.4	idle: AVG + 5.59%, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 1/0]	POS.
P.5	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 8/0]	POS.
P.6	idle: OK, busy: OK	Links: OK, registers: OK	13/14, 6/6, [+ 0/0]	9/11, [+ 3/0]	POS.
P.7	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
P.8	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
P.9	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
P.10	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
P.11	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
P.12	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
P.13	idle: OK, busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
P.14	idle: OK, busy: OK	Links: OK, registers: OK	12/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
P.15	idle: AVG - 6.73%, busy: AVG - 12.67%	Fast data interface out of order	Fast data interface out of order	Fast data interface out of order	NEG.

NOTE:

- There were no additional shorts detected other than the implemented ones.
- There were many undesired opens in the analogue interconnections, assembly problems confirmed by X.
- *Two opens (always the same ones) cannot be detected due to the design issue.

Y PS-MCK test summary table.

Hybrid ID	Current consumption [AVG: 105.4mA / 151.5mA]	Data links and config. registers diagnosis	Analogue shorts detection mutual, to GND, [+ additional]	Analogue opens detection implemented [+additional]	OVERALL RESULT
1. 5 T	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
2. 5 C	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
3. 1 U	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
4. 4 A	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
5. 4 P	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 1/0]	POS.
6. 4 J	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
7. 0 Q	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
8. 4 C	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
9. 7 W	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
10. 1 T	idle: OK busy: OK	4 R/W/T errors (I^2C) single retry	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
11. 1 R	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
12. 0 S	idle: OK busy: OK	12 R/W/T errors (I^2C) single retry	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
13. 4 D	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.
14. 4 F	idle: OK busy: OK	Links: OK, registers: OK	14/14, 6/6, [+ 0/0]	9/11, [+ 0/0]	POS.

NOTE:

- There were no additional shorts detected other than the implemented ones. All implemented shorts were found.
- *Two opens (always the same ones) cannot be detected due to the design issue.