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A Combined Versatile Platform for Silicon Strip Hybrids Reliability Assessment

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A unified platform combining a low noise 64-channel power supply with environmental monitoring and a high data rate transmission system, rated up to 1.2 Gbps/sec, has been developed for commissioning of the ATLAS ITk silicon strip hybrids. The power supply with 10mV peak-to-peak noise, implements 3kV isolation and software control. Humidity, temperature, voltage and current are monitored for all channels through I2C interface. Data paths are organized in a pyramid-like, fully programmable layout, enabling use of 8 LVDS lines for accessing all 64 data inputs. The system has been optimized to fit in a single 6U VME type C crate.

Summary

ATLAS ITk features strip system with 100 million readout channels and several custom ASICs. Burn-in tests are envisioned as a part of hybrid testing procedure in order to catch "infant mortality"of the ASICs. Implementing such tests requires a system providing all available services for DUTs. A multichannel compact architecture is presented, embedding precise low voltage powering, environmental control and data read-out transmission for 64 modules.

An autonomous 1.5V, 10mV peak-to-peak noise power supply is implemented for each channel. The 1.5A max current output in combination with the 3kV isolation provides 50% margin in respect or required power and medical grate protection for the sensitive equipment. Voltage and current are monitored at the receiving end while a passive humidity sensor in combination with a double channel ADC are included. Temperature is monitored through an NTC in conjunction with a precision current source and a configurable gain high precision amplifier directed to the second ADC input. Configuration, remote enable and data readout tough I2C interface is instrumented for each channel individually.

Data transmission is organized in three layers of high speed differential octal switches. Using a pyramidal fully user programmable architecture, the 64 differential inputs can be probed by 8 DAQ lines. The I2C structure configurability, enables any of the inputs to be connected to any of the available output lines while internal use of CML signaling ensures high bandwidth. While internal switching can be achieved up to 2.5Gbps/s, elements related to the LVDS standard limit data rates to 1.2Gbps/s. A universal clock is distributed to all channels while 32 direct differential lines are made available for specific functions. Pre-emphasis and equalization is implemented in all differential switching stages while SLVS to LVDS transceivers are introduced in the final stage of the control lines output. An intricate attention was devoted to noise reduction and signal referencing with single ground paths and high frequency filtering elements.
The system is organized in a single 6U VME crate and comprises of three distant autonomous elements: the individual channel power and environmental boards, power and data transmission mother-boards combining 8 power boards and the backplane, implementing high rate data switching and transmission. To accommodate higher powering requirements, the possibility of combining powering boards is implemented via I2C programming. Although this technique reduces the number of available channels by half, it allows a maximum 3A current per channel. The compactness of the system is enhanced by the single common 12V supply voltage for all elements allowing use of a commercial high power VME power supply. Finally, the integrated FMC connector on the backplane enables the addition of an FPGA daughter board of user choice simplifying integration, upgradability and compatibility with different platforms.

Overall, the high versatility of this combined powering, data transition and monitoring system, in combination

with low electronic noise, precision power supplies and reconfigurable data switching architecture, makes it a characterization platform compatible with any multichannel detector setup. The compact nature and upgradability facilitates integration and provides enhanced design freedom to the end user.

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