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Radiation Hardness Studies and Evaluation of SRAM-Based FPGAs for High Energy Physics Experiments

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Outline

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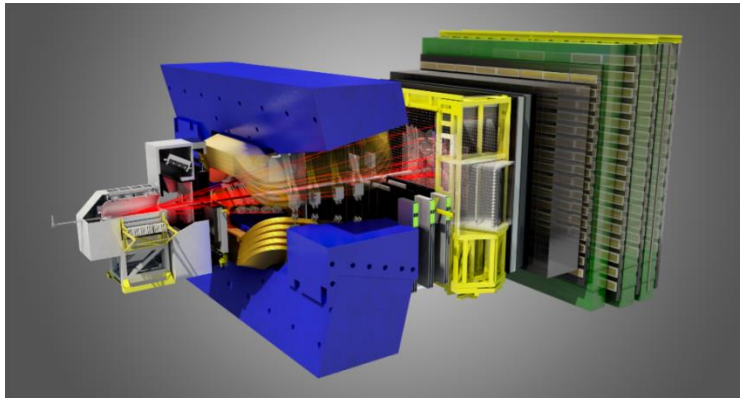
- Protons Irradiation Results
- X-Rays Irradiation Results
- Conclusions
- Future developments

Introduction-LHCb Upgrade

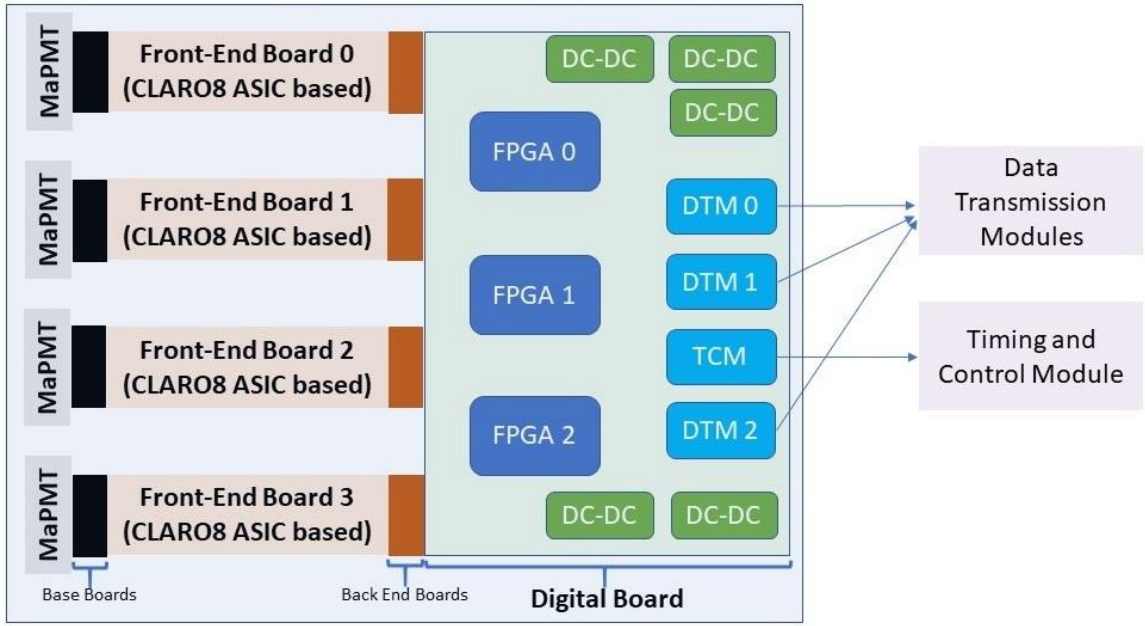


LHCb detector

https://lhcb-public.web.cern.ch/lhcb-public/

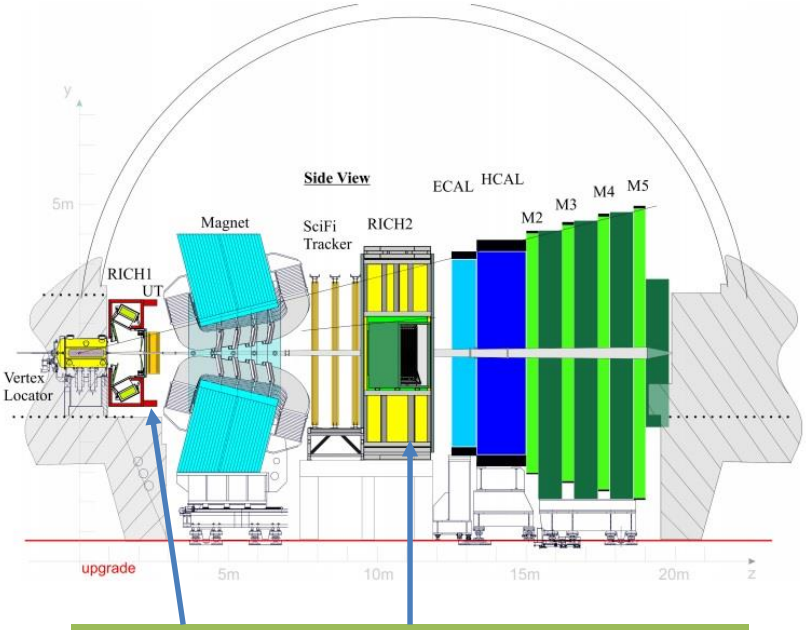
- During the second LHC long shutdown (2019-2020) the entire LHCb detector will be upgraded to operate at higher luminosity;
- The LHCb RICH sub-detectors upgraded with a 40 times increased readout rate;
- For the Digital Boards an SRAM based FPGA from Kintex-7 family has been proposed: ***XC7K70T-FBG676***;
- Device Under Test: ***XC7K70T-FBG484C6.*** (More info)

Elementary Cell (typical architecture simplified)
8 x 64 readout channels (each digital board can read 8 MaPMTs signals)



The LHCb Collaboration, *LHCb Particle Identification Upgrade Technical Design Report*, available at: link.

Radiation Environment



RICH 1 and RICH 2 sub-detectors

- FLUKA simulation --> Total Ionizing Dose (TID) and neutron equivalent for 50 fb^{-1};
- Worse case scenario values are expected in RICH 1 sub-detector, because of its position with respect to primary collision and single arm spectrometer;
- FPGA exposed to a maximum of 200 krad (2 kGy) over the Upgrade phase.

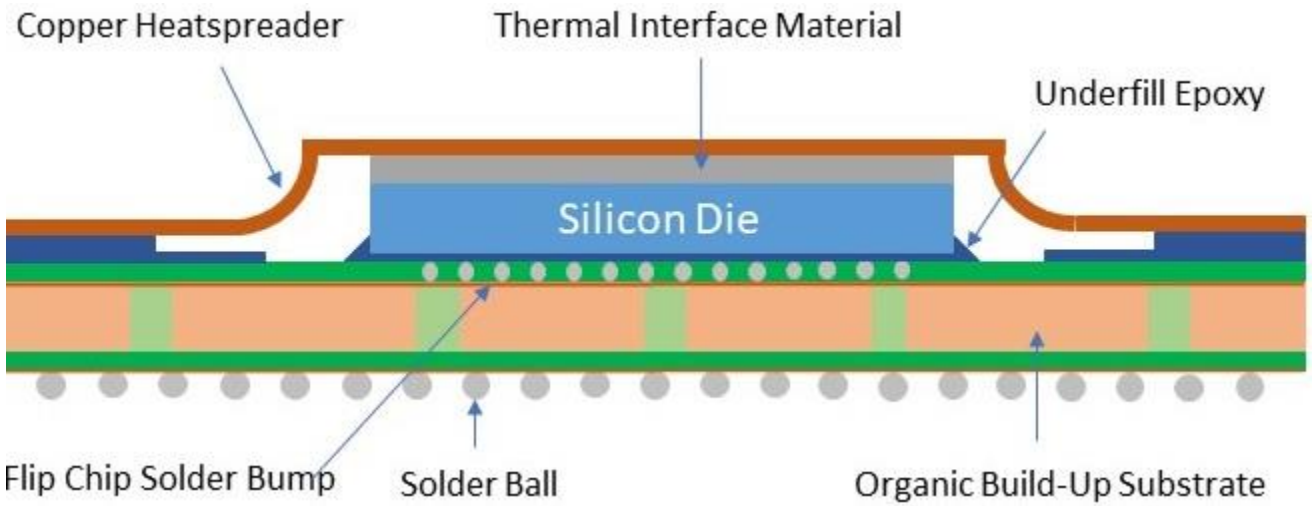
Framework TDR for the LHCb Upgrade: Technical Design Report

Region	TID [krad]	Neutrons: 1 MeV n_{eq} [cm^{-2}]	Hadrons: >20 MeV [cm^{-2}]
RICH 1	200	3×10^{12}	1.2×10^{12}

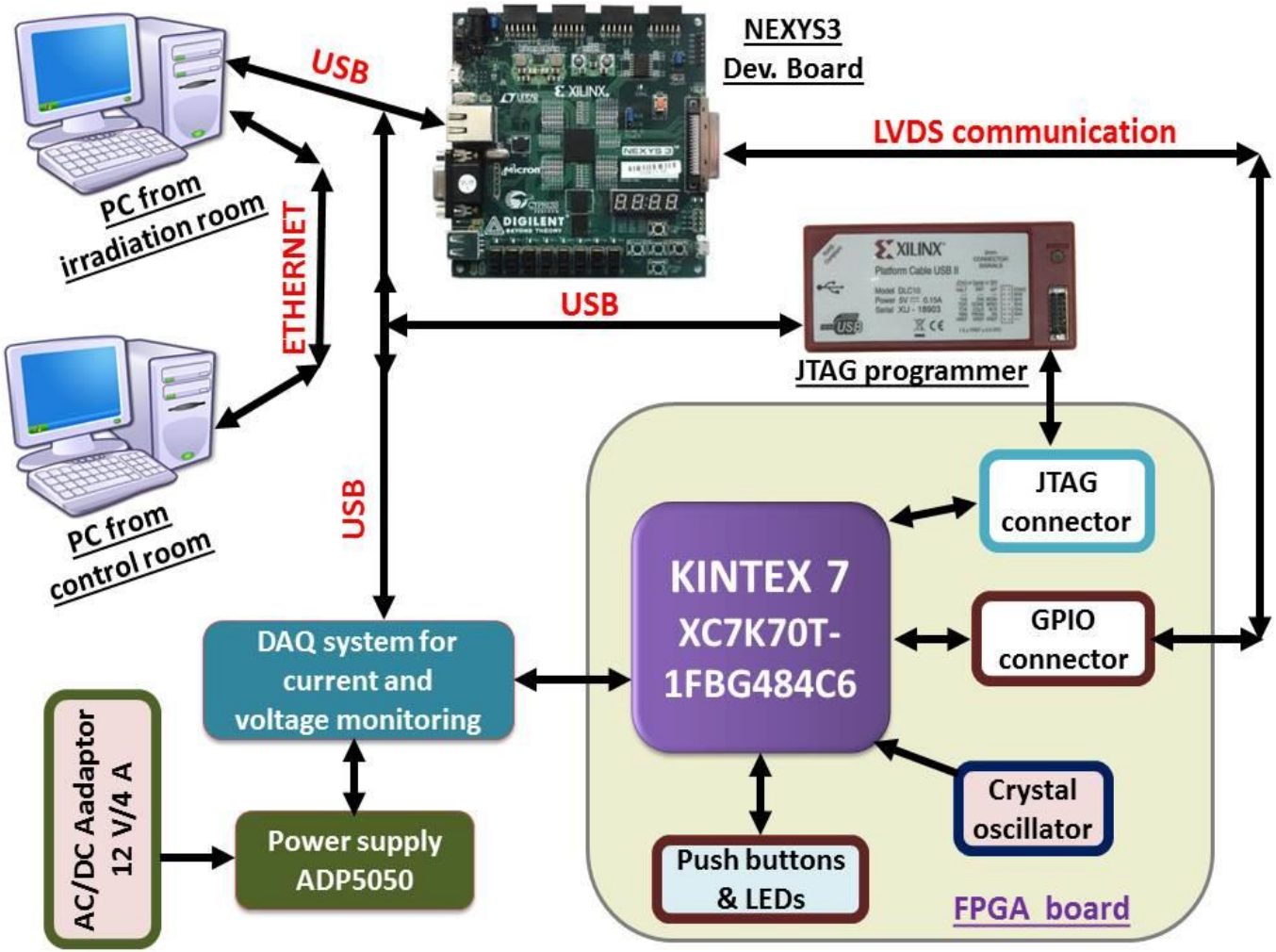
LHCb Upgraded RICH 1 Engineering Design Review Report

KINTEX-7

- SRAM FPGA family → Flip Chip design using 28 nm High-K Metal Gate technology;
- KINTEX-7 → best price/performance/watt ratio;
- In order to allow the heavy ions to penetrate the dice to the bottom active layer:
  - the FPGA package is lidless;
  - the wafer was thinned from 250 to about 60 µm (typical ^{18}O ion penetration depths of 100 µm for available beams at the laboratories from the list).
- DUTs were thinned.

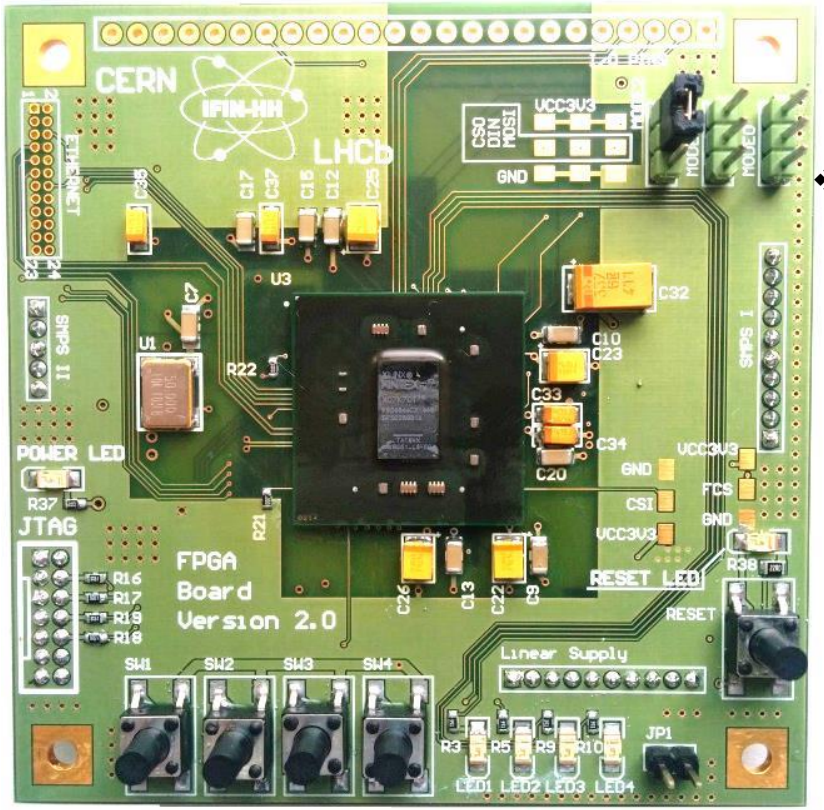


Experimental Setup



Experimental Setup

~FPGA Test Board~



Top view of the FPGA Test Board

- The DUT test board was designed considering the following test constrains:
  - Minimal external components usage just to ensure a base running;
  - No external FLASH configuration memory;
  - Reconfiguration through JTAG at each power up/cycle;
  - A single ended 50 MHz clock, for the mitigation IP CORE;
  - External clock which ranges from 500 KHz up to 12 MHz for the user logic.

http://www.xilinx.com/support/documentation/data_sheets/ds180_7Series_Overview.pdf

Experimental Setup

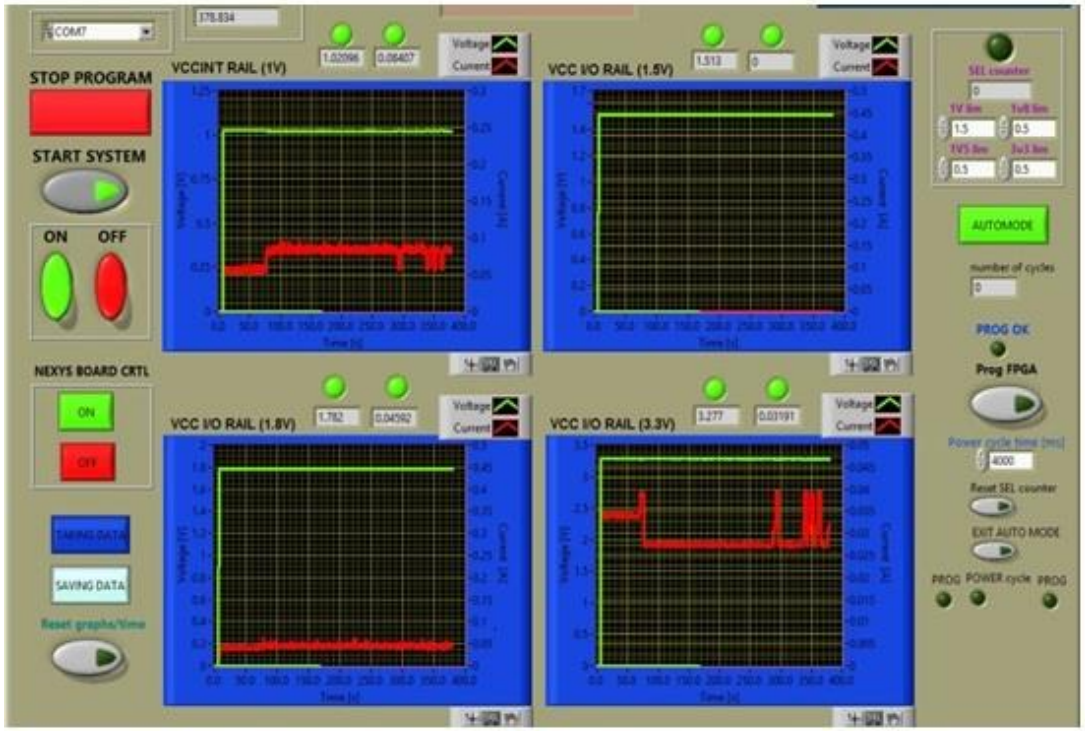
~SEM IP Core~

- Soft Error Mitigation IP Core is a special IP provided free by Xilinx and used to perform SEU detection, correction and classification for the configuration memory, CRAM;
- Typical detection latency: 25 ms;
- The error correction is an optional feature which can be done using one of the following method:
  - Correction by Repair method: ECC algorithm based and supports correction of configuration memory frames with single-bit errors; (one bit in each frame)
  - Correction by Enhanced Repair method: ECC and CRC algorithm based and supports single-bit or double-bit adjacent errors;
  - Correction by Replace method: supports correction of configuration memory frames with arbitrary errors. (external memory needed)
- Using the classification capability the user can determine if corrected errors have affected configuration memory in locations essential to the user design;
- Support error injection: with this feature the user can inject SEU in the configuration memory which is useful for establish the critical bits ratio of he user design.

https://www.xilinx.com/products/intellectual-property/sem.html

Experimental Setup

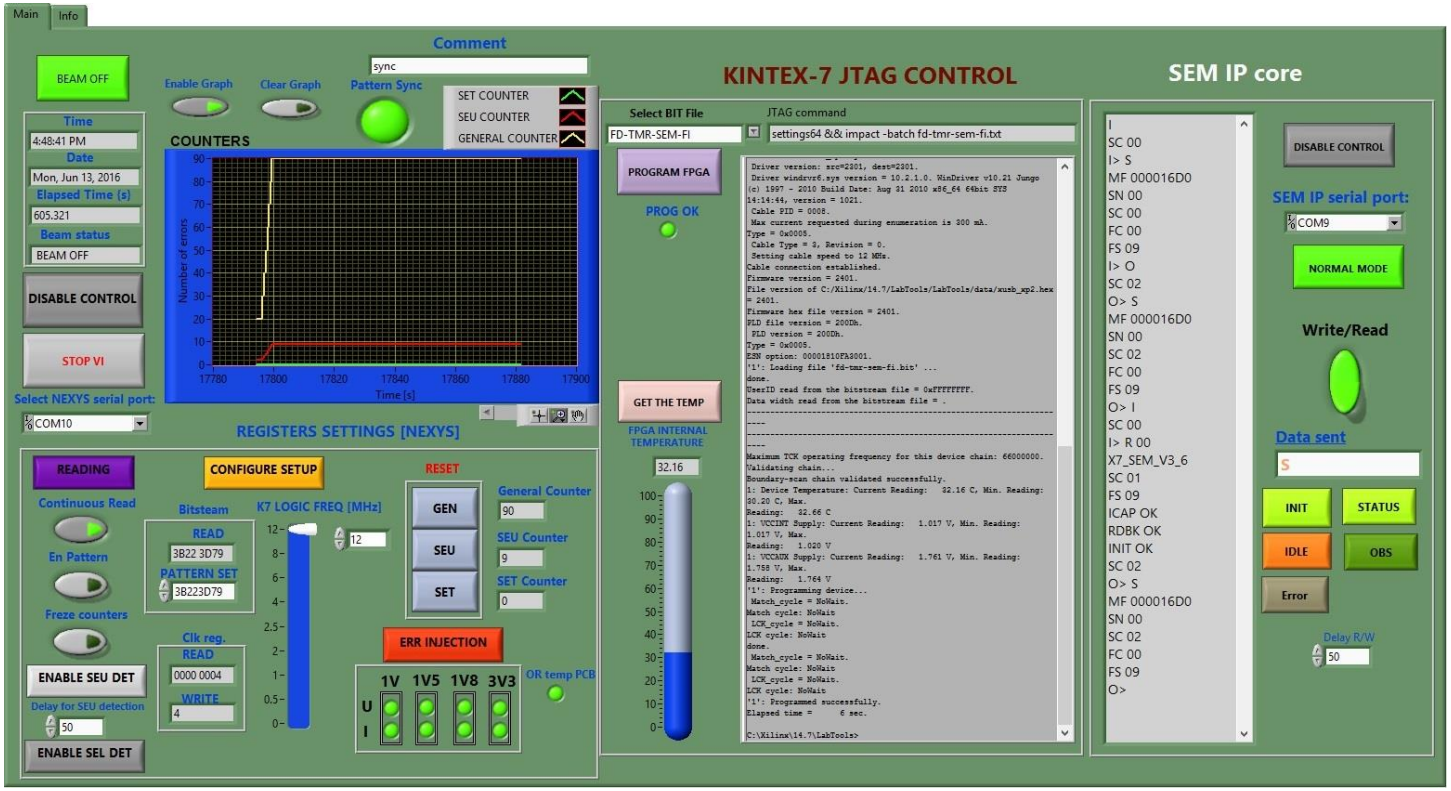
~Monitoring and Control~



- A custom DAQ system monitors the most important 4 voltage rails of the Kintex-7 FPGA;
- The LabVIEW GUI allow us to:
  - Read and plot the parameters;
  - Save the parameters in to ASCII files for offline analyses;
  - Perform power cycle for the entire FPGA or only on VCCAUX rail.
- All parameters are sampled at every 50 ms.

Experimental Setup

~Monitoring and Control~



- Allow us to reconfigure the FPGA and also to do a blind scrubbing procedure;
- We can see the SEM IP core response;
- We can control the functionality of the DUT board, by controlling its logic frequency, pattern type etc.;
- We can read the BRAM content and also we compared it with a golden copy.

Irradiation Facilities

- ***Heavy ions***:
  - ^{18}O at 126 MeV (LET=2.85 $MeV * cm^2/mg$) and ^{19}F at 118 MeV (LET=3.67 $MeV * cm^2/mg$) at SIRAD facility served by a 14 MV TANDEM accelerator from Legnaro National Laboratories; (Italy, July 2015)
  - ^{16}O at 108 MeV (LET=2.97 $MeV * cm^2/mg$) and ^{28}Si at 157 MeV (LET=8.58 $MeV * cm^2/mg$) at SIRAD facility served by a 14 MV TANDEM accelerator from Legnaro National Laboratories, in Italy; (Italy, March 2017)
  - Heavy Ion Facility at Cyclotron Resource Center at Louvain-la-Neuve, Universite Catholique de Louvain (UCL), the following ions were used: (Belgium, June 2016)
    - ^{13}C at 131 MeV (LET=1.3 $MeV * cm^2/mg$);
    - ^{22}Ne at 238 MeV (LET=3.3 $MeV * cm^2/mg$);
    - ^{40}Ar at 379 MeV (LET=10 $MeV * cm^2/mg$); (different inclination angles wrt the beam: 0, 30 and 50 degrees)
    - ^{58}Ni at 582 MeV (LET=20.4 $MeV * cm^2/mg$);
    - ^{83}Kr at 769 MeV (LET=32.4 $MeV * cm^2/mg$);

Note: Results from highlighted facilities will be presented in this talk.

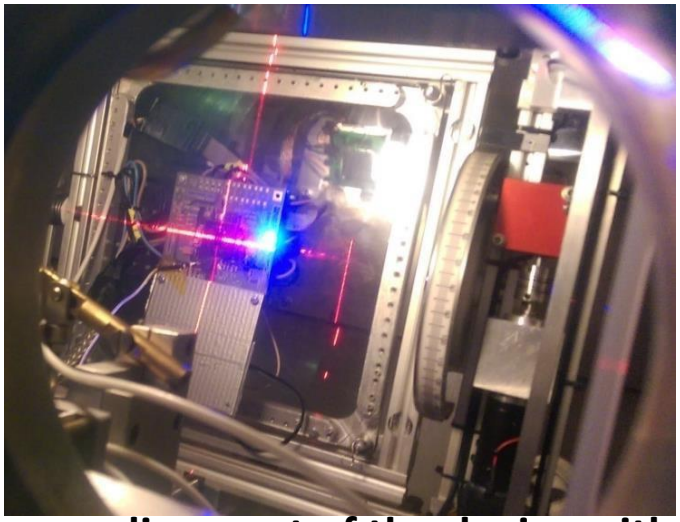
Irradiation Facilities

- ***Protons:***
  - Paul Scherrer Institute (at PIF) using 200 MeV protons (LET of 0.0036 $\mathbf{MeV} * \mathbf{cm}^2/\mathbf{mg}$); (Switzerland, August 2016)
  - Juliech Research Center (at COSY) using 35 MeV protons (LET of 0.0132 $\mathbf{MeV} * \mathbf{cm}^2/\mathbf{mg}$); (Germany, May 2017)
- ***X-Rays:***
  - Padova University using 10 keV photons; (Italy, March 2017)
- ***Mixed field:***
  - CERN (at CHARM) using 24 GeV protons with a metallic target, copper, without shield. (Switzerland, August 2017)

Note: Results from highlighted facilities will be presented in this talk.

Heavy Ions Irradiation Results

- Irradiation was performed at UCL, where several firmware versions were prepared for testing the CRAM and Flip-Flops failure rates;
- Two error mitigation techniques were introduced in the firmware versions: TMR for logic mitigation and SEM IP core for CRAM mitigation;
- A blind scrubbing procedure was implemented to allow a full device reconfiguration, and is triggered by the SEU rate occurrence in user logic (user defined criteria).



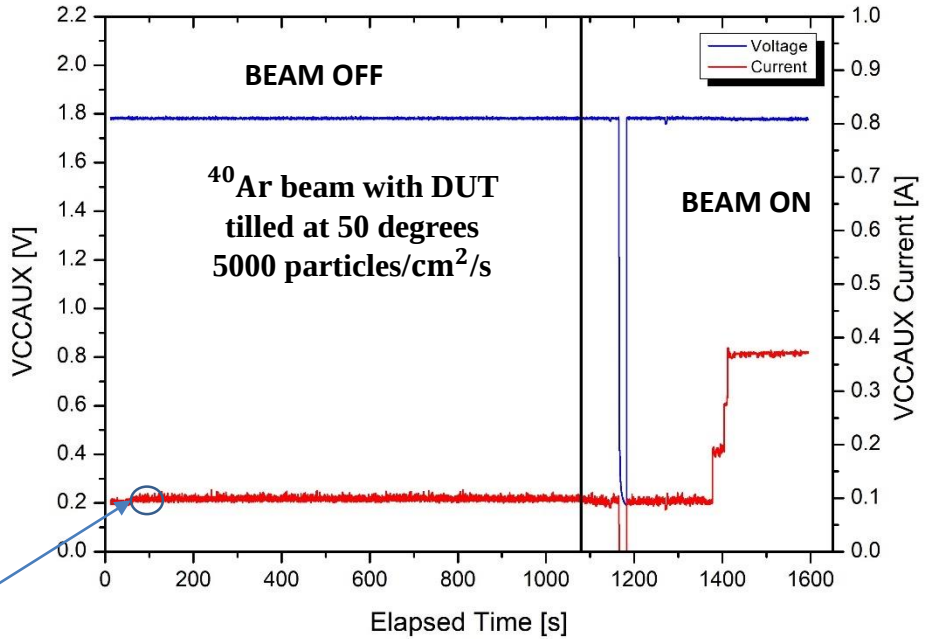
Laser alignment of the device with the particle beam longitudinal axis

The vacuum vessel inside of which the beam was extracted

Heavy Ions Irradiation Results

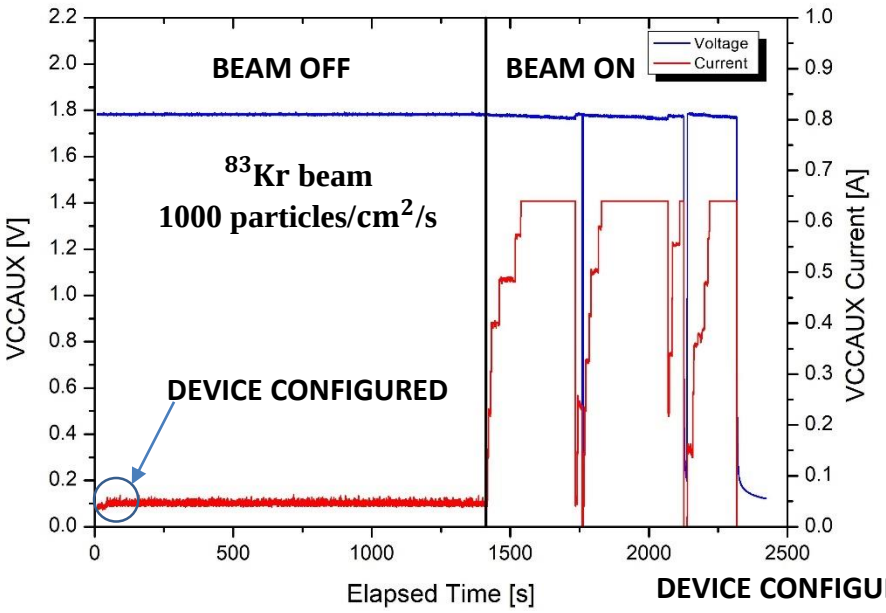
- With ^{22}Ne beam (LET=3.3 $MeV * cm^2/mg$): results - no latchup, significant SEU rate CRAM and logic;
- However, we saw 100 mA jumps (micro-latchup) in the VCCAUX rail when we used ^{40}Ar beam with the DUT tilled at 50 degrees with respect to the beam (LET=15.57 $MeV * cm^2/mg$).

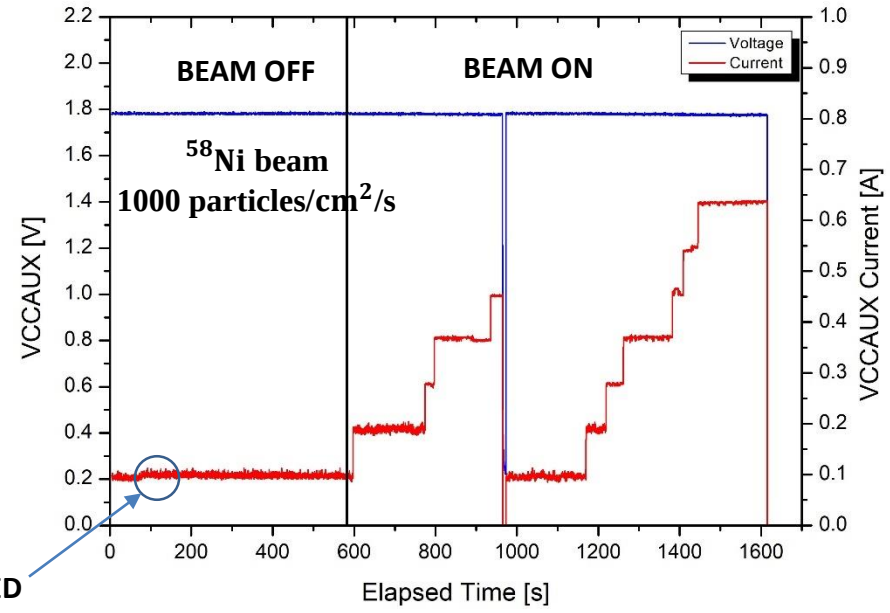
This kind of micro-latchup phenomenon observed on the VCCAUX rail is strongly related to the circuitry associated with type of programmable I/O banks, specifically the High Range I/O banks, for LET values < 40 $MeV * cm^2/mg$.
(DOI: 10.1109/NSREC.2016.7891736)



Heavy Ions Irradiation Results

- Micro-latchup reappears at higher LET, with ^{58}Ni at a LET of 20.4 $MeV * cm^2/mg$;
- When we used ^{83}Kr beam at a LET of 32.4 $MeV * cm^2/mg$ beside SEL, we saw 2 SEFI-like events.
  - During this run, we saw 2 latchup events in the 3.3 V rail used to power the HR I/O Banks and the programming block.

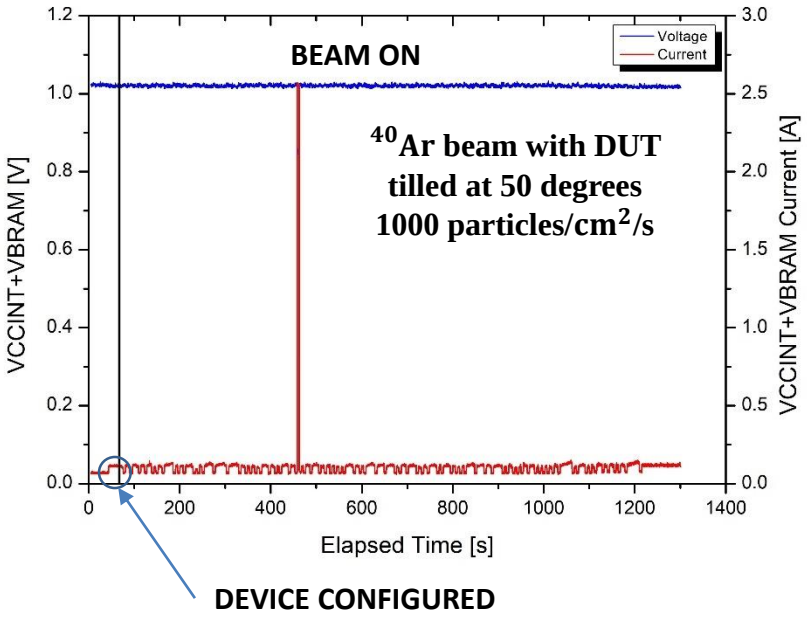




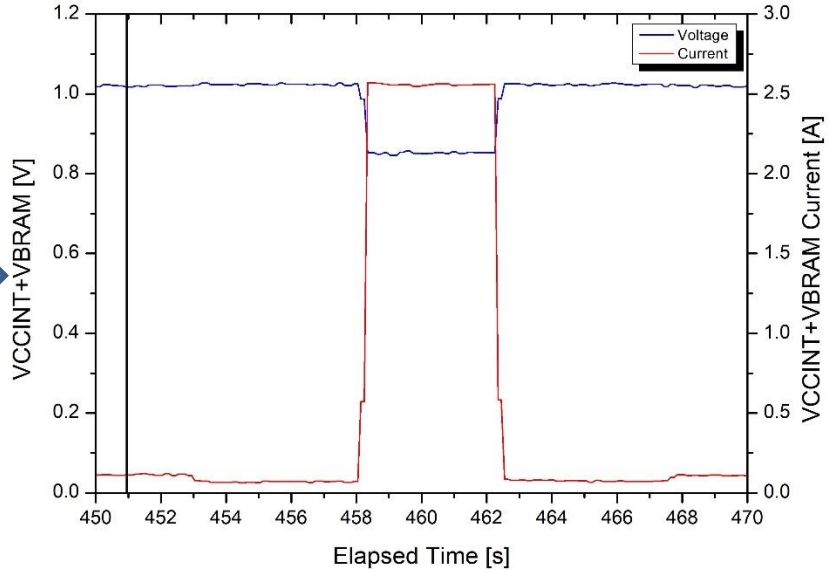
DEVICE CONFIGURED

Heavy Ions Irradiation Results

- High current states were observed in VCCINT rail when we used ^{40}Ar beam with the DUT tilled at 50 degrees with respect to the beam (LET=15.57 $MeV * cm^2/mg$);
- These events are called by literature *"Scrub SEFIs"*, because they are due to writing multiple frames into the wrong memory location when a scrubber is used (mostly), hence they are triggered either by a SEU in the Frame Address Register (FAR) or by a SET on the clock connected to the boundary scan registers that feed the configuration SRAM cells. (e.g. DOI: 10.1109/NSREC.2016.7891703)



Zoom on event



Heavy Ions Irradiation Results

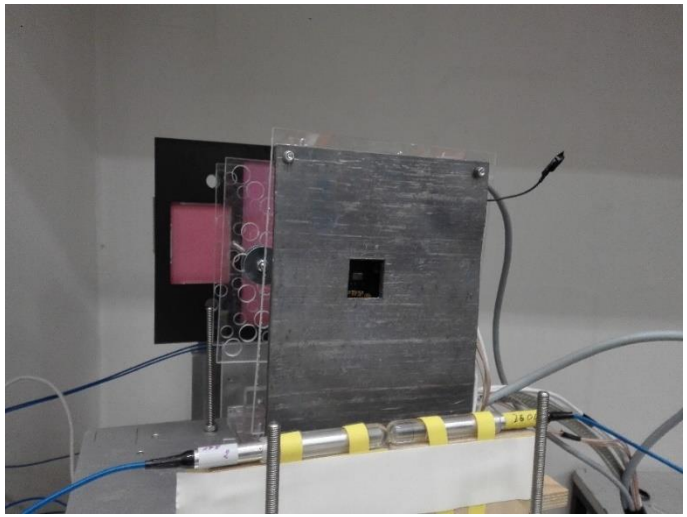
Ion Species	CRAM Cross-section $[cm^2/bit]$	Effective LET $[MeV * cm^2/mg]$
^{40}Ar	$0.9*10^{-9}$	15.57
^{58}Ni	$0.1*10^{-8}$	20.4
^{83}Kr	$0.3*10^{-8}$	32.4

Ion Species	SEL Cross-section $[cm^2/device]$	Effective LET $[MeV * cm^2/mg]$
^{58}Ni	$9.4*10^{-6}$	20.4
^{83}Kr	$5.5*10^{-5}$	32.4

- The threshold for CRAM SEU was seen below 1.3 $MeV * cm^2/mg$;
- The threshold for SEL is 15.57 $MeV * cm^2/mg$;
  - are consistent with other tests described by the literature;
- The measurement errors are between 30 - 50 %, and are due to Bragg Peak and substrate thickness;
- Full analysis results are being published.

Protons Irradiation Results

- Irradiation was performed at Juliech Research Center using COSY facility with 35 MeV protons;
- Several resources were tested: CRAM, BRAM, Flip Flops and I/O Banks;
- The SEM IP core was used as a mitigation technique for CRAM;
- For logic (Flip-Flops) we had 3 different TMR architecture which were tested in the beam;
- I/O Bank were connected in a ring structure.



DUT placed on the beam line

Protons Irradiation Results

- CRAM cross-section [cm^2/bit]: $4.9*10^{-15}$ (preliminary);
- BRAM cross-section [cm^2/bit]: $6.9*10^{-15}$ (preliminary);
  - Both measurements are consistent with the data available in literature;

Firmware type	Essential bits used for implementation	Resource utilization	Fluence [protons/cm^2]	Nr. of errors	Estimated cross-section [cm2/ logic element]
Single chain	300700 (1.59 %)	5500 FFs	$3.25*10^{10}$	35	$2*10^{-13}$
Basic TMR	1013097 (5.36 %)	18000 FFs 1 LUTs	$1.79*10^{10}$	36	$1.1*10^{-13}$
Partitioned TMR	1081293 (5.73 %)	16000 FFs 5333 LUTs	$3.32*10^{10}$	31	$0.43*10^{-13}$
Extended TMR	1092465 (5.78 %)	16200 FFs 5400 LUTs	$3.12*10^{10}$	38	$0.56*10^{-13}$

- Data are still under analysis.

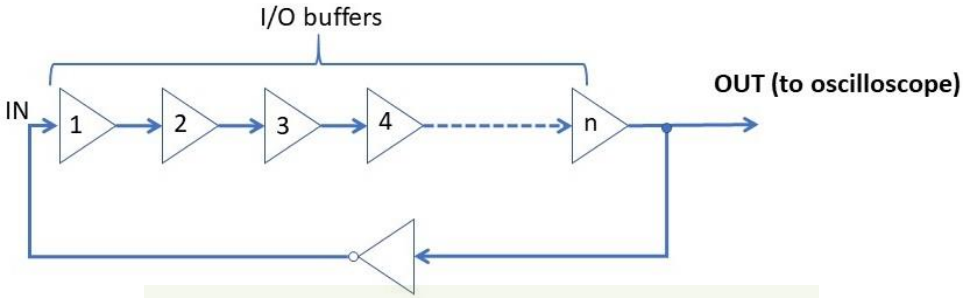
More about firmware architectures

Protons Irradiation Results

Firmware type (I/O used)	Essential bits used	Fluence [protons/cm^2]	Nr. of events	Estimated cross-section [cm2/bit]
71 %	36688 [0.19 %]	$1.85*10^{11}$	6	$0.9*10^{-15}$

Typical waveform of the oscillators

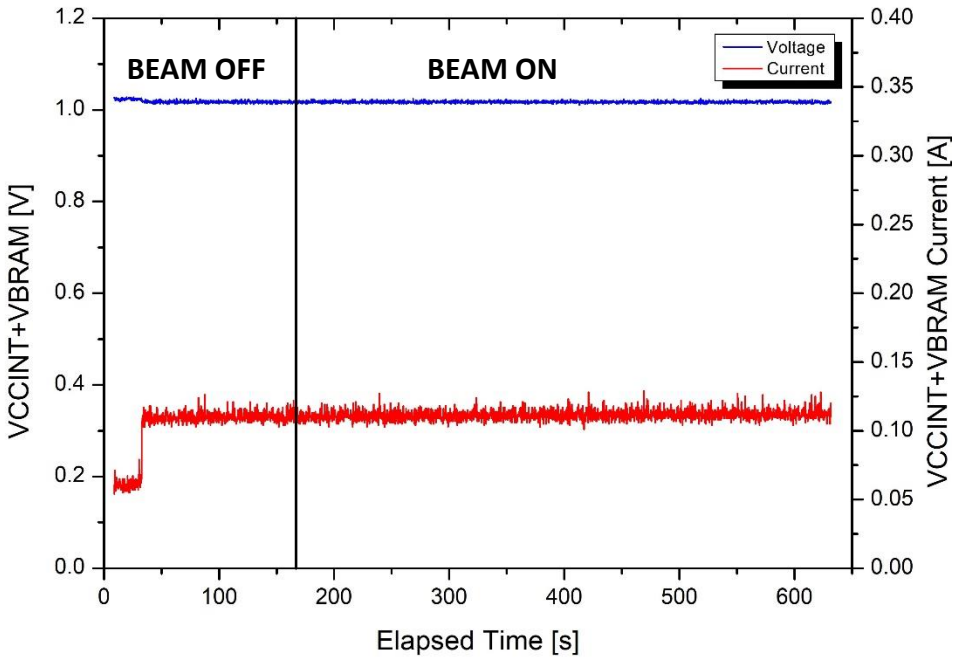
- We implemented 4 ring oscillators for each 5 from all 6 I/O Banks of the FPGA;
- The oscillation frequency of each ring oscillator is fixed, and ranges from 1 MHz to 11 MHz;
- Different type of failure have been seen: *changes in oscillation frequency* or *the output amplitude goes to 0*;
- Data is still under analysis.

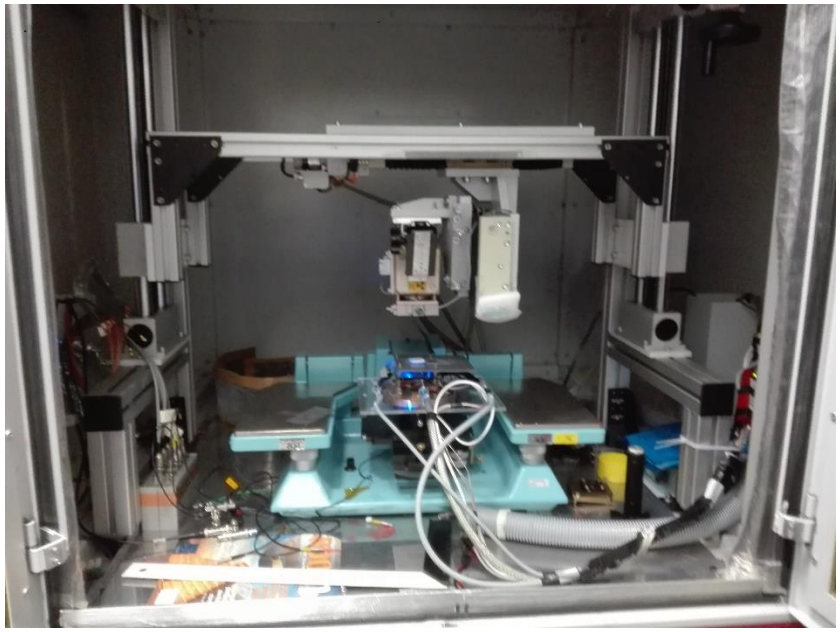


Simplified firmware architecture

X-Rays Irradiation Results

- Several resources were tested: CRAM, Flip-Flops and I/Os;
- 150 krad were delivered in 3 steps with 5 min per step each for 2 thinned FPGAs;
- No significant cumulative effects seen, DD and TID.





DUT placed in front of X-Ray-Source

TID summary

Sample	PSI protons [krad]	Padova X-Rays [krad]	Juelich protons [krad]	TOTAL TID [krad]
Sample 1	500		500	1000
Sample 2	510		250	760
Sample 3 (thinned)	500	160		660
Sample 4 (thinned)		150	250	410

Note:
- For PSI should be considered a 10-15 % fluency error;
- For Juelich should be considered a 5 % fluency error;
- For Padova should be considered a 20 % fluency error.

Conclusions

- Advance stage of investigation for device behavior in radiation environment - especially SEU in CRAM and the induced behavior;
- Large SEU rates in CRAM have been seen during beam tests;
  - the threshold was seen below 1.3 $\mathrm{MeV} * \mathrm{cm}^2/\mathrm{mg}$;
- SEFIs along with JTAG TAP controller failures were seen;
- The Kintex-7 withstand at 1 Mrad total TID delivered during beam tests;
- We are still analyzing the SEL data, though we had seen 2 SEL events in the 3.3 V rail used to power HR I/O banks and the programming block;
- Preliminary results do not recommend this DUT but also do not rule it out completely even for RICH radiation hard environment of the LHCb single arm spectrometer ;
  - *An equivalent back-up solution: the antifuse FPGA is to be tested next year.*

Future developments

- We had a mixed field radiation run at CHARM last month, and now we are analyzing the data;
  - I will give a short summary of the preliminary results on Wednesday, in the FPGA Working Group.

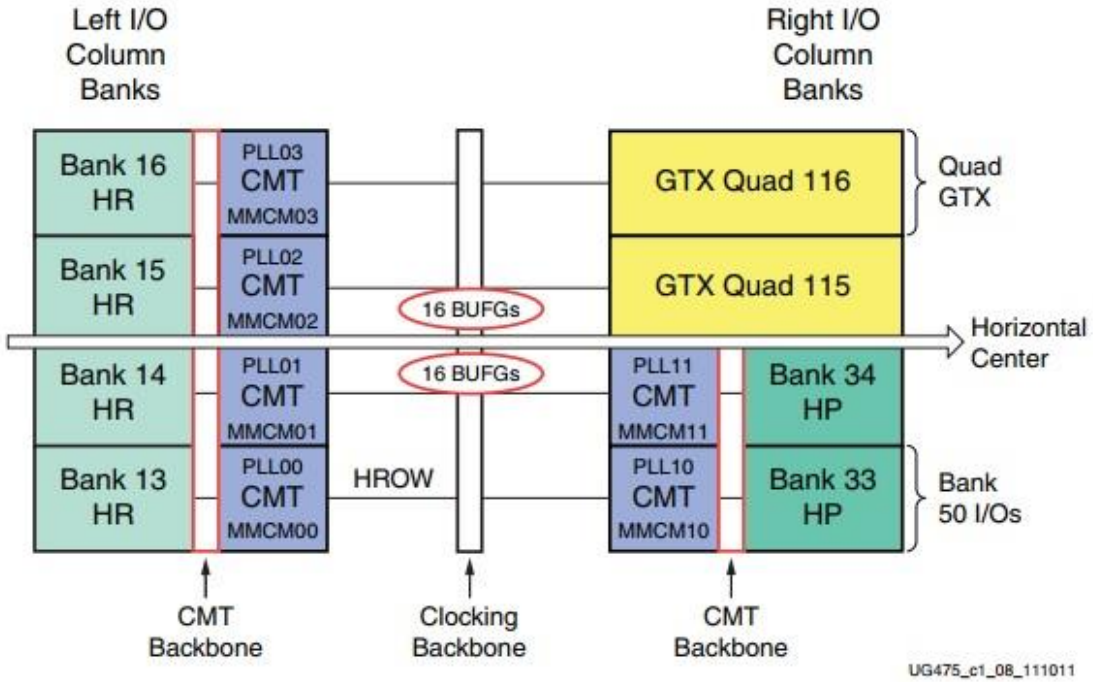
- Most measurements are in agreement with the existing literature, with caveats for hard particle spectra at LHC when extrapolating the results and interpreting;

- Study of I/O behavior is ongoing, a lot of data has been collected and are being analyzed and extrapolated to the case of LHC experiments;

- Improvements regarding the critical bits identification has to be done, with error injection through SEM IP Core tool.

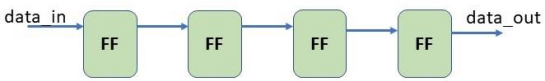
Backup Slides

XC7K70T-FBG484C6	XC7K70T-FBG676
❖ HR I/O bank 16 is partially bonded out. ❖ All HP I/O banks are fully bonded out. ❖ The GTX Quad 116 is not bonded out.	❖ All HR and HP I/O banks and the GTX Quads are fully bonded out in this package.

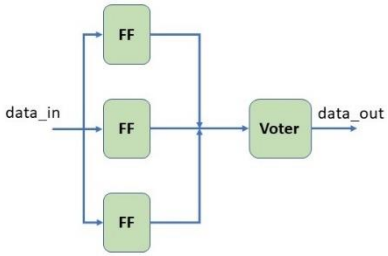


XC7K70T Banks

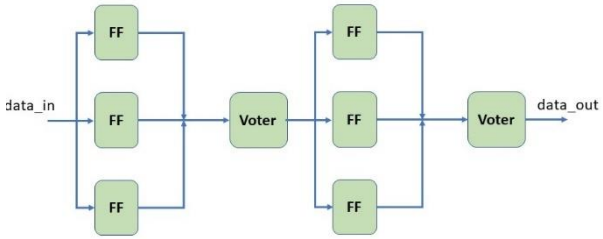
More at: link



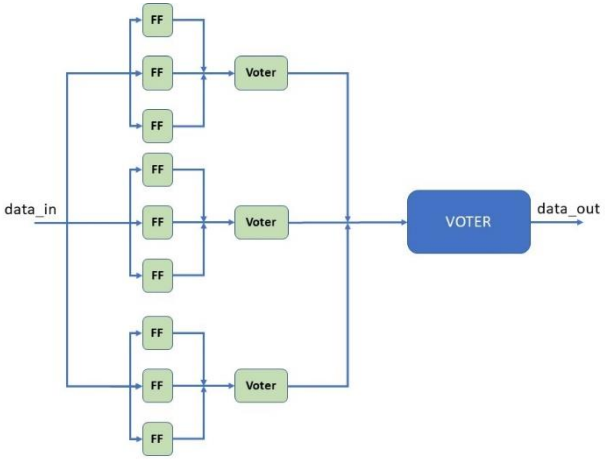
Single Chain



Basic TMR



TMR cell level



Extended TMR