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Radiation Hardness Studies and Evaluation on SRAM-Based FPGA for High Energy Physics Experiments

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Being a proposed solution for the digital boards of the upgraded LHCb RICH sub-detectors, SRAM-based FPGA devices have become widely used in high energy physics experiments. These studies aim to present the radiation hardness measurements done on the KINTEX-7 FPGA during irradiation with protons, X-rays and ions beams. For multiple values of the total ionising dose, linear energy transfer and proton energy, the cross sections of single-event-effects are estimated. We also give separate results for specific resources type: configuration RAM, block RAM, I/O banks and logic. Conclusions are reached on the radiation tolerance of this chip family in LHC environment.

Summary

The KINTEX-7 FPGA, considered the mid-range class of the 7 Series from Xilinx, is a commercial 28 nm high-K metal gate SRAM-based device which was proposed to be included in the design of the digital boards of the upgraded LHCb RICH detectors because of its price-performance ratio. An irradiation campaign was organized to test and qualify this FPGA for the radiation environment expected at 50 fb-1 integrated LHC luminosity. The test campaign includes irradiation sessions with: high penetration and high stopping power ion beams at the Legnaro National Laboratories in Italy and at the Cyclotron Resource Centre in Louvain Belgium; proton beams with different energies at the Paul Scherrer Institute from Switzerland and at the Nuclear Physics Institute in Jülich Germany; and an X-ray test at a facility from the University of Padova.
A custom test bench along with a DAQ system was specially designed for this kind of tests allowing us to run the FPGA in JTAG mode without any additional components like external configuration memory in order to have a realistic minimal setup which decreases the probability that the test board and monitoring system ensemble fails under radiation. Since the FPGA is designed using flip-chip technology and in order to allow the heavier ions to penetrate the dice to the bottom active layer the wafer was thinned from 250 to about 60 µm. During irradiation, the electrical parameters of the FPGA, voltages and currents, were monitored and saved for later analyses along with the CRAM mitigation report provided by the Soft Error Mitigation IP Core.
With ion beams providing Linear Energy Transfer (LET) values ranging from 1.3 to 32.4 MeV*cmˆ2/mg the FPGA was tested for single-event effects, especially the single-event latch-ups and single-event upsets, hence the calculated cross sections for both effects will be provided. With several dedicated firmwares calling specific resources like configuration RAM, block RAM, flip-flops chains, I/O banks, we have measured individually each corresponding cross-section.
Using 35 MeV and 200 MeV protons the FPGA was tested to get a maximum tolerance value for total ionizing dose and displacement damage. For single-event-effects, dedicated firmware was used to test logic with flip-flop chains, configuration RAM, block RAM and I/O blocks. The results of the device testing and its electrical characteristics during and after irradiation will be provided in this talk. A special attention was given to the I/O block ring oscillators which were tested, and I/O bank reliability will be discussed.
The X-ray tests helped us to confirm and tag the effects seen during proton tests, with most of them dependent on the total ionizing dose only.

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