Contribution ID: **101** Type: **Oral**

Effect of Gamma Irradiation on Leakage Current in CMOS Readout Chips for the ATLAS Upgrade Silicon Strip Tracker at the HL-LHC

Monday 11 September 2017 15:15 (25 minutes)

As part of the program for the upgrade of the ATLAS inner tracker for the High Luminosity LHC, irradiations have been carried out with 60Co gamma source. The measurements characterize the increase in the leakage current in the 130 nm-technology readout chips. The current as a function of total ionizing dose has been studied under different conditions: dose rate, temperature, power applied to the chip and pre-irradiation. The results show unique features that provide valuable information for the understanding of the mechanisms responsible for radiation damage in transistors. Models that attempt to parameterize the leakage current will also be presented.

Summary

The increase of the leakage current of NMOS transistors in certain 130 nm CMOS technologies during exposure to ionizing radiation needs special consideration in the design of detector systems, as this can result in large increases in current and power dissipation. As part of the R&D program for the upgrade of the ATLAS inner tracker for the High Luminosity upgrade of the LHC at the CERN laboratory, a dedicated set of irradiations has been carried out with the 60Co gamma source at the Brookhaven National Laboratory. Measurements will be presented that characterize the increase in the digital leakage current in the 130 nm-technology ABC130 readout chips, as observed by other experiments. The variations of the current as a function of time and total ionizing dose have been studied under different conditions, such as dose rate, temperature and power applied to the chip. The ranges of variation of dose rates and temperatures have been set to be as close as possible to those expected at the High Luminosity LHC, i.e. in the range 0.6 krad/h - 2.5 krad/h and between -10 ℃ and +10 ℃. Some of the chips under test were pre-irradiated with high doses of X-rays at Rutherford Appleton Laboratory, i.e. at a total dose of 8.5 Mrad and dose rate of 0.85 Mrad/h, in order to study the different effect of radiation on un- and pre-irradiated devices.

The results of this irradiation campaign reproduce the general observations by other experiments, however some unique features have been observed. Specifically, it has been observed an increase of the digital leakage current that peaks at values that are 1.2 - 2.7 times the baseline value (i.e. before irradiation), and both current peak value and current peak time depend on the dose rate. In order to study the dependence of the leakage current on temperature, temperature conditions were changed during operations. No changes in current have been observed when the temperature is raised from -10 ℃ to +10 ℃ after the current peak is reached. In order to study the effect of voltage bias on transistors, the chip power was turned off during irradiation. It has been observed that the current slowly resumes to the expected general trend once the power is applied again after a few days of interruption. Furthermore, It has also been found that pre-irradiated chips show no increase in digital leakage current up to a few Mrad of total ionizing dose, differently from chips that were not pre-irradiated. These results can provide valuable information for the understanding of the underlying mechanisms responsible for radiation damage in transistors and detector readout chips.

Models that attempt to parameterize the leakage current under different environmental conditions and how they fit to experimental data will also be presented.

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Session Classification: Radiation Tolerant Components and Systems

Track Classification: Radiation Tolerant Components and Systems