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A SEU Tolerant Latches Study for the RD53A Chip

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Abstract:
The RD53 collaboration was established to develop the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC and requiring extreme rate and radiation tolerance. The 65 nm CMOS process is adopted in order to satisfy the high level of integration requirement. The SEU immunity for this highly scaled process should be carefully considered because the device dimensions are small and the capacitance of the storage nodes becomes very low.
A chip prototype including different SEU tolerant structures was designed in the TSMC 65nm technology and proton irradiation tests were done in order to estimate the SEU tolerance of the proposed structures.

Summary

The 65 nm CMOS process is a promising technology for the pixel readout chips at HL-LHC in terms of high integration density and a first 65 nm demonstrator chip containing 76 800 pixels of 50µm × 50 µm will be submitted during the summer 2017.

Simulations show that the innermost parts of the new pixel detector will integrate a fluence of about 2.1016 n/cm2 (1 MeV neutron equivalent) corresponding to a Total Ionizing Dose (TID) of 1Grad equivalent of 10 years of exploitation. Irradiation studies were done in order to estimate the TID tolerance of the 65nm process and design rules were followed for digital and analog blocks to ensure good functionality in these aggressive operating conditions.
The flux of particles producing Single Event Upset (SEU) in the pixel barrel layer 0 (at approximatively 3.7 cm) is estimated to be 0.5 109/cm²/s. The cross section of the foundry latches is estimated by measurements to 3.10-14 cm²/bit which indicates that the mean time between 2 errors for the pixel configuration in each readout chip is around 50 ms. In order to optimize the immunity of the latches against SEU, a chip prototype integrating 2 different main flavors of SEU tolerant cells have been designed in 65nm technology and have been tested using a 24 GeV proton beam.

The first studied structure is the DICE latch (Dual Interlocked CEll) based on the redundancy of the storage node. The main drawback of this structure concerns the sensitivity of the charge sharing effect which appears on 2 nodes identified like critical. These nodes can be isolated and separated spatially by using an interleaved layout technic. Measurements show an improvement of SEU tolerance by a factor of 10 with respect to the single latch. A layout of 8 bits configuration memory block was done to be implemented as a pixel configuration memory inside the readout chip. The size of such a block represents only 4% of the whole pixel area.

The second type of latch is a Triple Redundant Latch (TRL) cell including a self correction error. Particular attention has been paid to the combinatorial logic controlling each single latch of the TRL and the global nodes were triplicated in order to prevent the transient errors occurring in the control logic to be propagated to the latches. Measurements of this structure show that the TRL latch allows an improvement of the SEU tolerance by a factor 3600 with respect to the single latch. However, it consumes a rather large area and can not be implemented inside the pixel. It can nevertheless be used in the chip periphery where it increases the SEU-hardness quite drastically.
In the pixel chip prototype, the TRL is used in the digital chip bottom and the synthesis tool is constrained to separate sufficiently sensitive nodes.

Recently, a new 65nm SEU prototype has been submitted in order to study the effect of the Deep NWell, used in this process, on the SEU tolerance.

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