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Development of Trigger and Readout Electronics for the ATLAS New Small Wheel Detector Upgrade

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The present small wheel muon detector at ATLAS will be replaced with a New Small Wheel (NSW) detector to handle the expected rate at the increase in data rates and harsh radiation environment expected at the LHC. Resistive Micromegas and small-strip Think Gap Chambers will be used to provide both trigger and tracking primitives. A new trigger and readout system is developed for the NSW detector. The new system has about 2.4 million trigger and readout channels and about 8,000 frontend boards. We will discuss the overall electronics design and studies with various ASIC and board prototypes.

Summary

The planned Phase-I and Phase-II upgrades of the LHC accelerator drastically impacts the ATLAS trigger and trigger rates. A replacement of the ATLAS innermost endcap muon station with a new small wheel (NSW) detector is planned for the second long shutdown period of 2019 - 2020. This upgrade will allow us to maintain a low pT threshold for single muon and excellent tracking capability even after the High-Luminosity LHC upgrade.

The NSW detector will feature two new detector technologies, Resistive Micromegas and small-strip Thin Gap Chambers. Both detector technologies will provide trigger and tracking primitives. The total number of trigger and readout channels is about 2.4 millions, and the overall power consumption is expected to be about 75 kW. The electronics design will be implemented in some 8000 front-end boards including the design of four custom front-end ASICs capable to drive trigger and tracking primitives with high speed sterilizers to drive trigger candidates to the backend trigger processor system. Tasks such as time, trigger and control signal distribution and readout are performed by the GBTx (Gigabit transceiver) ASIC, Slow Control ASIC, and an Front End Link Interface eXchange (FELIX) system. The large number of input channels, short time available to prepare and transmit data, harsh radiation environment, and low power consumption all impose great challenges on the design. The overall design as well as studies with ASIC and board prototypes will be presented.

Author: ZHU, Junjie (University of Michigan (US))

Presenter: HU, Xueye (Umich)

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