A Data Acquisition System for the CLIC Vertex Detector Readout Chip

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on behalf of the CLICdp collaboration

CERN, EP-LCD

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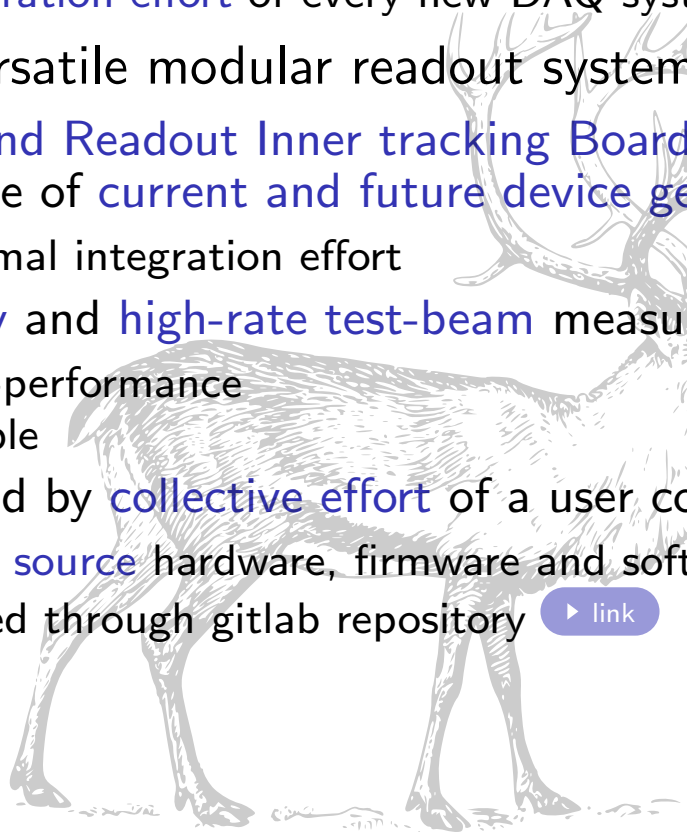
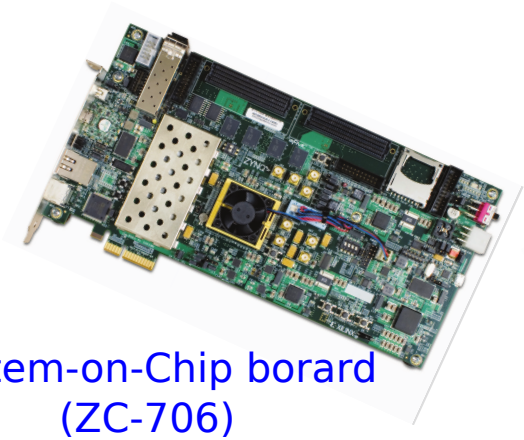
Outline

Motivation

- development of pixel detectors for future high-energy physics experiments
  - variety of DAQ systems
    - ★ chip characterisation requires commissioning and debugging of new hardware/firmware/software
    - ★ not innovative from functional point of view
    - ★ difficulty of cross-compatibility
    - ★ integration effort of every new DAQ system with a test-beam infrastructure
- solution: a versatile modular readout system
  - Control and Readout Inner tracking Board (CaRIBOu)
  - wide range of current and future device generations support
    - ★ minimal integration effort
  - laboratory and high-rate test-beam measurements
    - ★ high-performance
    - ★ flexible
  - maintained by collective effort of a user community
    - ★ open source hardware, firmware and software
    - ★ shared through gitlab repository ▸ link

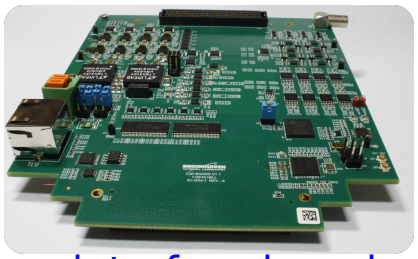


CaRIBOu as a multi-chip modular DAQ system



System-on-Chip borard (ZC-706)

FMC cable (optional)



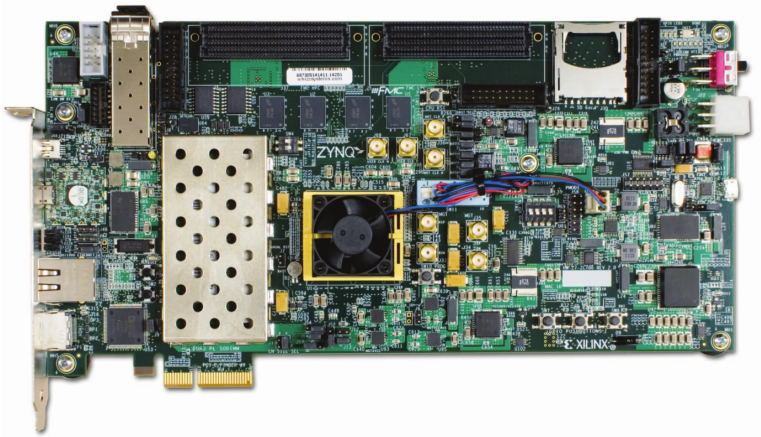
interface board (CaR)

application specific chipboard

Features:

- **CLICpix2/C3PD/FEI4/H35Demo** support
  - set of chipboards with minimal functionality provided by users
- voltage regulators, ADCs, bias sources and clock generator are close to the chip on the directly connected interface CaR board
- Zynq SoC can be placed in a safe distance (∼50 cm FMC cables) from the sensor assembly, to prevent radiation damage from sources or particle beams and facilitate mounting
- Zynq firmware and the interface CaR board developed by collective effort
  - collaboration under CaRIBOu project (Brookhaven National Lab, University of Geneva, CERN)

Commercial SoC ZC706 Evaluation Kit



- Zynq-7000 System-on-Chip (Z-7045)
- FMC HPC connector (8 GTX transceivers)
- FMC LPC connector (1 GTX transceiver)
- SFP+ connector
- availability
- cost effective and rapid solution for a small volume

Usage:

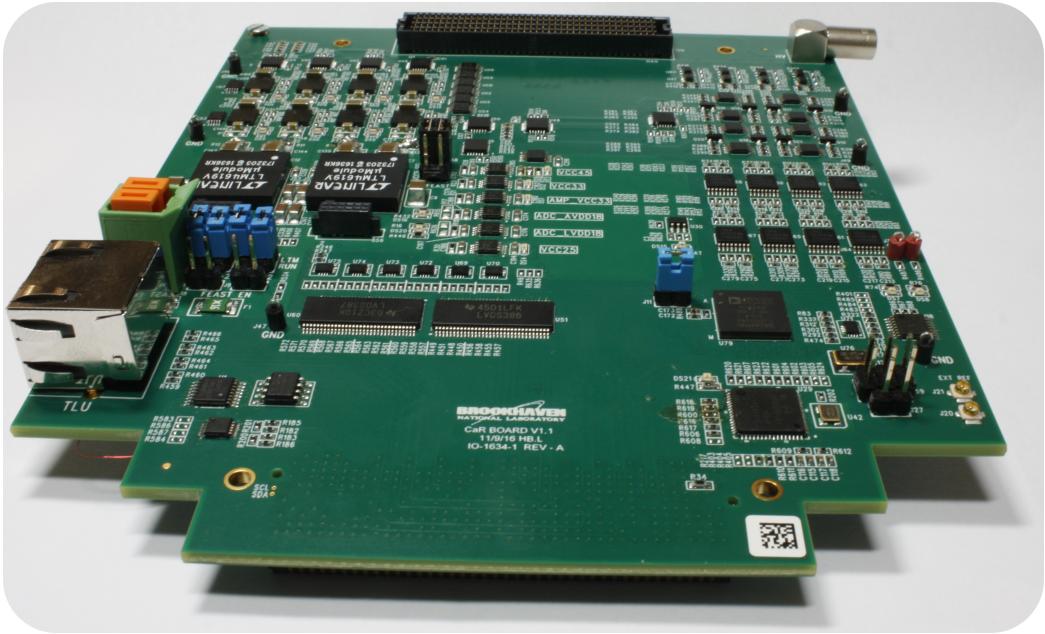
- the integrated dual core ARM Cortex-A9 processor runs Linux OS and the actual DAQ software
  - access through Secure Shell (*ssh*) connection (1Gbps Ethernet) or UART
- possibility of prompt local software analysis (data-quality monitoring, calibration, etc.)
- data pushed further through 1 Gbps (RJ45) or 10 Gbps Ethernet (SFP+)
  - possibility to use other interfaces of the evaluation kit (USB, SD card, PCIe) which are supported by the Linux kernel out of the box

Multi-chip CaR board v1.1

gitlab link

- FMC mezzanine — FMC HPC Connector
- Chip Board Connector — Samtec SEAF 320 Pins
- 8 × general purpose power supplies

  with monitoring capabilities
  - Maximum current: 3 A
  - Voltage range 0.8 — 3.6 V
- 32 × adjustable voltage output (0 — 4 V)
- 8 × current output (0 — 1 mA)
- 8 × voltage input (0 — 4 V)
- FEASTMP support
- 8× full-duplex SERDES links
- ADC (16 channels, 65 MSPS/14-bit)
- 4 × injection pulser
- HV input
- I2C bus
- TLU RJ45 input (clock and trigger/shutter)



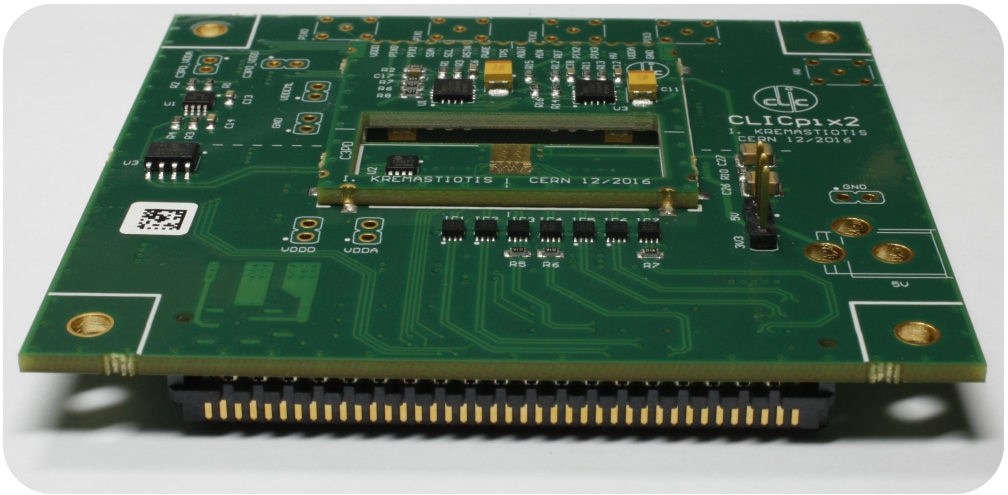
- general CMOS signals (10 × outputs, 14 × inputs) with adjustable voltage levels (0.8 - 3.6V)
- 17 × LVDS pairs — CML converters only on the specific chipboards
- output jitter attenuator/clock multiplier (SI5345)
  - Inputs: quartz, TLU, FMC, EXT (UMC)
  - Outputs: 3 × FMC (including GBT), 2 × SEAF, 1 × ADC
  - 0-delay mode

Suitable solution for various target chips:

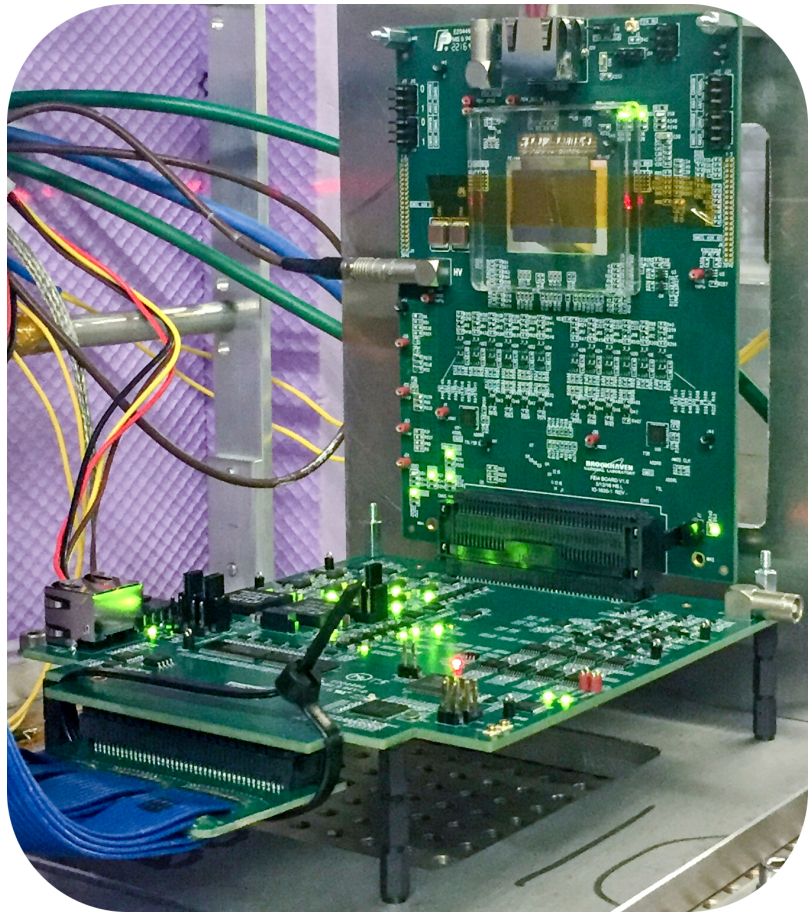
- support of many voltage levels, communication standards
- local measurement and monitor capabilities (ADCs)

Chipboards

- boards with minimum functionality
  - routing between SEAF connector and the chip under test
  - straightforward design
  - small production cost
  - specific buffers (LVDS-CML converters)
  - convenient test points



CLICpix2/C3PD chipboard



ATLAS FEI4/H35Demo chipboard mounted on CaR board

Plans of hardware upgrade

Xilinx Zynq UltraScale+ MPSoC ZCU102 Evaluation Kit

- 2 × High Pin Count (HPC) connectors
  - 2 × 8 GTH transceivers (up to 16.3 Gb/s each) — higher throughput
  - FMC connectors are pin compatible with the current CaRIBOu hardware
- quad core ARM Cortex-A53 Application Processing Unit (APU) — more computing power
  - frequency up to 1.2 GHz
  - 64-bit architecture
- dual core Cortex R5 Real-Time Processing Unit (RPU)
  - frequency up to 500 MHz
- ARM Mali-400 Based GPU
- 4 × SFP+ cages
- 4GB 64-bit DDR4 memory
- SATA connector
- price comparable with the currently used ZC706 kit

CaR v1.2

- bug fixes
- extension of the board specification
  - if requested, specific features can be added

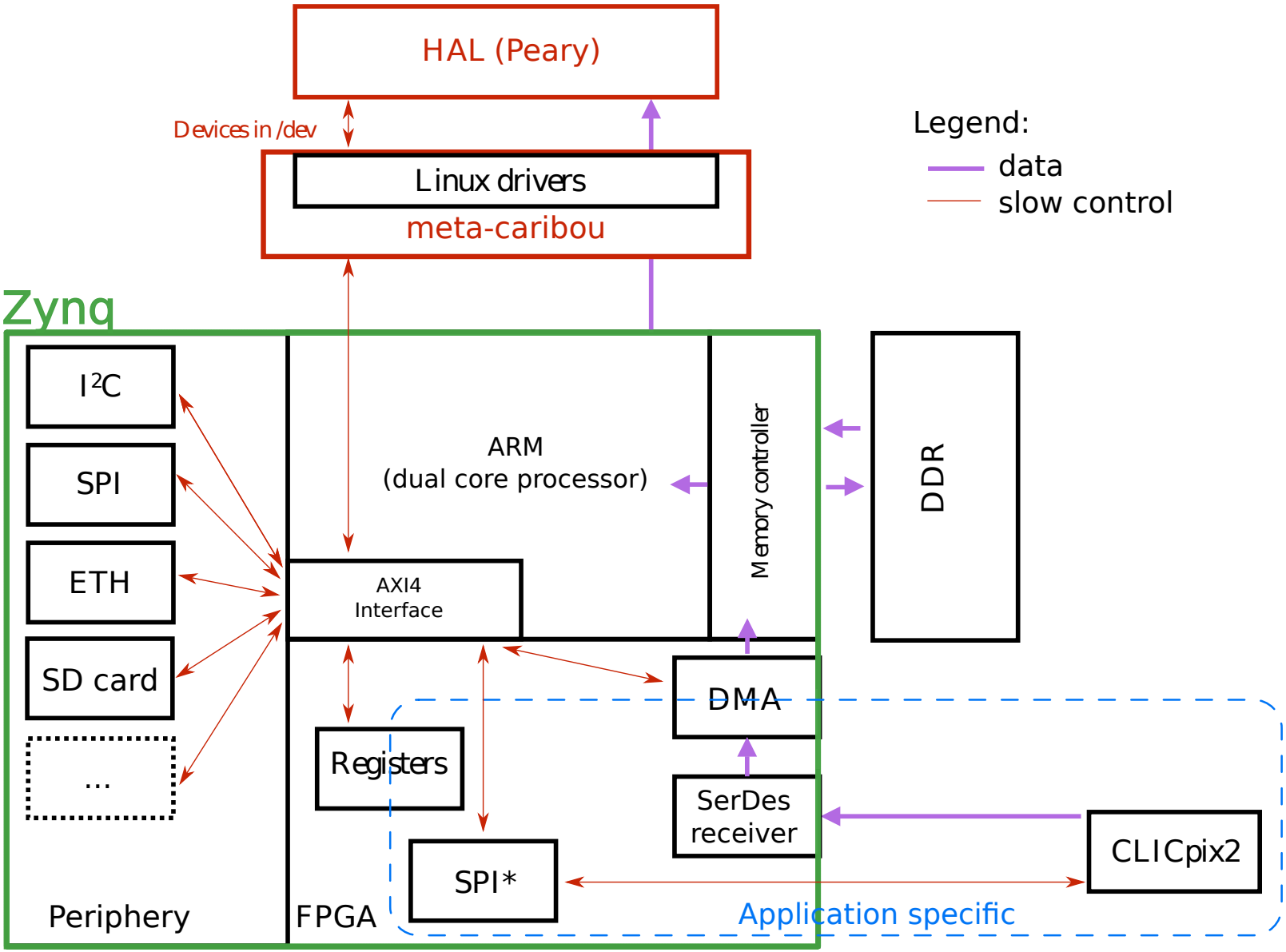
CaRIBOu DAQ

CaRIBOu DAQ consists of 3 parts shared through open access repositories:

- Peary link — software DAQ framework
- Meta-caribou link — custom Linux distribution
- Peary-firmware link — FPGA processing
  - universal CaR board unit
  - application specific unit
    - ★ library of sub-modules which can be ported between different applications

The framework supports currently CLICpix2 and C3PD. There is ongoing activity at UniGE in adding support for more chips.

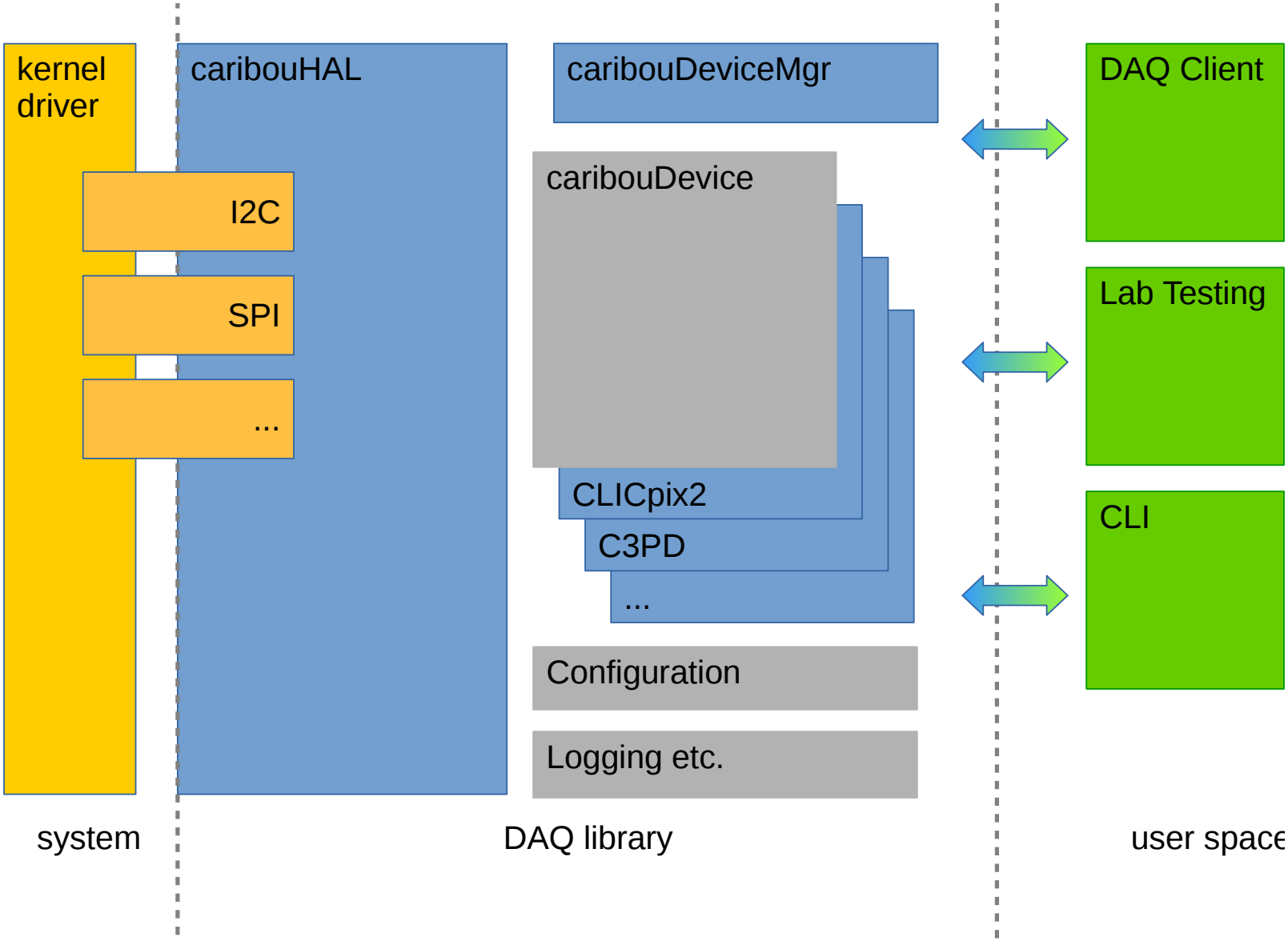
CaRIBOu DAQ schematics



Peary

link

DAQ software framework for the CaRIBOu DAQ System



Peary link

DAQ software framework for the CaRIBOu DAQ System

- control of the CaR board
  - user friendly Hardware Abstraction Layer (HAL)
  - unified way to access variety of hardware interfaces
- control of the chip
  - support of multiple devices in parallel (i.e.readout chip + sensor)
- device manager
  - dynamic linking of libraries based on device name stored in the configuration files
- Command Line Interface (CLI) support
- DAQ client support
  - integration with the top DAQ run control

Meta-caribou ▸ link

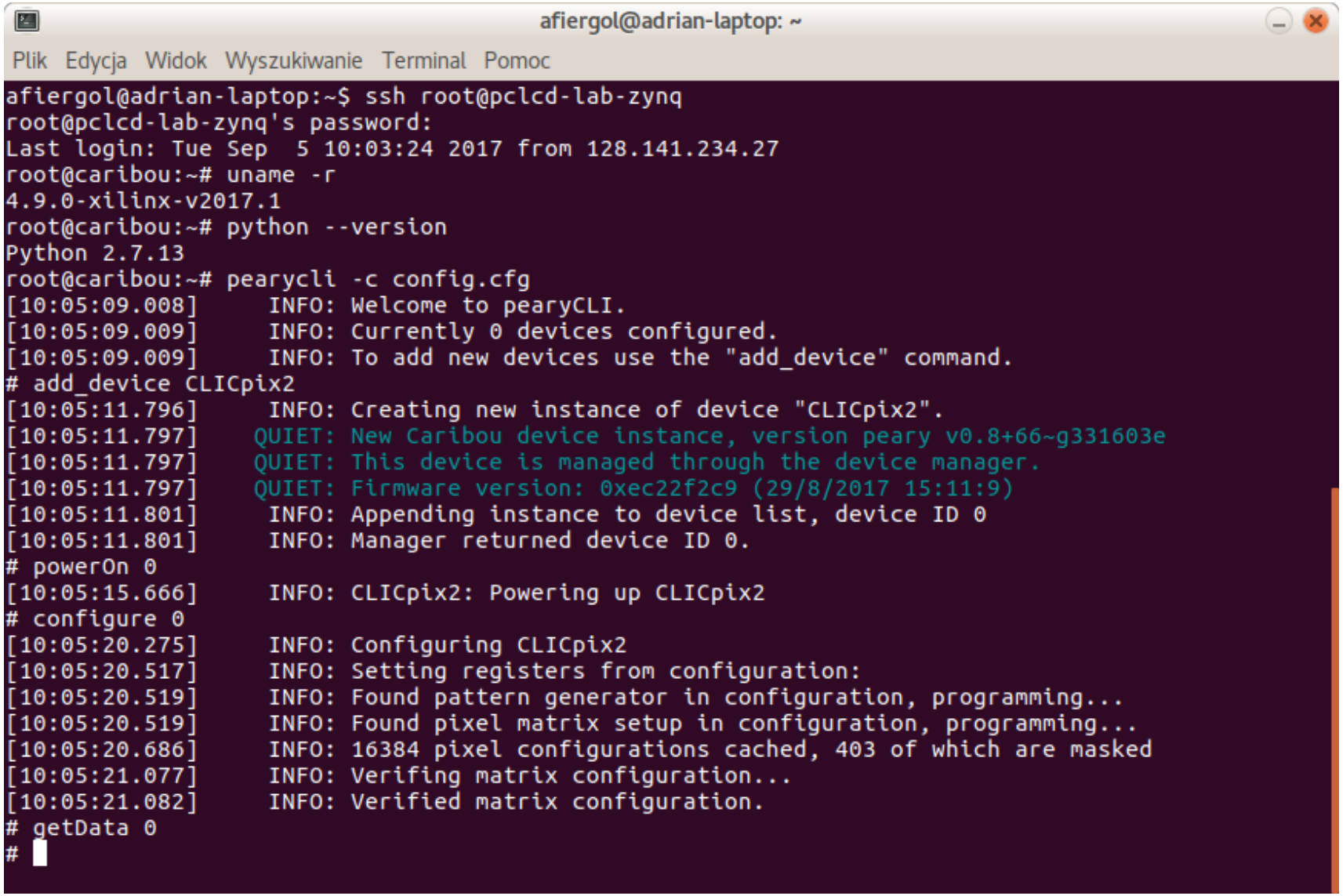
Yocto layer customizing CaRIBOu specific Linux distribution

CaRIBOu customization:

- A console-only image with full-featured Linux system functionality installed
  - popular packages (python, ssh, gdb, etc.) pre-installed
- Secondary Program Loader (SPL)
  - loads FPGA firmware (bitfile from Peary-firmware)
  - set ARM CPUs in the desired state (Peary-firmware)
- integrated with fixed revision of Peary-firmware
  - resources automatically fetched by build process
- CaR specific hardware description (Device tree)
- SD image creation which can be raw copied
  - dedicated script (*/meta-CaRIBOu/scripts/preapre_sd.sh*)

Meta-caribou ▸ link

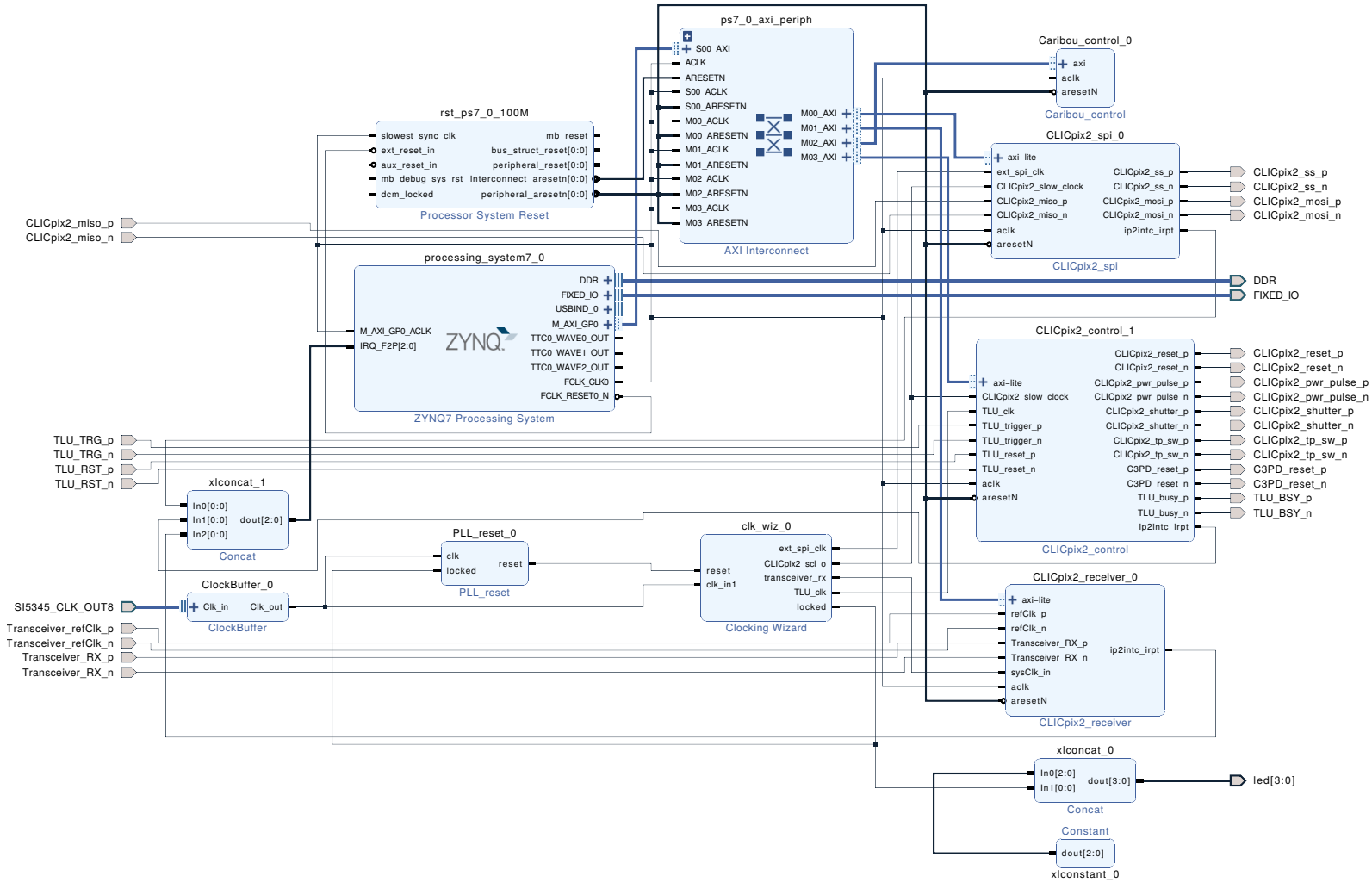
full-featured Linux OS system



Peary-firmware ▸ link

Firmware for Peary DAQ which is supported by custom Linux image defined by Meta-caribou.

It is the only part of CaRIBOu DAQ utilizing Xilinx property tools.



peary-firmware in CLICpix2 application

Peary-firmware ▸ link

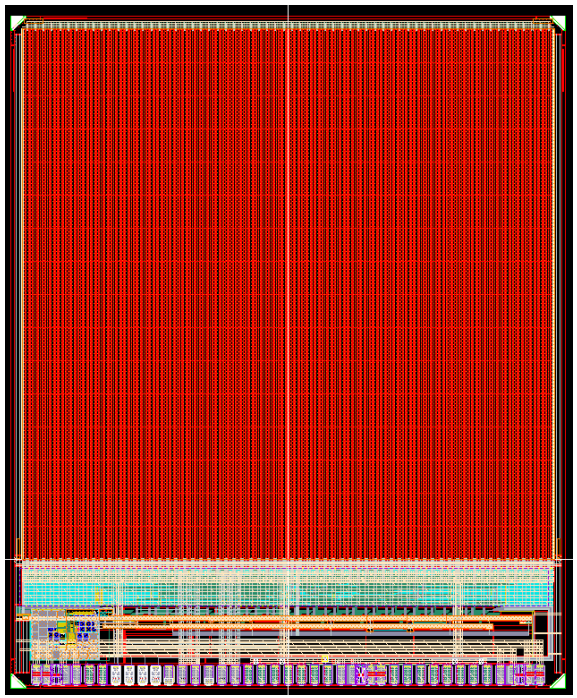
- configuration of the System-on-Chip (SoC)
  - periphery
  - address space
  - clock frequencies
- design handled by Xilinx IP Integrator
  - autonomous blocks following IP-XACT standard
  - easy integration
- library of Vivado IPs (i.e. DMA, SPI, I2C, etc.)
  - Linux device drivers maintained by Xilinx community of users
- application specific blocks
  - provide access to the chip (i.e. CLICpix2)
  - System Verilog support
  - easily accessible from software through */dev/mem* device
  - set of custom sub-modules (like SerDes receiver, custom SPI) already available in the repository
    - ⋆ software support examples
- Linux device tree and SPL generation
  - based on Hardware Description File (HDF)

CLICpix2 readout chip specification

- 65 nm CMOS technology
- pixel matrix:

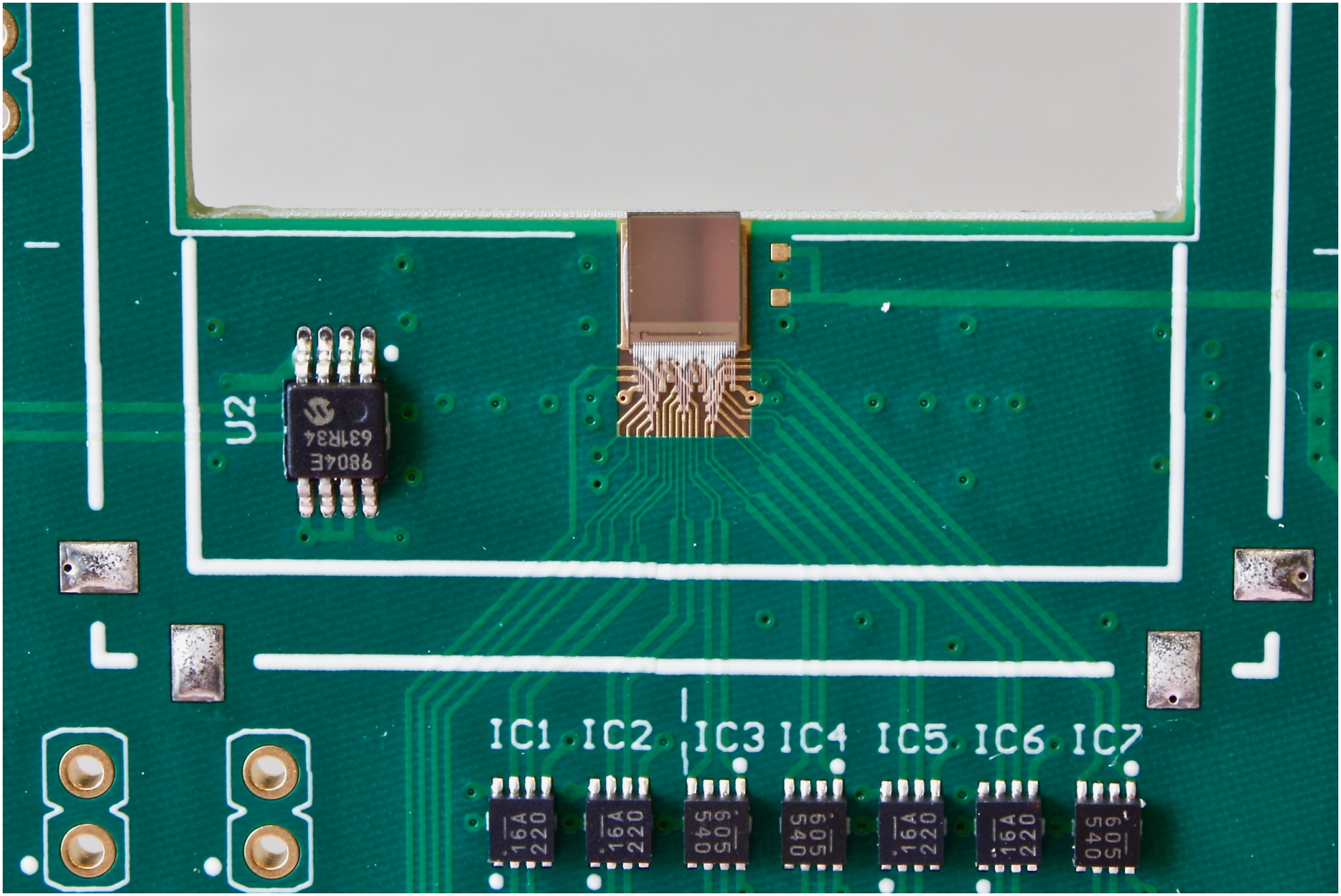
Matrix size [pixels]	**128 × 128**
Active area [mm^2]	**3.2 × 3.2**
ToT counter	**5 bits**
ToA counter	**8 bits**

- readout protocol based on Ethernet-like 640 Mbps SerDes stream
- configuration over SPI protocol (100 MHz)
- data compression
- frame encoding
- test pulse
- power pulsing

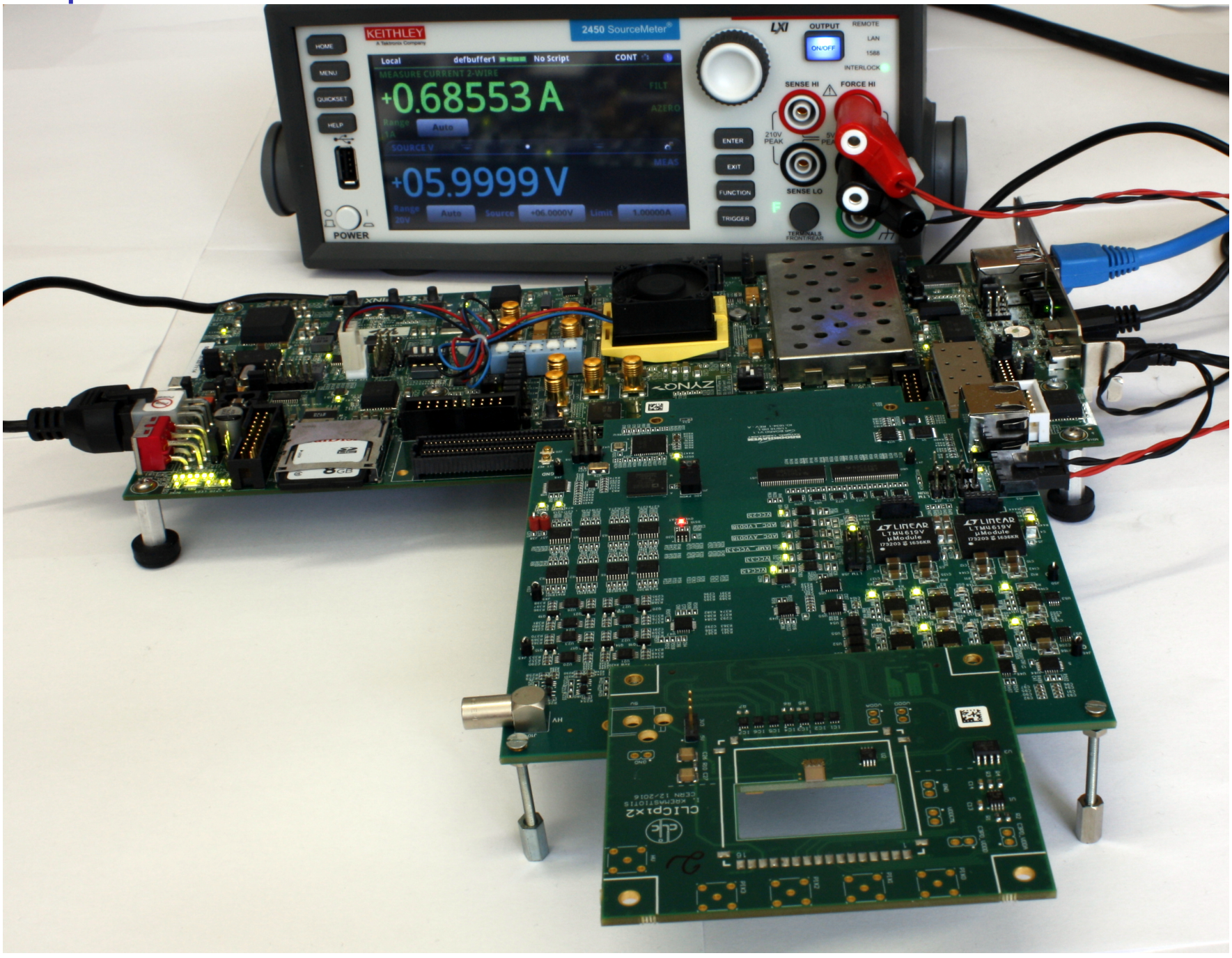


P. Valerio, E. Santin

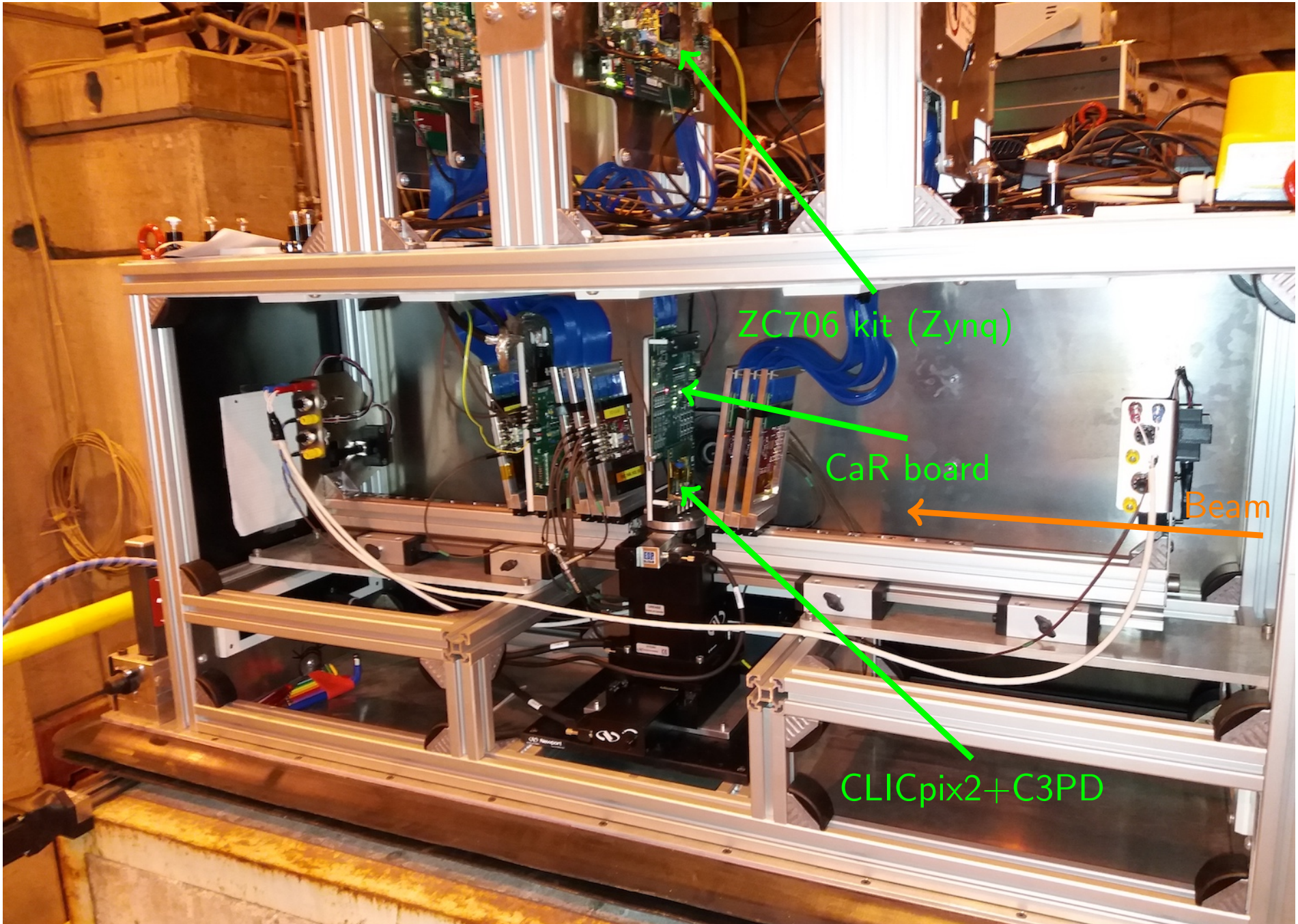
CLICpix2 assembly



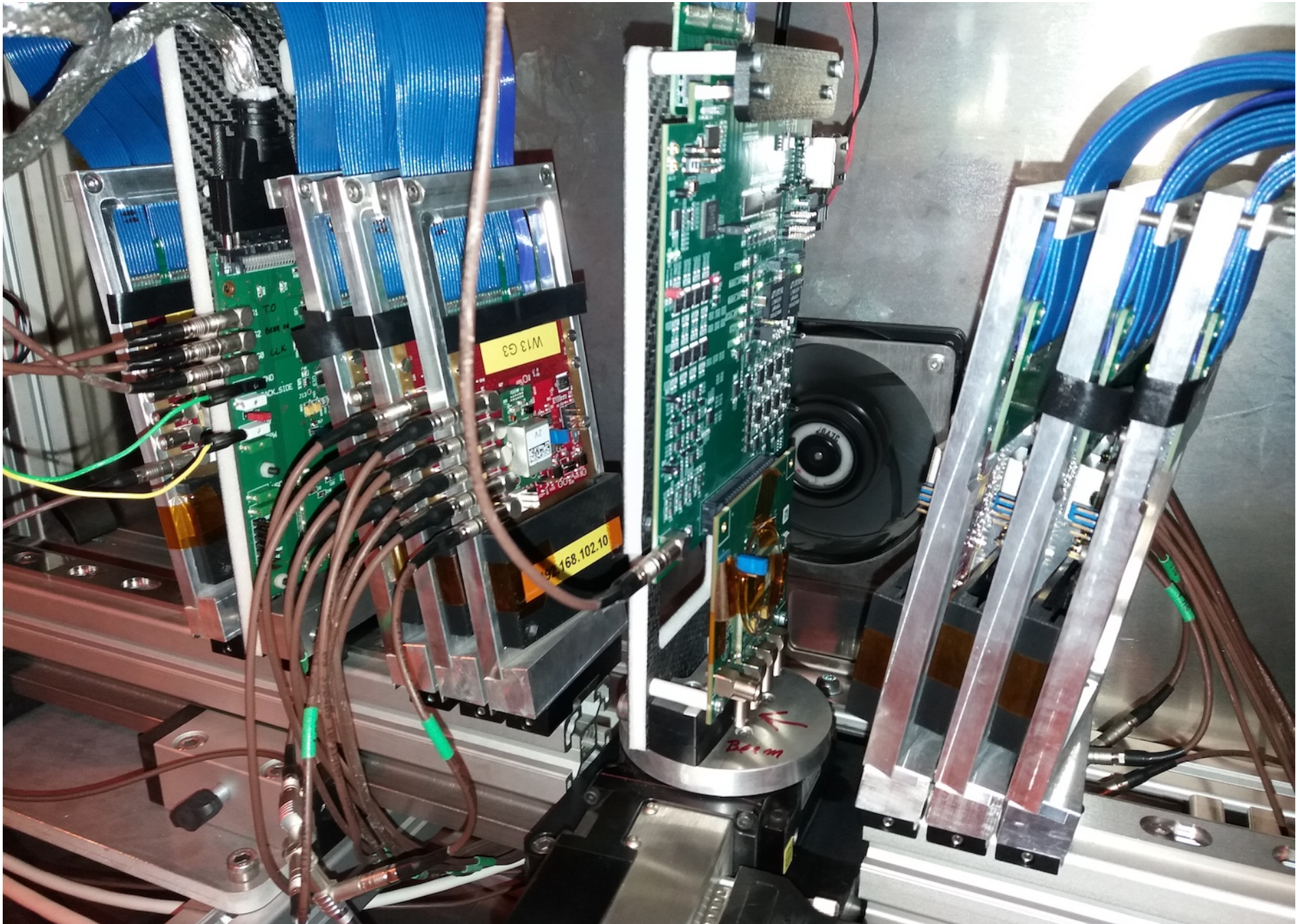
CLICpix2 in CaRIBOu framework



Test beam setup

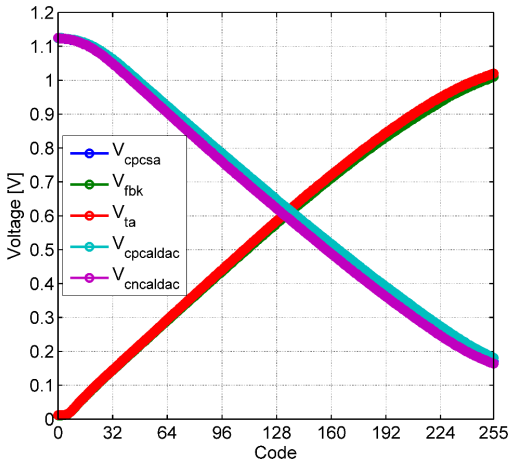


Test beam setup

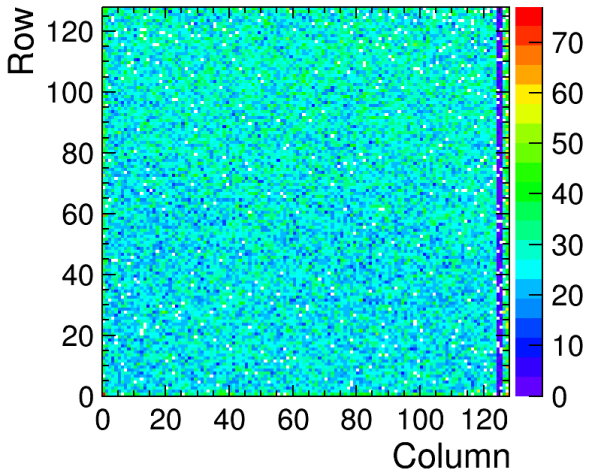


CLICpix2 and C3PD commissioning using CaRIBOu

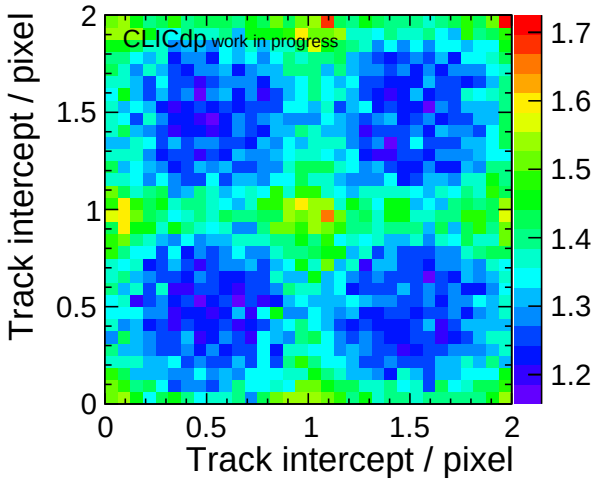
DAC scan



Hitmap



Cluster size



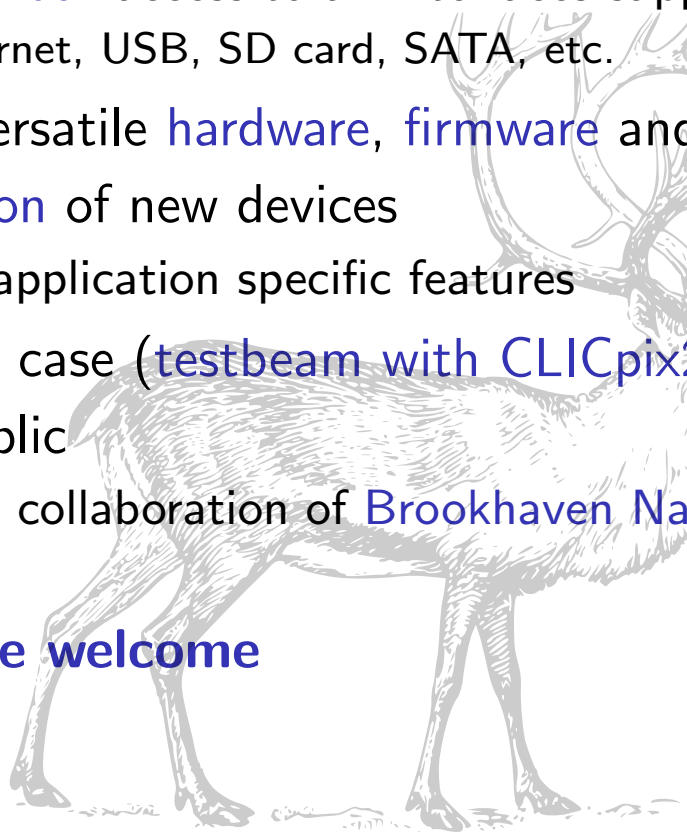
The measurements involved different features of the CaRIBOu system:

- SerDes readout and software frame decoding
  - 1.3 kHz frame rate for 80μs shutter length (disabled frame decoding)
    - can be further optimized by use of a binary data format and DMA acceleration
- chip configuration over SPI (CLICpix2) and I2C (C3PD)
- bias voltage and current source scans (DACs of the CaR board)
- local voltage measurements (ADCs of the CaR board)
- local clock generation using the CaR board resources
- adjustment and monitoring of power provided by the CaR board
- fast stand-alone equalisation
  - the CPU has direct access to the chip — no network delays
- successful integration with the Timepix3 SPIDR DAQ in the test beam

Summary

The CaRIBOu DAQ system:

- unique user experience of a regular fully-functional Linux terminal
- rapid implementation
- flexibility
  - can run locally user code written in any language
  - out of the box access to all interfaces supported by Linux kernel
    - ⋆ Ethernet, USB, SD card, SATA, etc.
- comes with versatile hardware, firmware and software
- easy integration of new devices
  - focus on application specific features
- successful use case (testbeam with CLICpix2 and C3PD)
- is open to public
  - successful collaboration of Brookhaven National Lab, University of Geneva and CERN
- **new users are welcome**



Thank you for your attention.