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A Data Acquisition System for the CLIC Vertex Detector Readout Chip.

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The DAQ of the CLICpix2 readout chip is based on the Control And Readout Inner tracking BOard (CaRIBOu). CaRIBOu is a versatile readout system targeting a multitude of detector prototypes. It profits from the heterogeneous platform of the Zynq System-on-Chip and integrates in a monolithic device front-end FPGA resources with a back-end software running on a hard-core ARM-based processor. The user-friendly Linux terminal with the pre-installed DAQ software is combined with the efficiency and throughput of a system fully implemented in the FPGA fabric. We present the design of the system and show examples of the achieved functionality and performance.

Summary

The development of pixel detectors for future high-energy physics experiments requires flexible high-performance readout systems supporting a wide range of current and future device generations. The versatile readout system of the Control and Readout Inner tracking BOard (CaRIBOu) targets laboratory and high-rate test-beam measurements with a multitude of detector prototypes. Under the project umbrella, application-specific chip-boards and a common interface card have been developed for a variety of pixel detector readout ASICs and active sensors. While currently supporting CLICpix2 and ATLAS FE-I4 hybrid pixel detector readout ASICs, it can be easily interfaced to other devices. The boards are hosted by a commercial evaluation kit (ZC706). This talk focuses on the data acquisition system (DAQ) based on a heterogeneous Xilinx Zynq All Programmable System-on-Chip (AP SoC). The device integrates the software programmability of an ARM-based processor with the hardware flexibility of an FPGA, enabling acceleration of the design, verification, test and commissioning processes. The CPU handles the slow control of the system, while the FPGA fabric performs data processing and data encapsulation in UDP datagrams moved by a Direct Memory Access (DMA) device through the High Performance Advanced Extensible Interface (AXI) port directly to the shared Random Access Memory (RAM). Further, data in RAM is accessed by the CPU for prompt analysis (data-quality monitoring, calibration, etc.) or is transferred eventually to a storage server over the 10 Gbps Ethernet link using a standard Linux network stack, the DMA and an offload engine implemented in the FPGA. Thanks to the fully capable dual-core processor running a Linux operating system, the DAQ board provides the unique user experience of a regular fully-functional remote terminal able to execute high level code (such as Python scripts). Moreover, as the code runs locally on the CPU integrated directly or indirectly (through the FPGA fabric) with the given ASIC, operations involving high input/output (I/O) activity (e.g. chip equalization) are not affected by network delays. The logic modules implemented in the FPGA fabric are available to the end user through the open source Linux device drivers maintained by the Xilinx community. In order to facilitate the creation of an embedded Linux distribution, CaRIBOu provides a layer to the Yocto build framework supported by a large community of open-source and industrial developers. The talk presents the design of the SoC-based DAQ system, its building blocks and shows examples of the achieved functionality and performance for the CLICpix2 readout ASIC and the C3PD active CMOS sensor.

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