Validation of the front-end electronics and firmware for LHCb vertex locator

On behalf of the LHCb VELO Upgrade Group

TWEPP 2017, Santa Cruz, CA

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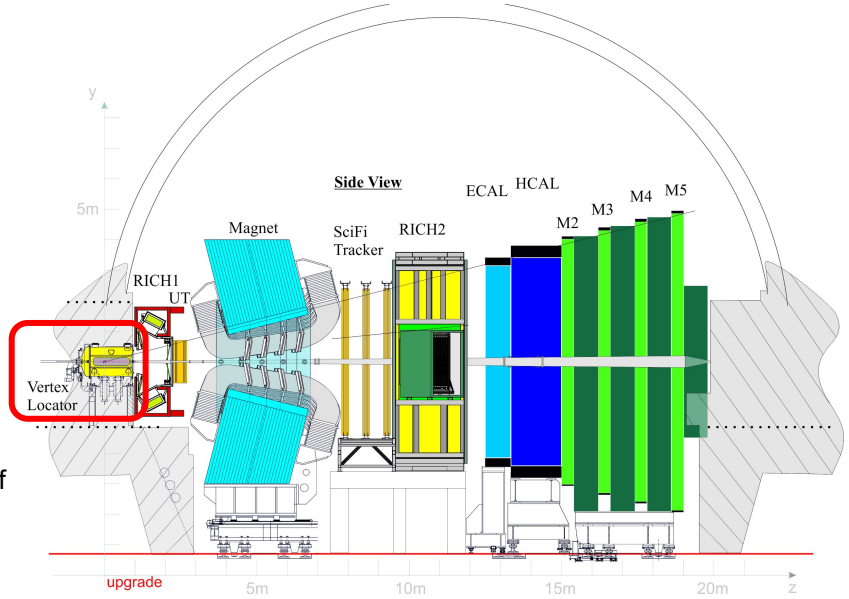
Overview

- LHCb upgrade overview
- VELO upgrade overview
- VELO upgrade electronics
  - On-detector
  - Off-detector
- Status of the hardware validation
- Status of the firmware validation

The Large Hadron Collider Beauty (LHCb) upgrade

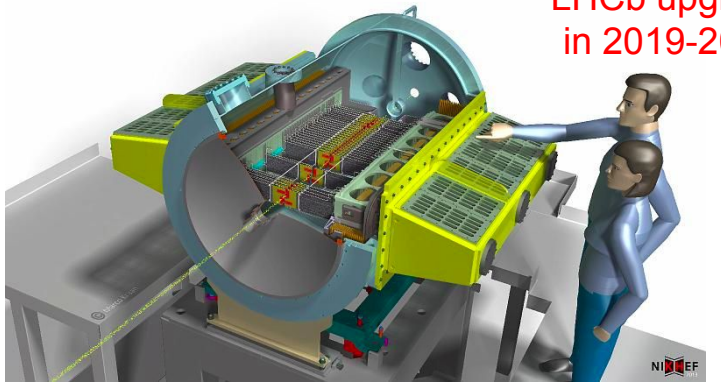
- LHCb is a dedicated experiment searching for new physics by studying CP violation and rare decays of b and c quarks
- Forward angle spectrometer with excellent vertex resolution and particle identification
- LHCb upgrade
  - Goal: 5x current luminosity
  - Actions:
    - Remove the current hardware trigger of 1MHz
    - New front-end and back-end electronics in most of the subdetectors
    - New tracking system

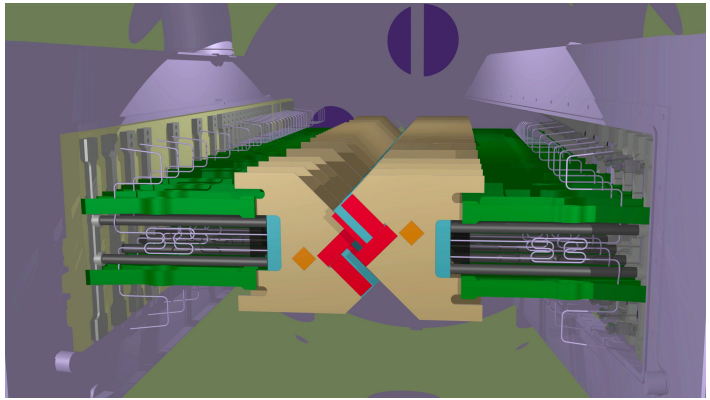


LHCb VELO upgrade

- Primary tracking and vertexing detector surrounding the collision region
  - In high vacuum (separated from the LHC)
- Pixel technology (currently microstrip)
  - More robust track reconstruction performance
  - Better resolution
  - Closer to beam (8.1mm to 5.1mm)
- Faster readout @ up to 40MHz
- New ASIC VeloPix, based on TimePix family
- Numbers
  - 52 modules, 624 VeloPix ASICs
  - Detector active area 0.12m²
  - ~41 M pixels
  - HV tolerance of 1000V
  - Trigger-less readout ~2.9 Tbit/s
  - New microchannel evaporative CO_2 cooling
  - Highly non-uniform radiation. Up to 400 Mrad

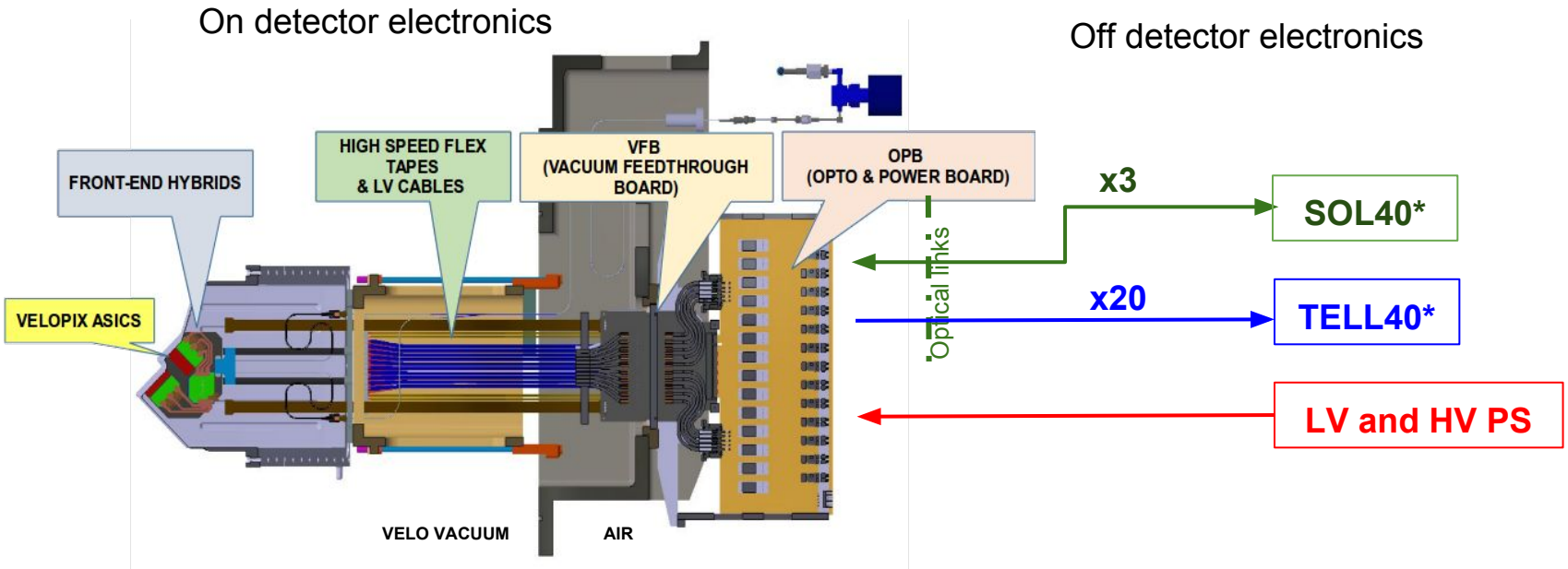
LHCb upgrade in 2019-2020





LHCb VELO upgrade electronics

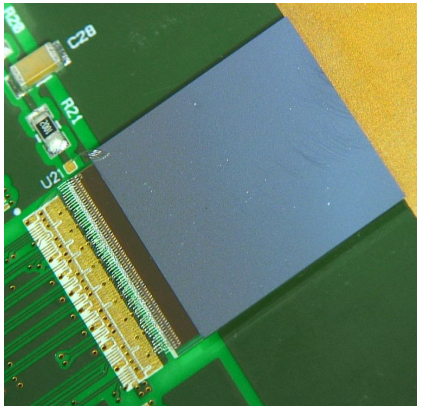
VELO electronics

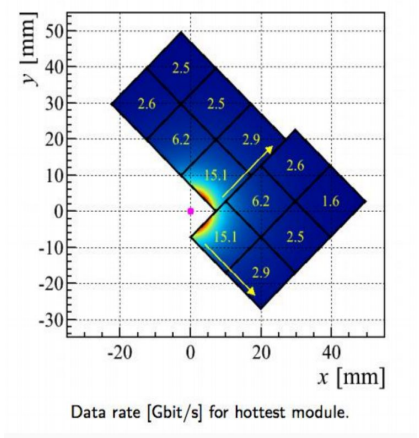


(*) - SOL40 board is responsible of distributing all the control signals to the front-ends
- TELL40 board is responsible of the high speed data acquisition

VeloPix ASIC

- 130 nm CMOS
- 256x256 pixels
  - Pixel size of 55 x 55 um²
- Radiation hardness
  - Highly non-uniform radiation
  - 400 Mrad, SEU tolerant
- Power consumption < 1.5 W/cm^2
- Peak hit rate of 900 Mhits/s/ASIC or 50 khits/s/pixel
- Binary readout
- Data driven readout at 40MHz
- Triggerless readout with max output rate 20.48 Gbps
- VeloPix V1 was produced in July 2016
- VeloPix V2 (final) sent to produce in July 2017

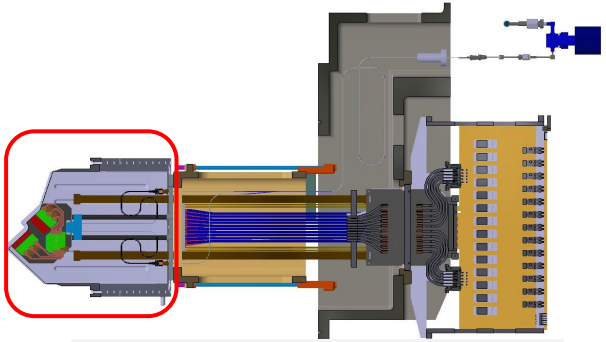


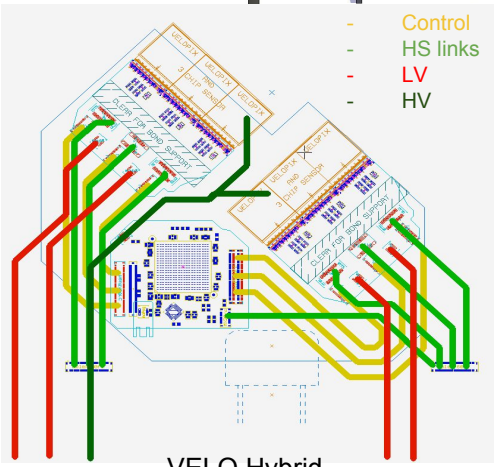


Data rate [Gbit/s] for hottest module.

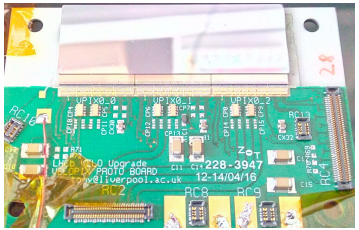
VELO module

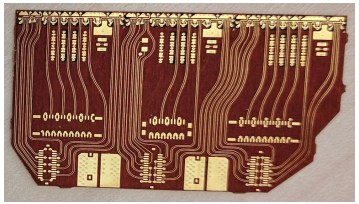
- VELO module is composed of 2 VELO hybrids, 1 on each side of a substrate
- Each hybrid is made of:
  - 2 **Tiles**, each one of them are made by a silicon sensors bump bonded to a row of 3 VeloPix ASICs
    - 1 tile is wirebonded to a FE board
  - 1 GBTx board
    - 6 VeloPix controlled directly with 1 GBTx chip (connected to e-port)
    - GBT protocol @ 4.8 Gb/s
- 20 High speed links come out of the VELO module using VELO GWT protocol @ 5.12Gbps
  - Main reason for using GWT protocol and not LHCb standard GBT is to reduce the power consumption
- LV from OPB board
- Pre-series of the final version is now in production

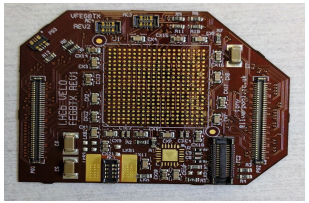




VELO Hybrid

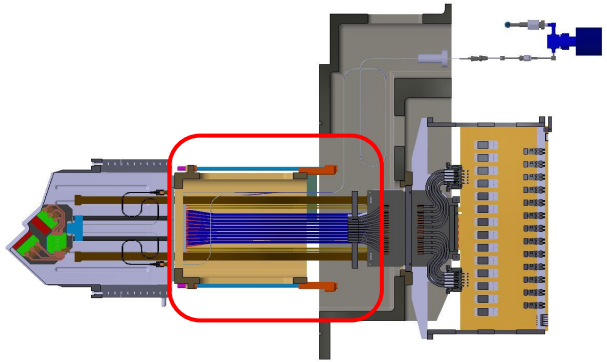

VeloPix tile


FE Hybrid board

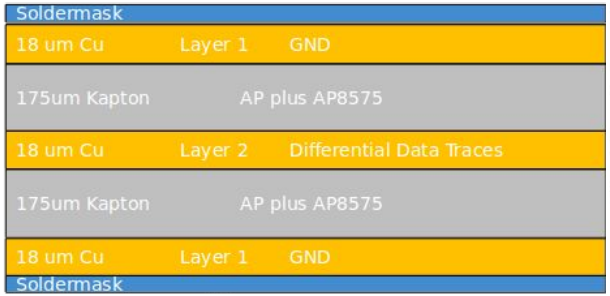

GBTx Hybrid board

Flex tapes

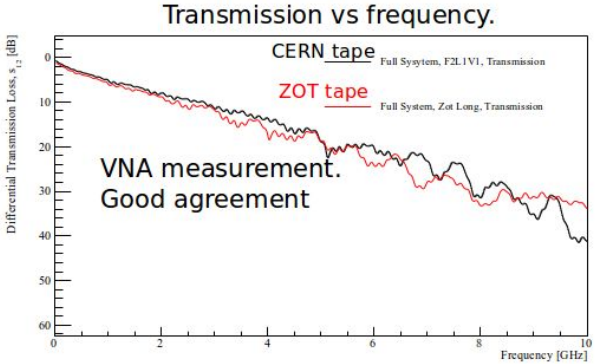
- Produced at CERN and industry (ZOT)
  - CERN prototypes v1
    - 200 um track & gap, 175 um Pyralux AP plus dielectric
    - Lengths: 56 cm
  - Industrial prototypes (Zot Engineering)
    - 180 um track, 200 um gap, 175 um Pyralux AP plus dielectric
    - Lengths: 56 cm
- Ready to produce

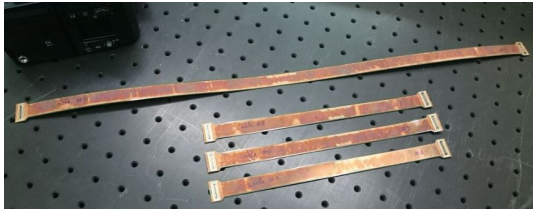


stackup



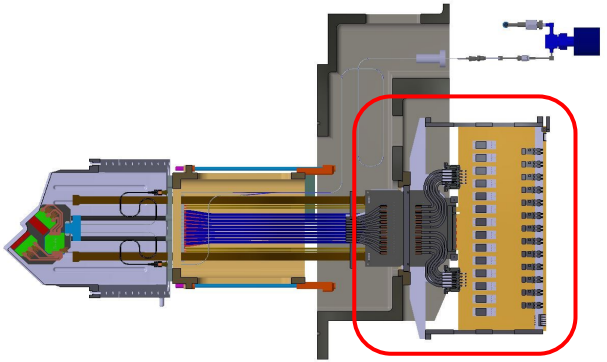
Using 50um Espanex Glue

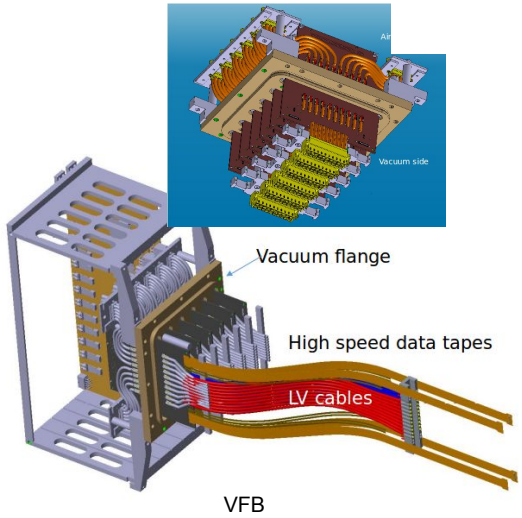


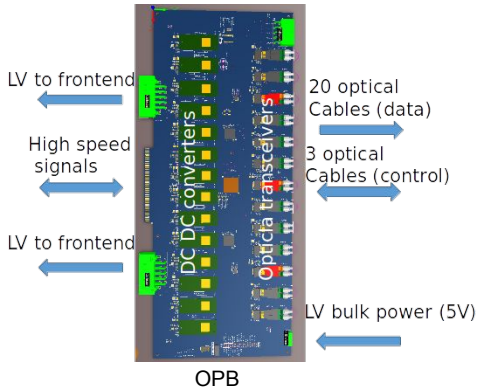


Vacuum feedthrough and opto power board

- Vacuum feedthrough board (VFB)
  - High speed signals
  - Temperature signals from NTCs
  - LV to module
  - HV to sensors
  - Temperature signals from cooling block
- Opto power board (OPB)
  - Provide low voltage power supply to the FE
  - Electro optical conversion
    - 10 VTTX (data link)
    - 3 VTRX (control link)
  - 2 SCA
    - FE monitoring Temperature, analog signals, etc
    - Control FE low voltage
  - 2 GBLD
    - Line driver to pre emphasis the FE GBT signal
- Pre-series of the final version is now on production

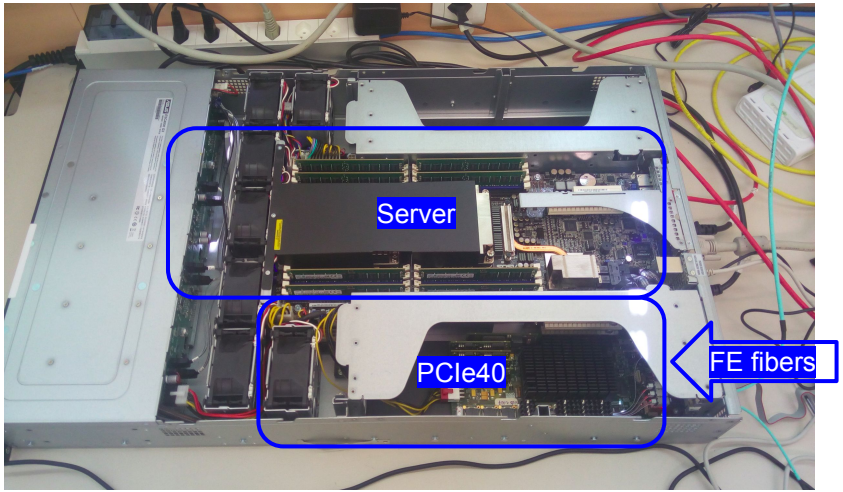






Off-detector electronics

- LHCb wide common off-detector electronics, the same hardware, PCIe40 (Altera arria 10 FPGA) board + server, with different firmware configuration (S-ODIN*, SOL40, TELL40)
  - SOL40
    - FE control
      - Experiment Control System (ECS), configure and readout the FE
      - Timming and Fast Control (TFC), synchronize the data acquisition of the whole experiment
    - 4 SOL40 boards for the whole VELO
  - TELL40
    - Data acquisition with a max rate of 100Gb/s
    - 20 links per TELL40 (1 module)
    - 52 TELL40 boards for the whole VELO
- Note: for future test and validation of produced modules of VELO will be used MiniDAQ 2 system (PCIe40 board + server) with a combination of the firmwares: S-ODIN, SOL40 and TELL40
  - MiniDAQ 2 delivered to VELO group in July 2017

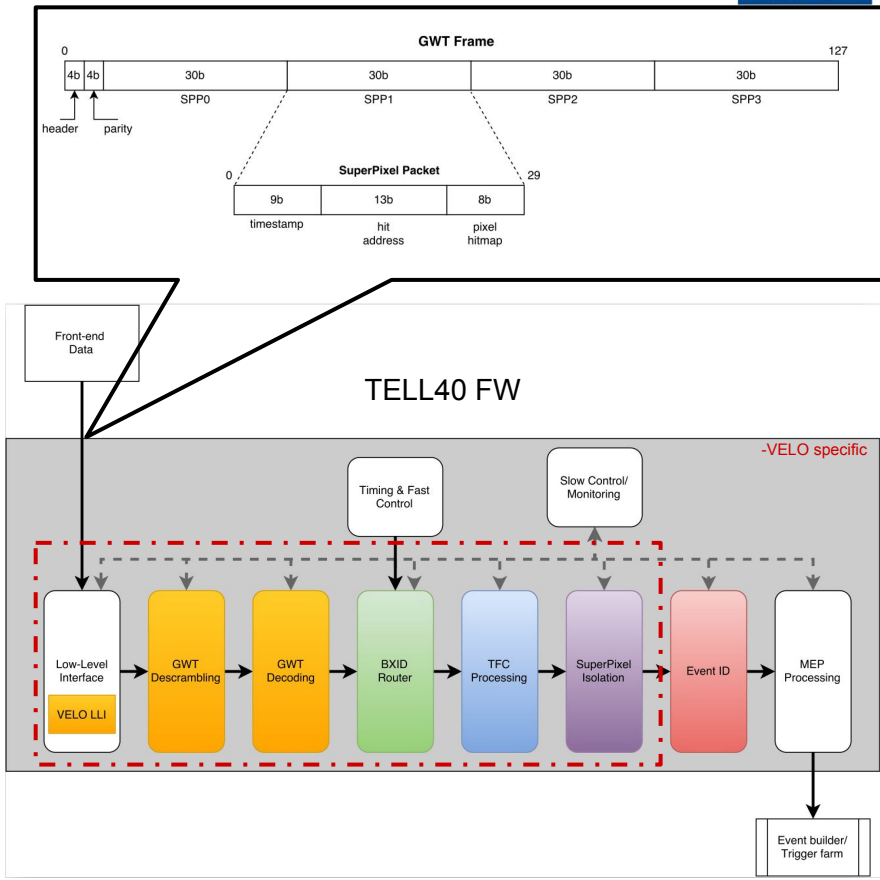


MiniDAQ2 system

(*) S-ODIN is responsible of timing and fast control

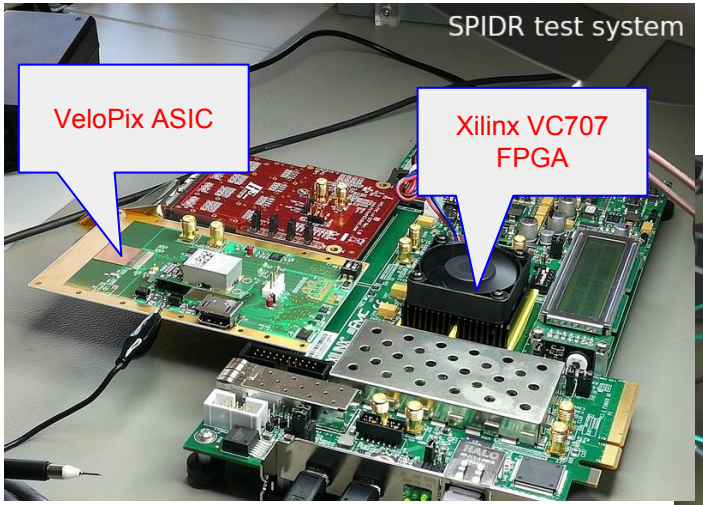
VELO Firmware

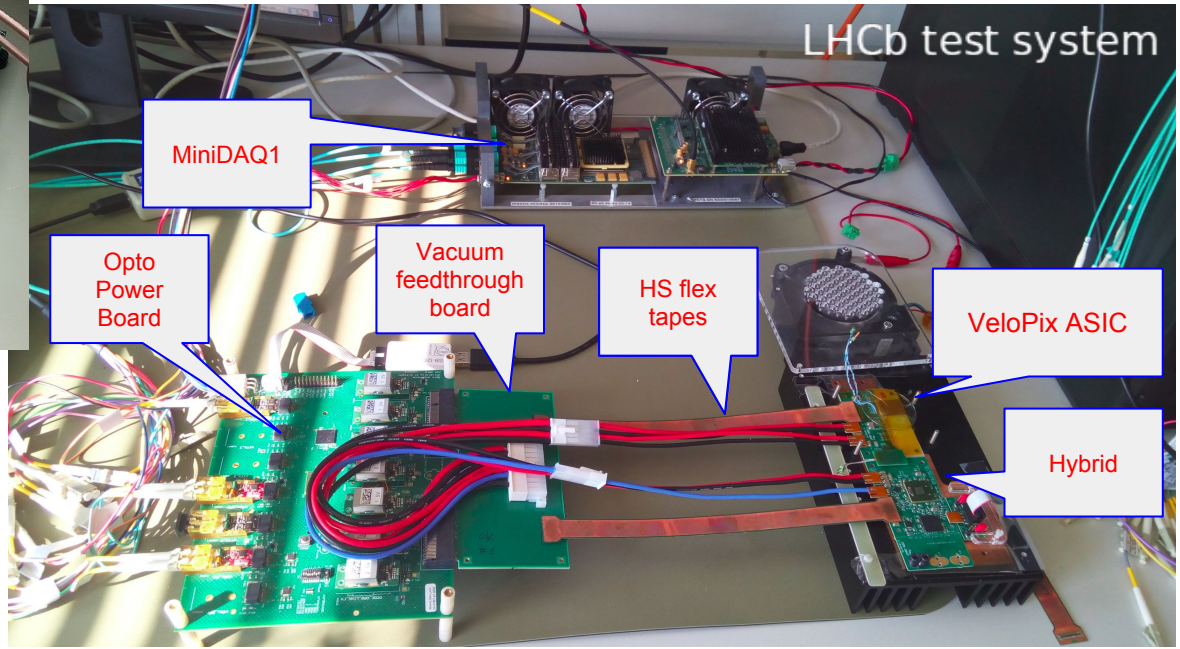
- SOL40
  - Modifications on LHCb common FW in order to control VeloPix directly from GBTx E-port
- TELL40
  - Input of 20 links @ 5.12 Gb/s each
  - LLI
    - Velopix data reception, recovering the data from the fiber
    - Descrambler is needed
      - VELO GWT data maximize the optical link transitions, allowing TELL40 CDR to recover the clock, by scrambling the data
  - BXID router
    - Router is needed because VELO is the only subdetector that sends temporarily unsorted data
  - Super pixel isolation
    - Search for neighbouring SuperPixels
- (Global firmware is more complex, many units omitted for clarity)



Validation

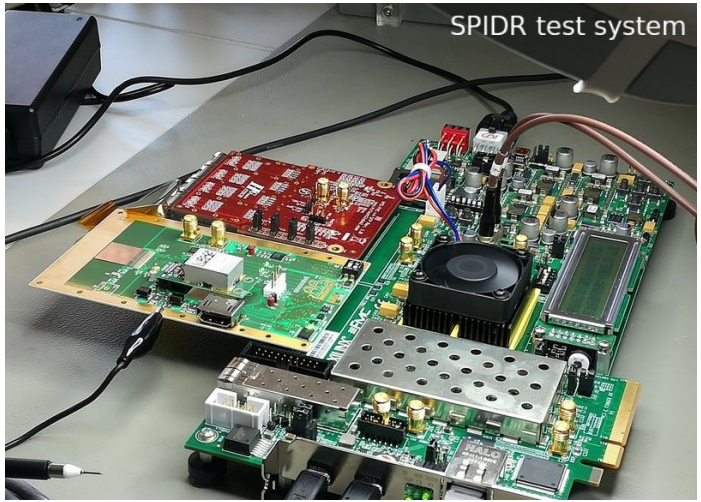
Prototype for testing





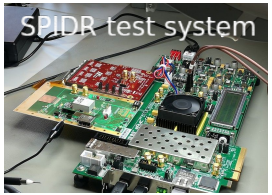
Validation of VeloPix v1

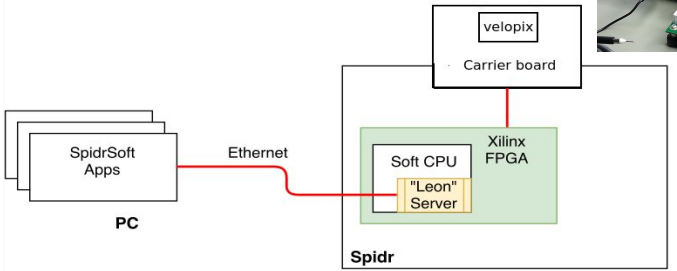
- Functional verification
  - All digital and analogue functionality has been validated and conforms to specifications
  - Verified correct operation at low temperature (-40º C)
  - Wafer probe card received. Development of test software starting
- Total Ionising Dose (TID) tested up to 400Mrad
  - No change in digital power consumption observed
  - No drift in analogue parameters:
    - pixel thresholds & noise and global DACs remain stable
- Single event effects
  - Unexpectedly found SEL (“single event latchups”)
  - SEU Errors in the reset receiver
- Excessive jitter on GWT high speed serial link
- VeloPix V2 with all the errors corrected is being produced

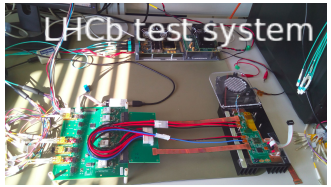


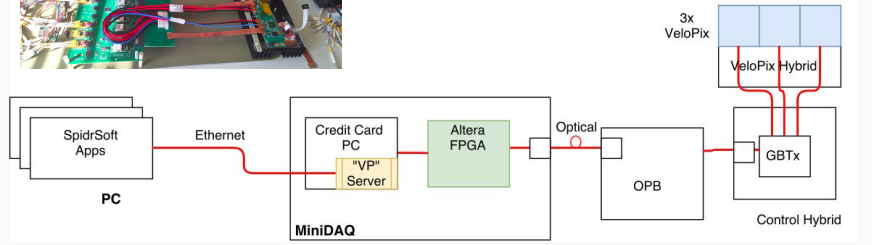
ECS on detector electronics validation

- SPIDR SYSTEM (used for VeloPix testing)
  - Xilinx VC707 board
    - Soft CPU
    - Basic DAQ
  - 1 VPX ASIC connected through a Carrier board
- LHCb test system
  - VELO test hardware
    - VeloPix Hybrid. 3 VPX ASICs connected to 1 GBTx chip
    - Flex tape (up to 50 Cm)
    - Feed-through
    - Opto Power Board (OPB)
  - Final VELO SOL40 FW with a thin server layer in CCPC (emulating SPIDR behaviour)
  - MiniDAQ V1 (Credit Card PC + Altera Stratix V FPGA)
- SPIDR ECS system was successfully migrated into LHCb test system



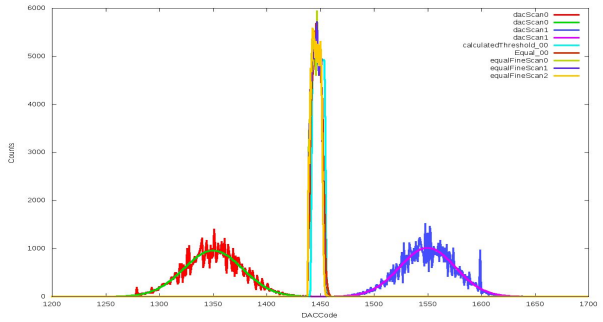






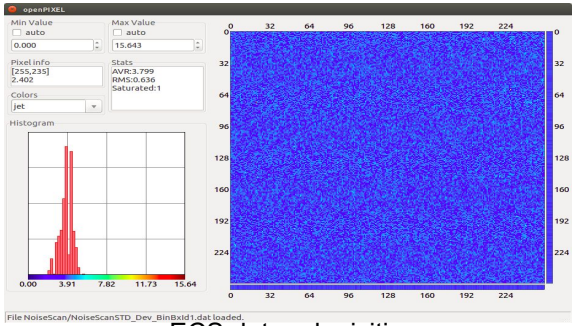
Velopix Equalization and GBT data acquisition

LHCb test system can successfully equalize and acquire data up to 3 VeloPix with similar results as SPIDR

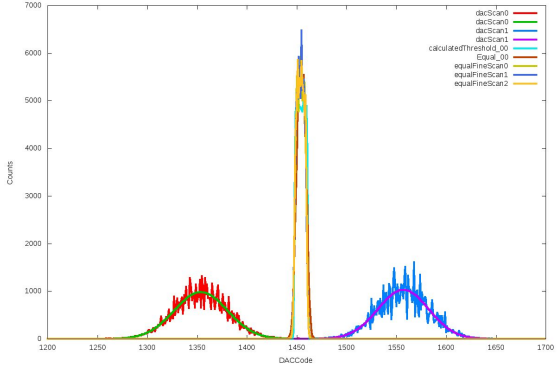


VeloPix Equalization

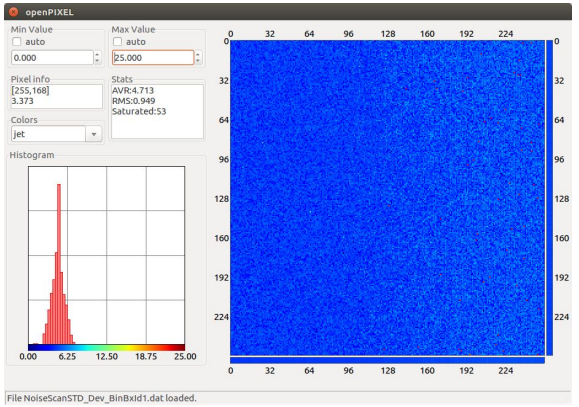
LHCb test system



ECS data adquisition

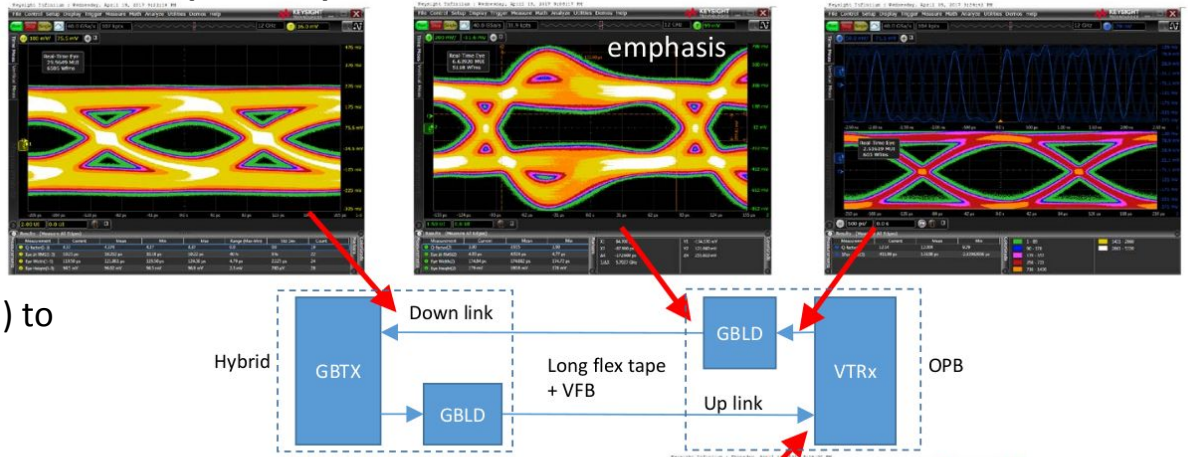


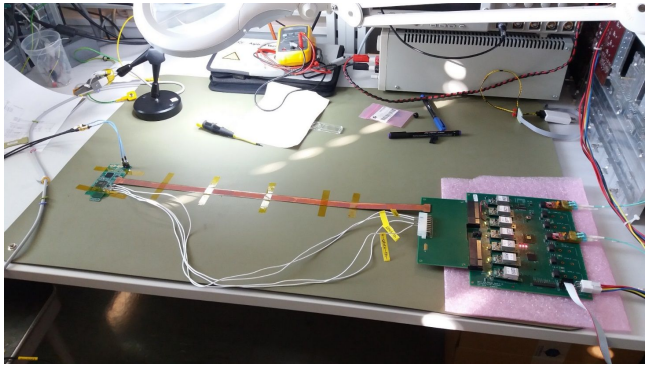
SPIDR system

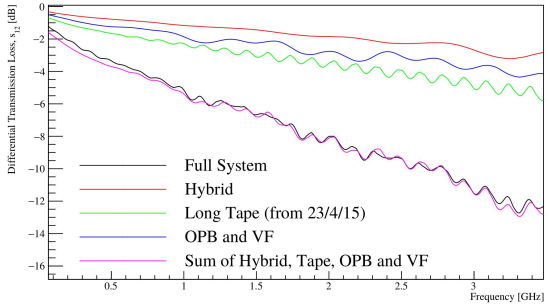


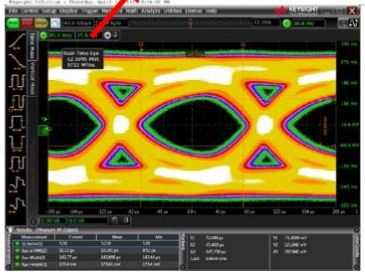
Transmission quality of high speed signals (GBT)

- GBLD used as line driver
  - Radiation hard
  - Equalizer functionality
- Good eye quality
- Will add a CTLE (OPB and hybrid) to improve eye

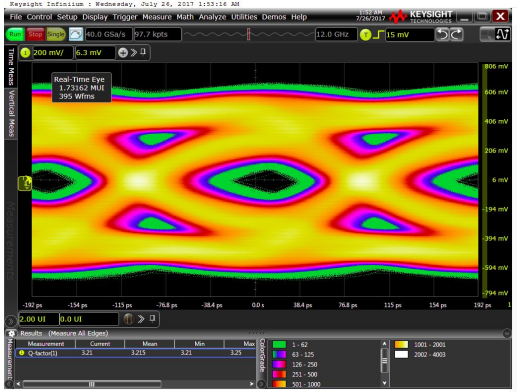




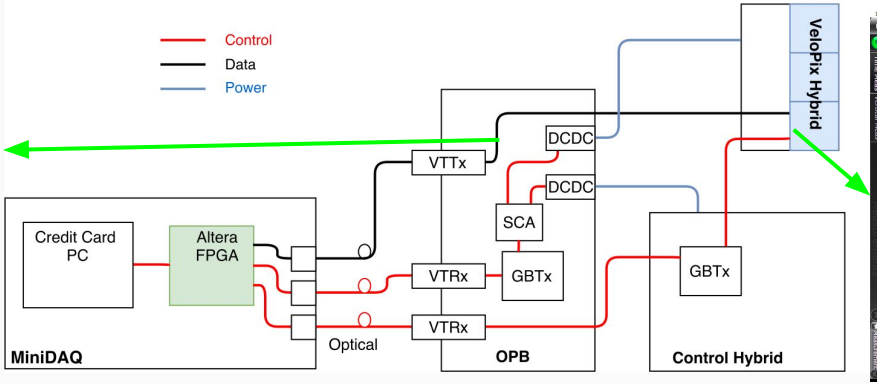




Transmission quality of high speed signals (GWT)

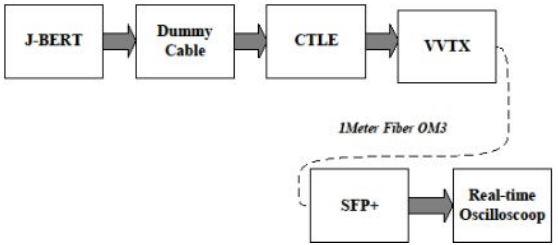


Eye diagram for the best PLL phase



VeloPix 320 MHz clock

- VeloPix 320 MHz clock with huge jitter that causes this bad eye diagram
  - Known error from VeloPix
  - For VeloPix 1 we can improve the quality by adding external on-chip decoupling, shorted bond wires, optimizing internal clock phase … (under test now)
  - **320 MHz clock optimized for VeloPix 2**
- CTLE will also be implemented and has already been tested
  - BER without CTLE => 1 e-7
  - BER with CTLE
    - 325 meters of optical fiber => 1.297 e-15



VELO Off-detector firmware and software

- SOL40
  - Up to 3 VeloPix Successfully controlled through GBTx
  - OPB successfully controlled and monitored through GBTx and SCA chips
  - WinCC Panels has been created for the control of the system
- TELL40
  - All VELO specific blocks was successfully simulated
  - Currently working on characterization of the quality of GWT data links coming from VeloPix
    - BER test are performed in the altera transceiver
  - System is been tested with fiber loopbacks
  - Slow control and monitoring registers are under implementation
  - VELO TELL40 data acquisition will be complete soon
- SOL40 and TELL40 are being migrated from MiniDAQ V1 (stratix V FPGA) into MiniDAQ V2 (arria 10 FPGA)

Summary

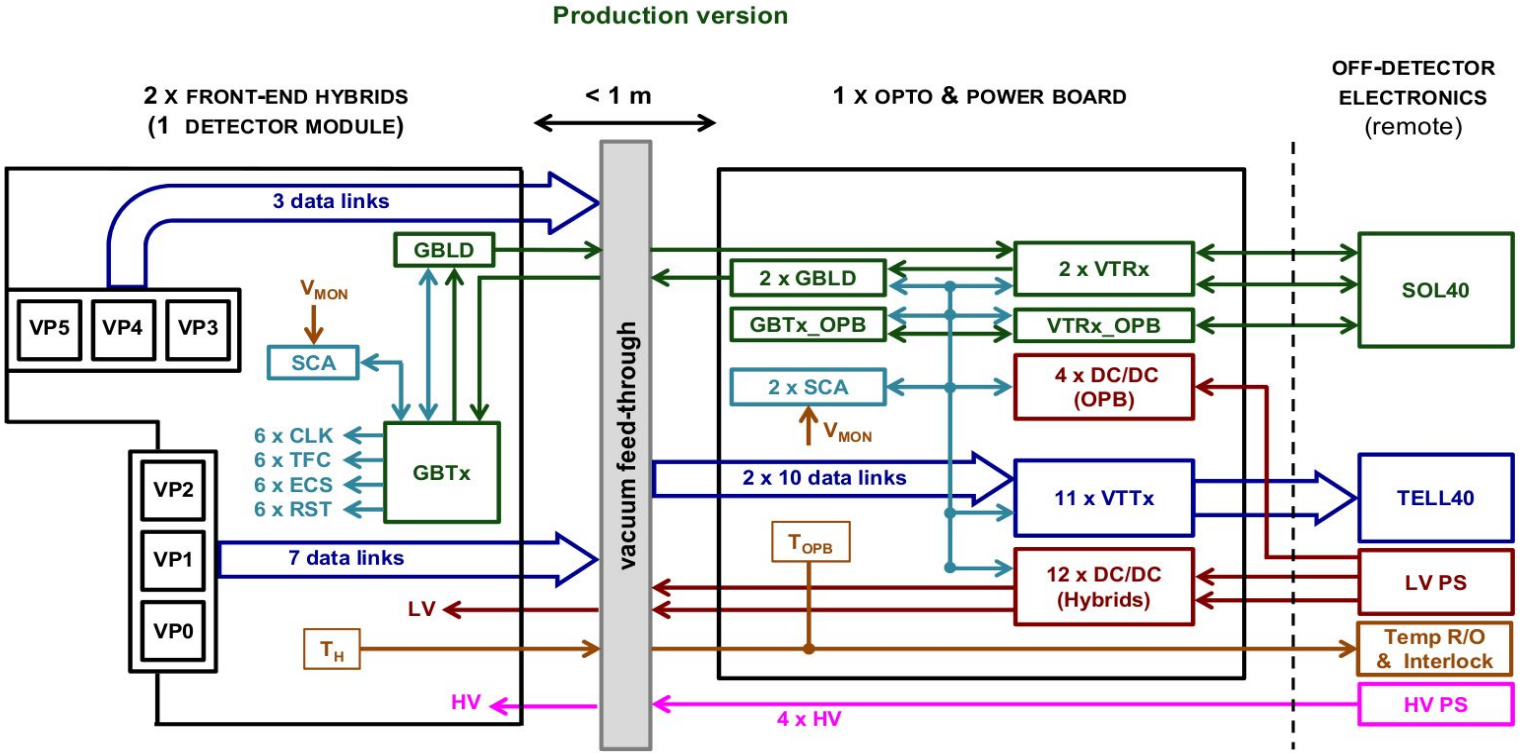
- Upgraded LHCb VELO experiment will be installed during the LHC LS2 shutdown, currently scheduled to in 2020
- Redesign VELO in order to improve:
  - Radiation tolerance
  - Better resolution
  - Readout data rate up to 40 MHz
  - Distance to the beam
- Prototype systems has been successfully integrated and validated
- Pre-series versions of the final hardware are been produced now
- VELO control firmware is working
- VELO Data acquisition firmware is been implemented and validated with the prototypes
- Module production will start soon (Very tight schedule)
  - Preliminary version of the entire firmware will be released in order to test the modules

THANK YOU

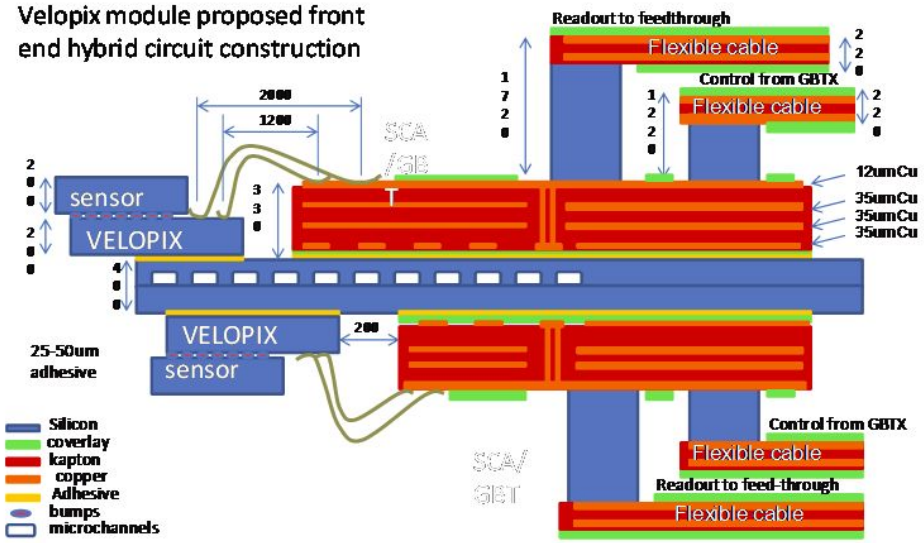
Questions?

BACKUP

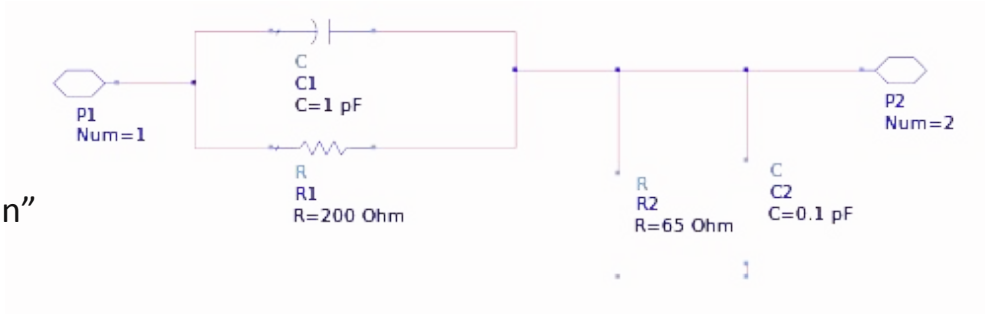
Electronics schematic



VeloPix-hybrid connection



CTLE



- CTLE = “Continuous Time Linear Equalisation” = passive high pass filter (1 zero, 1 pole).
- Compensate signal distortion, but loss of signal amplitude.

$$H_{ctle}(s) := \frac{R_2}{R_1 + R_2} \cdot \frac{(1 + R_1 \cdot C_1 \cdot s)}{1 + \frac{R_1 \cdot R_2}{(R_1 + R_2)} \cdot (C_1 + C_2)s}$$

High speed data link test