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Validation of the Front-End Electronics and Firmware for LHCb Vertex Locator.

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The LHCb Experiment will be upgraded to a trigger-less system reading out the full detector at 40 MHz event rate with all selection algorithms executed in a CPU farm. The upgraded Vertex Locator (VELO) will be a hybrid pixel detector read out by the “VeloPix” ASIC with on-chip zero-suppression. This talk will present the systems overview and design of the VELO on-detector electronics and readout firmware. Results will show the evaluation of the prototypes boards and readout firmware.

Summary

The upgrade of the LHCb experiment will be installed during the shut-down of LHC operations in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. It will be a hybrid pixel detector read out by the VeloPix ASIC. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s,
adding up to 1.6 Tbit/s of data for
the 40 Mpixels of the whole VELO.
This talk will present the architecture and the design of the VELO electronics,
describing each
component and how they interface to each other and to the LHCb common frame. Its main components are the VeloPix ASIC at 5 mm from the beam in a secondary vacuum tank and extremely high and inhomogeneous radiation environment,
the Opto- and Power Board (OPB) outside of the vacuum,
but
still in a high radiation environment.The LHCb readout (TELL40) and front-end control (SOL40) boards are placed in a radiation free environment on the surface.
The front-end hybrid hosts the VeloPix ASIC as well as the GBTx ASIC which provides the control signals and clocks for the VeloPix. The VeloPix transmits data packets with binary hit information and a time-stamp of 25 ns over serial highspeed electrical links at 5Gbit/s. This data is converted to optical in the OPB and sent to the TELL40 board over 300m optical links.The OPB also supplies the front end voltages using DC/DC conversion.
Each of the 52 TELL40 boards handles all 20 data links from a single module. All control of the front-end electronics is handled by 4 SOL40 boards. The firmware of VELO TELL40 boards is based on the LHCb common framework. However,
due to the non time ordered data stream from the VeloPix ASIC
and the specific data transfer protocol (GWT) about 80% of the code has to be customised for VELO.
Prototypes for all components of the whole readout chain,
including firmware,
have been integrated
and tested.The results and experience gained from these test will be presented.

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