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Design and Results from a Front-End Board for Micromegas Chambers in the ATLAS New Small Wheel

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The design and implementation of demonstrator front-end electronics for Micromegas detectors to be employed in the New Small Wheel, an ATLAS muon spectrometer upgrade, are presented. The demonstrator has 512 Micromegas detector channels as input. Signal processing and digitization utilize a custom ASIC developed by Brookhaven National Lab. Configuration, control and Ethernet readout functions are performed using an Artix-7 FPGA. Design constraints and considerations are discussed. Measurements of noise performance, both off- and on-detector, are presented. Results using an Fe-55 source are also shown. Design considerations for the final front-end electronics to be used in the ATLAS experiment are discussed.

Summary

The design and implementation of demonstrator front-end electronics for Micromegas detectors to be employed in the New Small Wheel (NSW), an ATLAS muon spectrometer upgrade, are presented. In order to improve the performance of the ATLAS end-cap muon system in response to ever-increasing luminosity of the Large Hadron Collider (LHC), the Level-1 trigger capability must be augmented. Adding hit information from the innermost layer of the end-cap muon system will significantly reduce the Level-1 trigger rate associated with combinatoric sources. Small-strip Thin Gap Chambers (sTGC) and Micromegas detectors (MM) will comprise the ATLAS New Small Wheel and provide improved triggering and reconstruction capability.
The MM detectors are constructed using a resistive strip design. The strip pitch for the MM front-end board is 400 um and the NSW system (both end-caps) consists of approximately 2 million strips. The front-end board has inputs for 512 MM channels, hence 4096 front-end boards are required for NSW system. The electrical connections between the front-end board and MM detectors are two elastomeric connectors. The connectors are made of silicon rubber with six rows of gold plated contacts spaced with 50 um pitch. G10 holders are used to hold the two connectors for each front-end board. A compression system that is part of the MM system bar provides the necessary clamping force. Input protection on the front-end board consists of a set of TVS diodes.
Signal processing and digitization utilize a custom ASIC, called the "VMM", developed by Brookhaven National Lab. Each VMM ASIC has 64 channels. Each channel contains an amplifier with adjustable gain and shaper. Signals passing a sub-hysteresis discriminator have their peak amplitude and times digitized by 10-bit and 8-bit ADC's respectively. The discriminated signal also provides an address-in-real-time that can be as part of the MM trigger. Digitized data are buffered and subsequently readout using a two-bit serial output. There are eight such VMM ASIC's on the front-end board.
This demonstrator version of the front-end board utilizes an Artix-7 FPGA for configuration, control and Ethernet readout functions. MicroBlaze is used to communicate with the on-board Ethernet PHY. The final version of the front-end board will utilize two custom ASIC's for the configuration and control functionality. The demonstrator version also makes use of commercial DC-DC converters and low dropout regulators for power. The final version will utilize a radiation tolerant DC-DC converter developed by CERN.
Noise measurements are made using an oscilloscope connected to a monitor output for the analog signals from the VMM ASIC's. These measurements are cross-checked by a similar set of measurements using the

XADC functionality of the FPGA. Data are also collected and analyzed using a small test MM chamber with 256 readout channels. Using an Fe-55 source, a clear photopeak and Argon escape peak are observed and the energy resolution for this MM detector is approximately 12%.

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