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Demonstrating TTC-PON Robustness and Flexibility

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In 2016, a TTC-PON (Timing, Trigger and Control system based on Passive Optical Networks) demonstrator was presented at TWEPP as an alternative to replace the TTC system, currently responsible for delivering timing, trigger and control commands in the LHC experiments. Towards a deployment foreseen for ALICE phase-1 upgrade, the system has been consolidated through flexible software implementation providing full configuration, complete calibration and extended monitoring and diagnostic tools. A scaled-up setup was built with various FPGA platforms to stress the system in realistic conditions. The system and its features will be demonstrated together with a discussion on its robustness.

Summary

The TTC-PON system (Timing, Trigger and Control system based in Passive Optical Networks) was first envisaged in 2010 as an alternative to the current TTC system, responsible for timing distribution, and for sending level-1 trigger accept and control commands from the central trigger unit to the detector sub-partitions of the CERN LHC (Large Hadron Collider) experiments. TTC-PON is a bidirectional point-to-multipoint optical communication system in which a master node can communicate with slave nodes over the same fiber using WDM (Wavelength Division Multiplexing) and TDMA (Time Division Multiplexing Access). Compared to the current TTC system, TTC-PON has a much higher bandwidth and allows bidirectional optical communication between the master and slaves. In addition, TTC-PON masters can serve more slave nodes (up to 64) when compared to the current system (up to 32).

Since the TTC-PON will be installed in the back-end of the experiments, COTS (commercial off-the-self) optical components and FPGAs (Field Programmable Gate Arrays) are used for the system implementation. In 2016, a demonstrator based on the XGPON1 technology was presented overcoming major limitations of past solutions. The system can handle up to 64 slave nodes per master with a comfortable optical margin and the TDMA is based on 125 ns timing slots allocated to each slave. This demonstrator was based on a single manufacturer for the optical components and all the nodes of the system were implemented using Kintex7 FPGAs by means of KC705 evaluation boards (Xilinx).

Since then, the FPGA firmware has been consolidated and is being prepared for a full deployment in the framework of ALICE phase-1 upgrade. The proposed system is now fully software configurable with a very flexible design based on Python; several features have been made available to the users in order to have full configuration and calibration procedures and extended online and offline monitoring tools of the system. An improved setup consisting of one master and eight slaves has been built. Based on Kintex Ultrascale and Arria 10 development platforms, as well as on PON transceivers from several vendors, this new test bench allowed to perform stress tests (extended bit error ratio tests, temperature, long fibers, dynamic range⋯) in order to better understand system limitations and to improve its robustness.

This paper will focus on the current core design and a demonstration of its features will be performed. The system stress tests results and the robustness of the current setup will also be discussed.

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