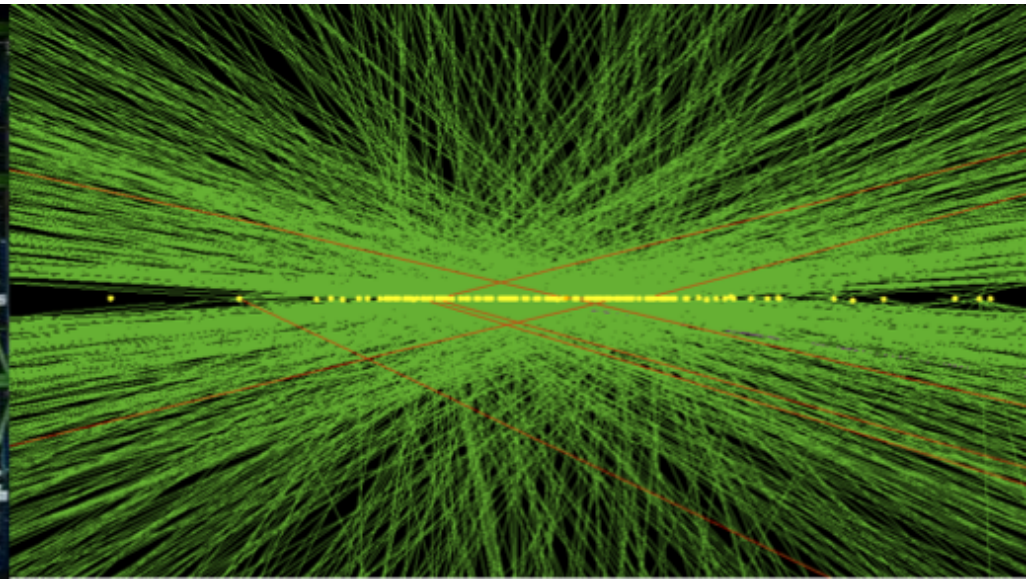
Prospects for a Precision Timing Upgrade of the CMS Crystal Electromagnetic Calorimeter for the HL-LHC

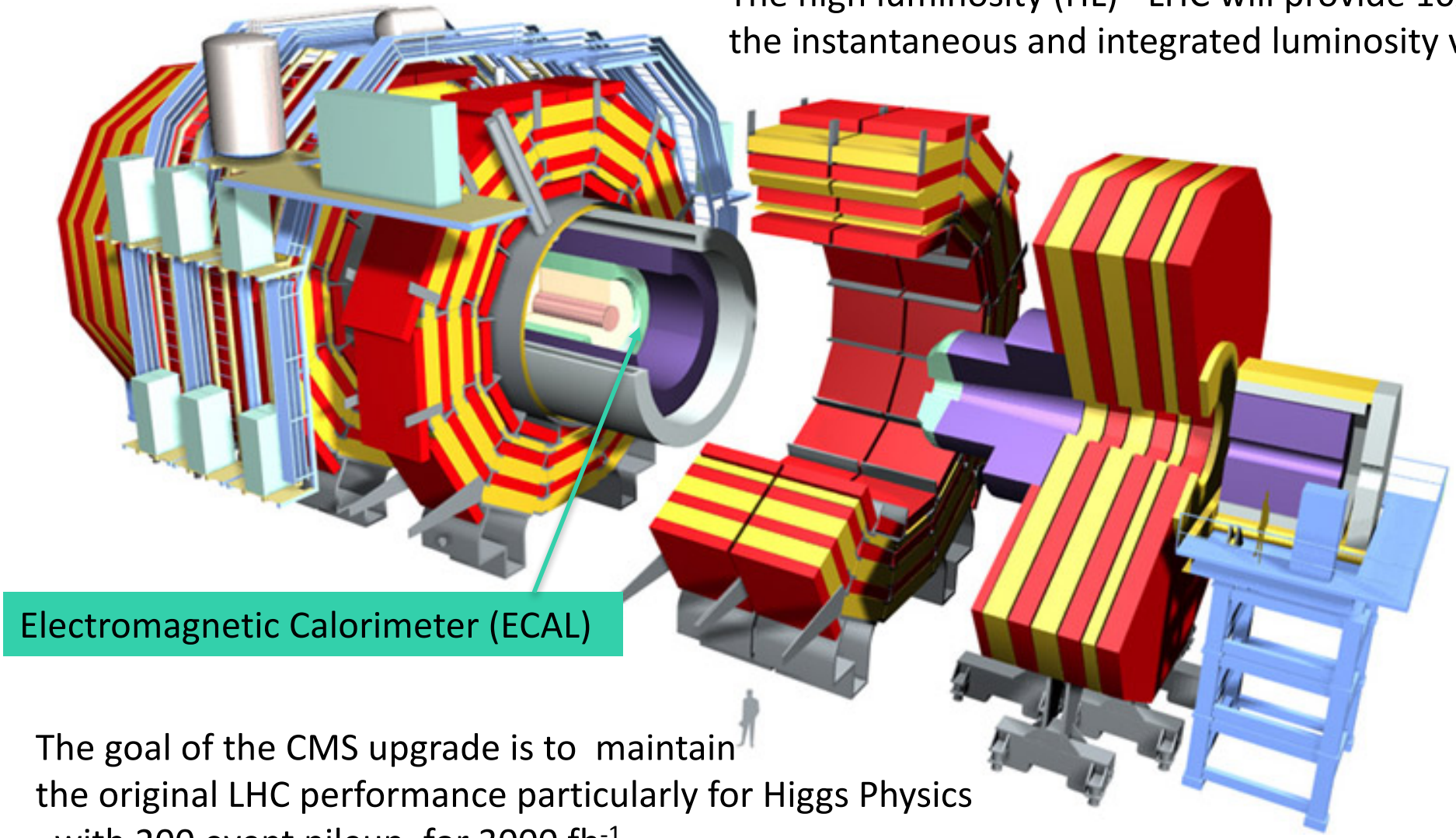
Colin Jessop
University of Notre Dame

for the CMS Collaboration
September 14, 2017



The CMS detector at the (HL) LHC

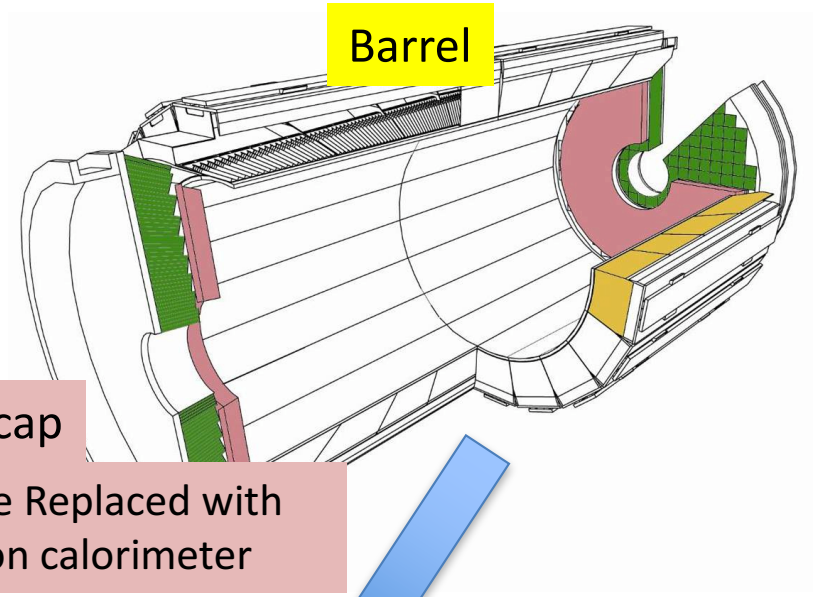
The high luminosity (HL) –LHC will provide 10x the instantaneous and integrated luminosity vs LHC

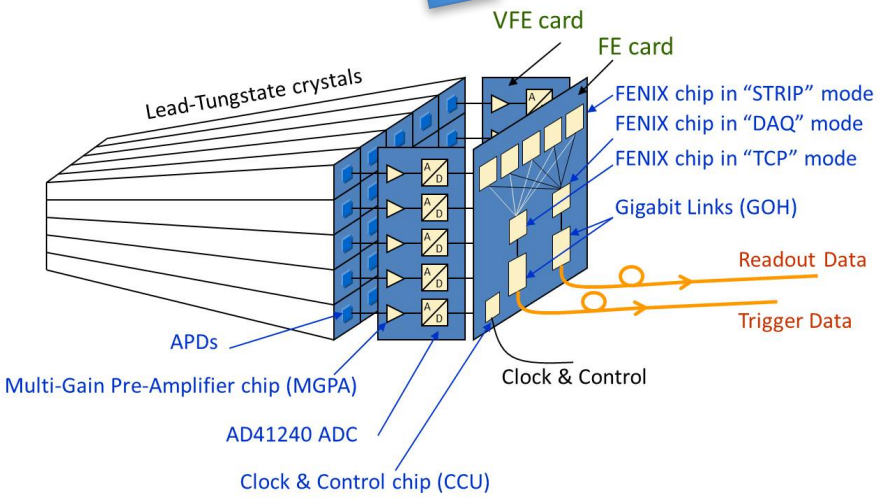


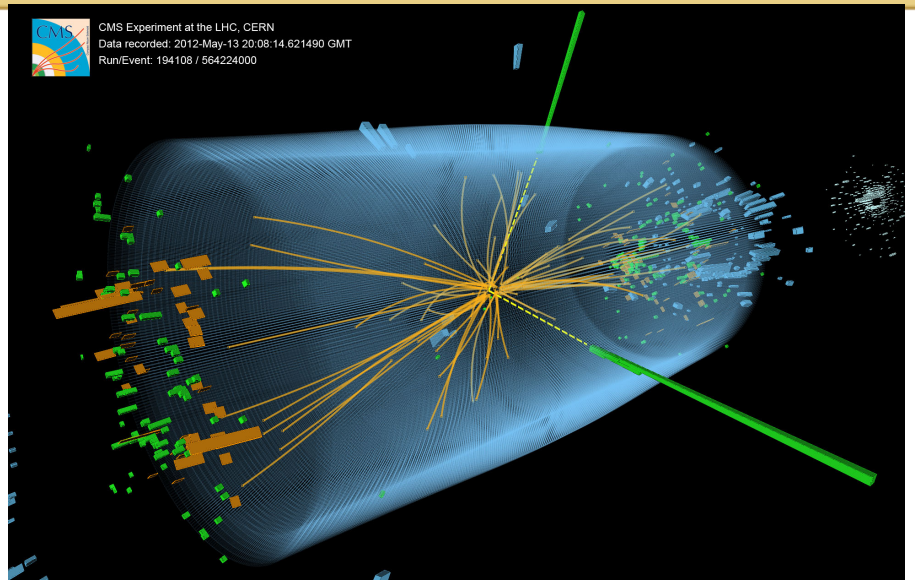
Electromagnetic Calorimeter (ECAL)

The goal of the CMS upgrade is to maintain the original LHC performance particularly for Higgs Physics , with 200 event pileup, for 3000 fb^{-1}

The Barrel Electromagnetic Calorimeter





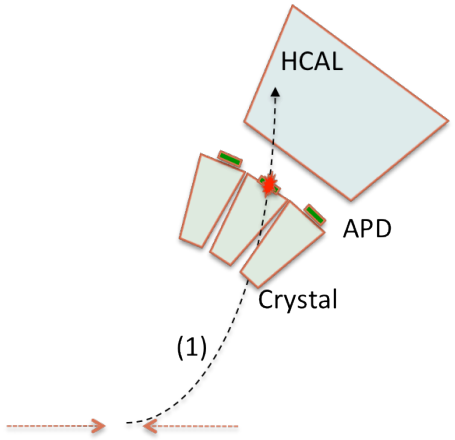


A $H \rightarrow \gamma\gamma$ candidate event observed in the ECAL

Parameter	Barrel
η coverage	$\lvert\eta\rvert < 1.5$
# crystals	61200
Granularity	36 supermodules

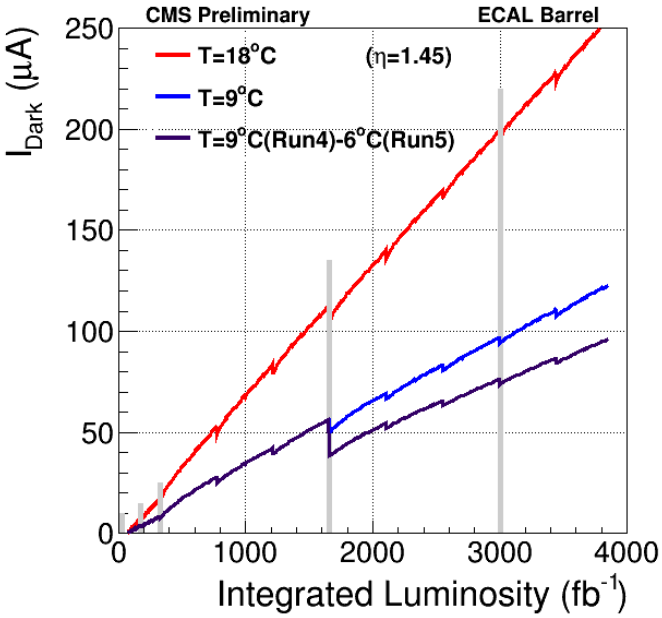
ECAL Barrel Upgrade Technical Requirements

1. Accommodate HL-LHC trigger requirements to be able to trigger on Higgs Bosons



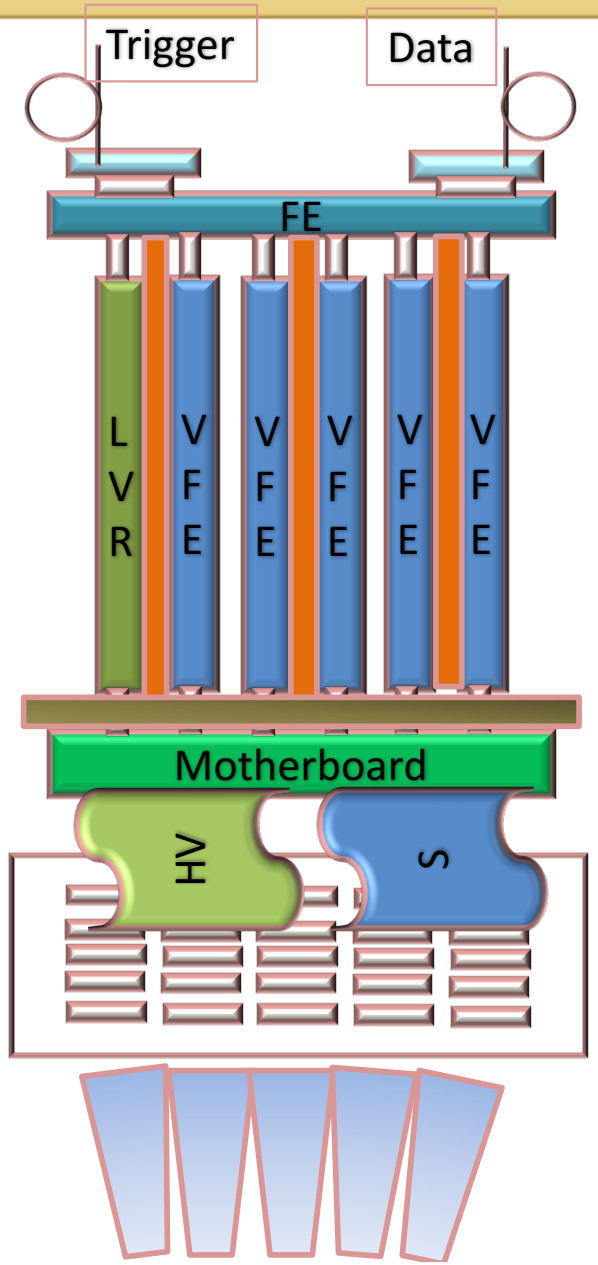
2. Provide 1x1 crystal info to trigger instead of present 5x5. Better isolation and also better spike rejection

	Max Level 1 Accept Rate	Max Latency
Trigger Phase 2	750 kHz	12.5 μS
ECAL Phase 1	150 kHz	6.4 μS



3. Cool photodetectors (18->9°C) to reduce noise increase due to radiation damage. Also change pre-amp for more optimal noise filter and 30ps timing @40 GeV to suppress spikes and pileup

Legacy On-detector Electronics



1.6 GB/s

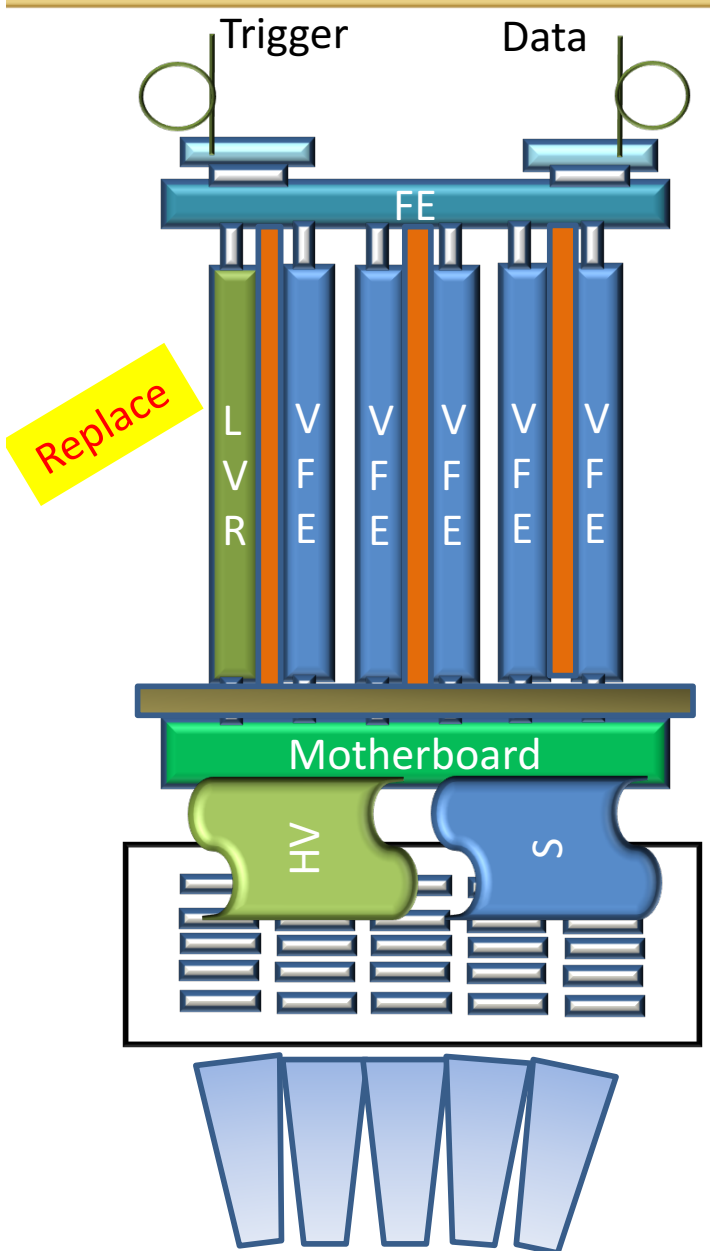
FE = Front End. Forms sum of 5 crystals in a strip For trigger primitive and has latency buffer to store data while waiting for L1 accept

VFE = Very Front End. Preamp, Shaping and ADC

Motherboard is passive – basically just a connector HV and LV to APD and signals to VFE

Crystals with two Avalanche Photodiodes (Connected so I channel per 2 APD's)

Upgraded On-detector Electronics



Replace 36 Gb/s

FE = Front End passes single crystal information to the back end. No latency buffer in front end

Replace

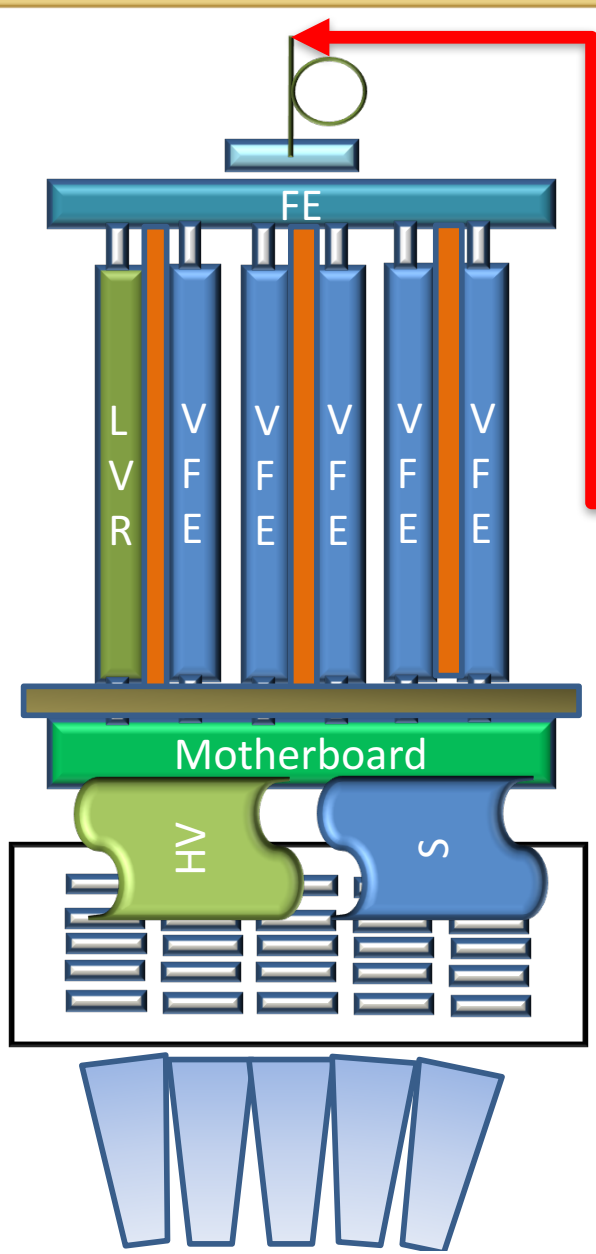
VFE = Very Front End. Preamp, Shaping and ADC

Motherboard is passive – basically just a connector HV and LV to APD and signals to VFE

Cool

Crystals with two Avalanche Photodiodes (Connected so I channel per 2 APD's)

Upgraded Off Detector Electronics



L1 Trigger

Trigger Concentrator

36 GB/s Data

Data concentrator

DAQ

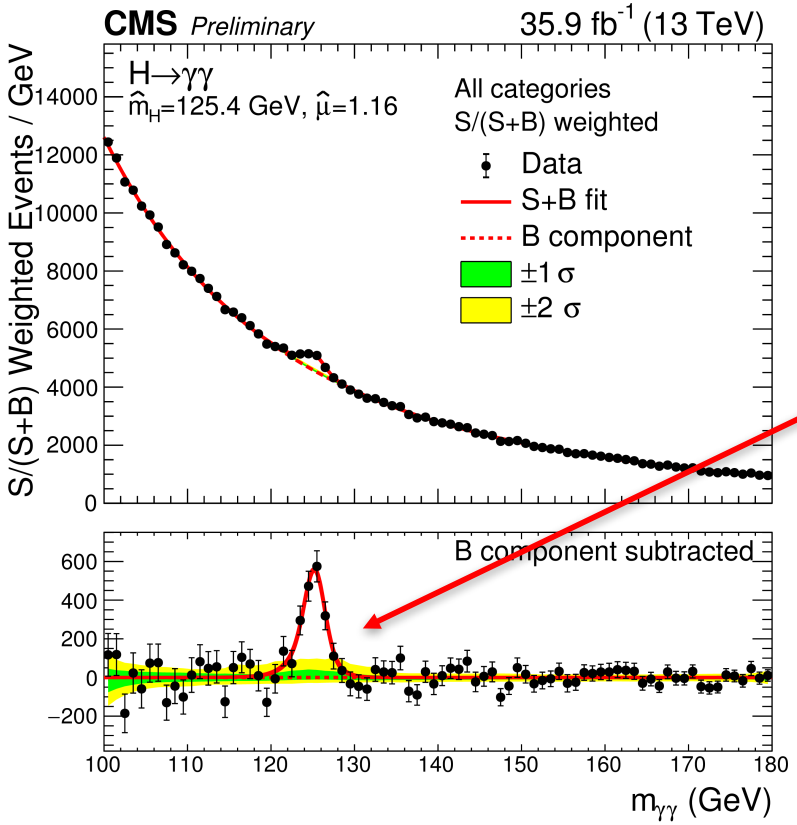
Clock Control

Clock and Control

System Clock and Detector Control System (TCDS)

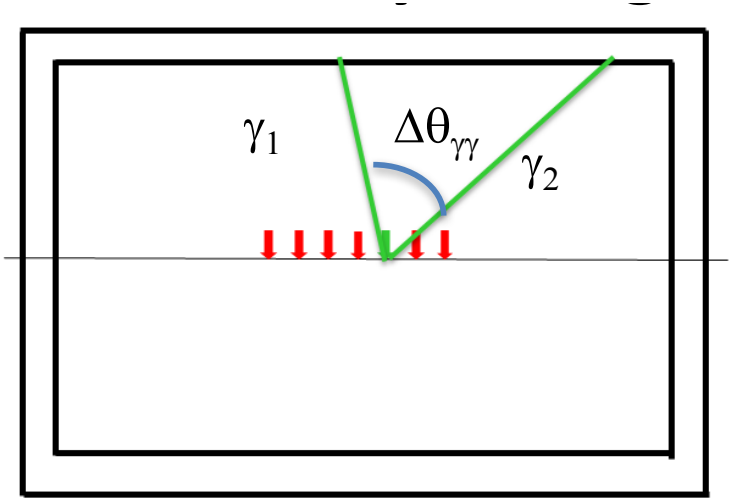
Single Board ATCA Board called the Barrel Calorimeter Processor (BCP) using powerful modern FPGA's

H→γγ in high pileup



The vertex resolution contributes to the mass resolution in addition to energy resolution

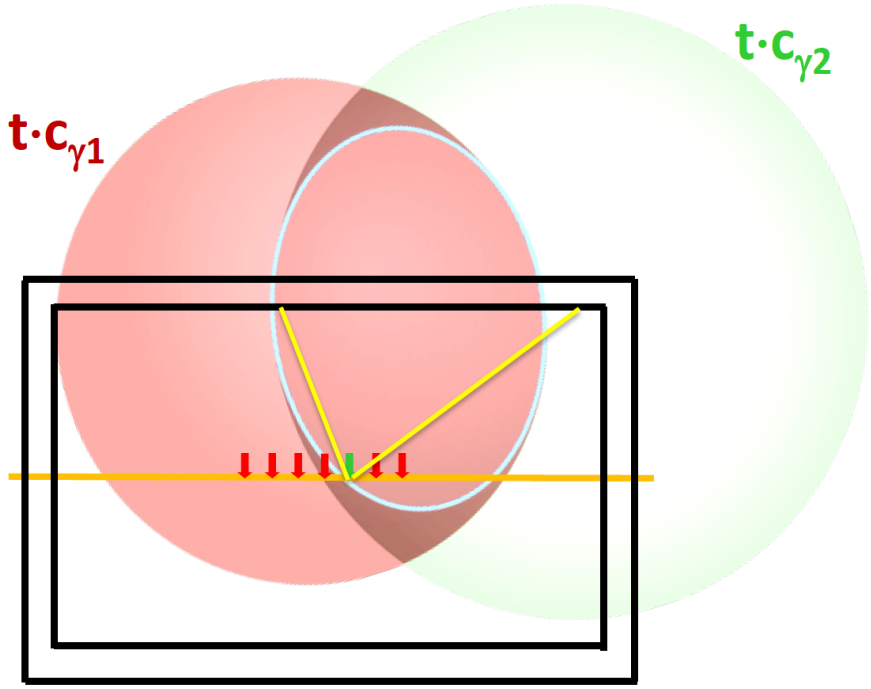
$$\frac{\Delta m_{\gamma\gamma}}{m_{\gamma\gamma}} = \frac{1}{2}\left[\frac{\Delta E_{\gamma 1}}{E_{\gamma 1}} \oplus \frac{\Delta E_{\gamma 2}}{E_{\gamma 2}} \oplus \frac{\Delta\theta_{\gamma\gamma}}{\tan\left(\theta_{\gamma\gamma}/2\right)}\right]$$

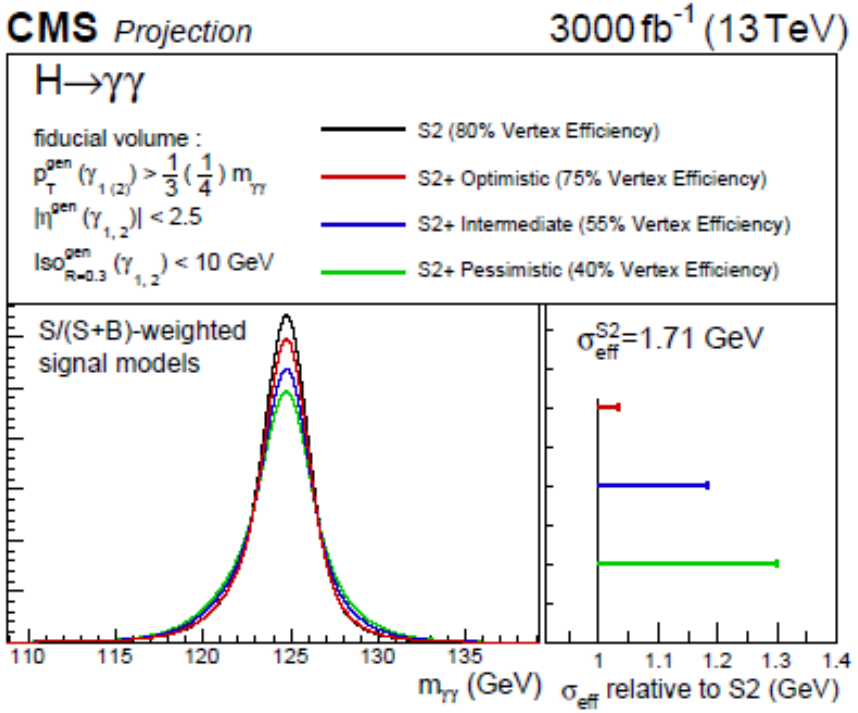


In pileup of 140 the vertex finding efficiency drops from 80% to 40% (PU20) degrading vertex resolution

Precision Timing for H→γγ

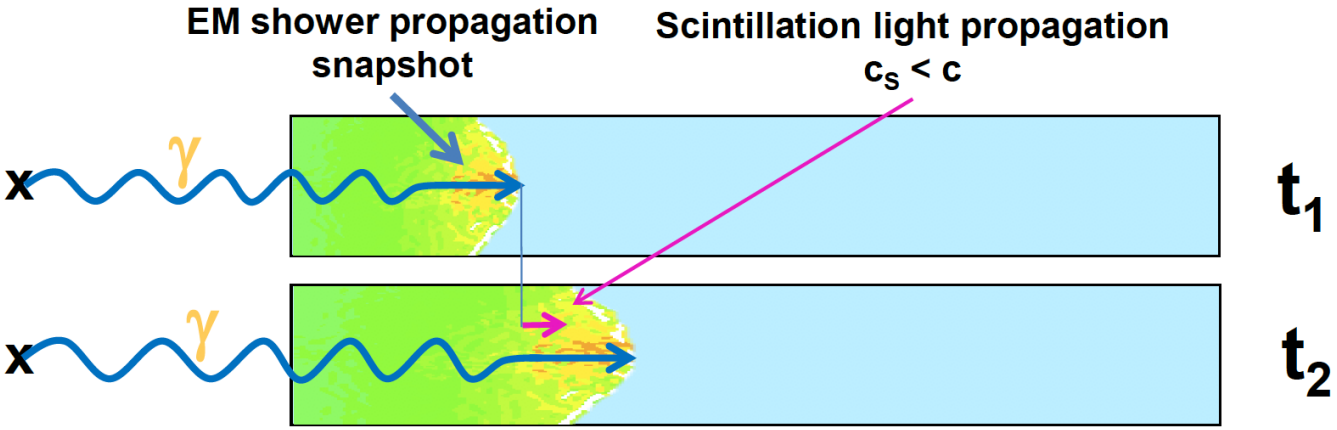
Timing is used to triangulate the vertex



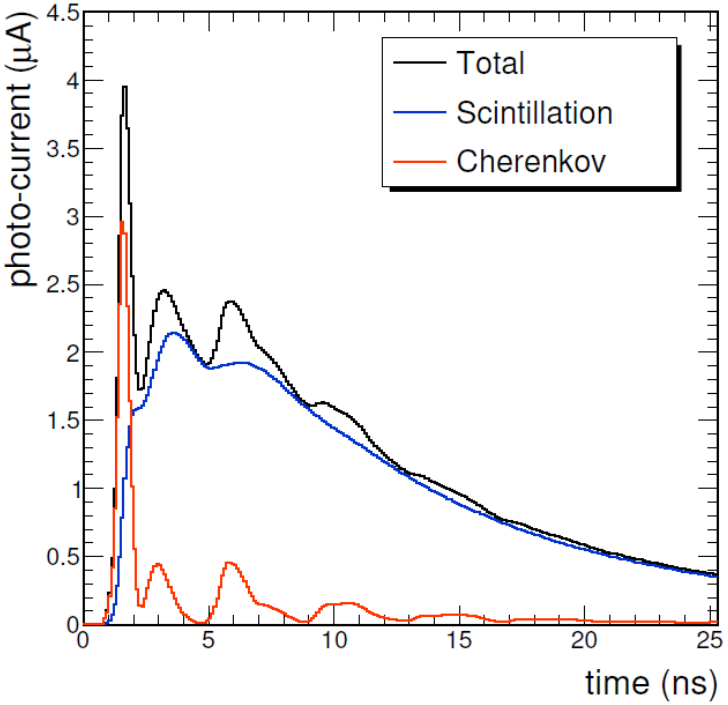


30ps photon timing recovers vertex finding efficiency from 40% to 55% and coupled with charged track precision timing to 75% (versus 80% in low pileup)

Precision timing with scintillating crystals



Detailed simulation of shower time development to optimize readout

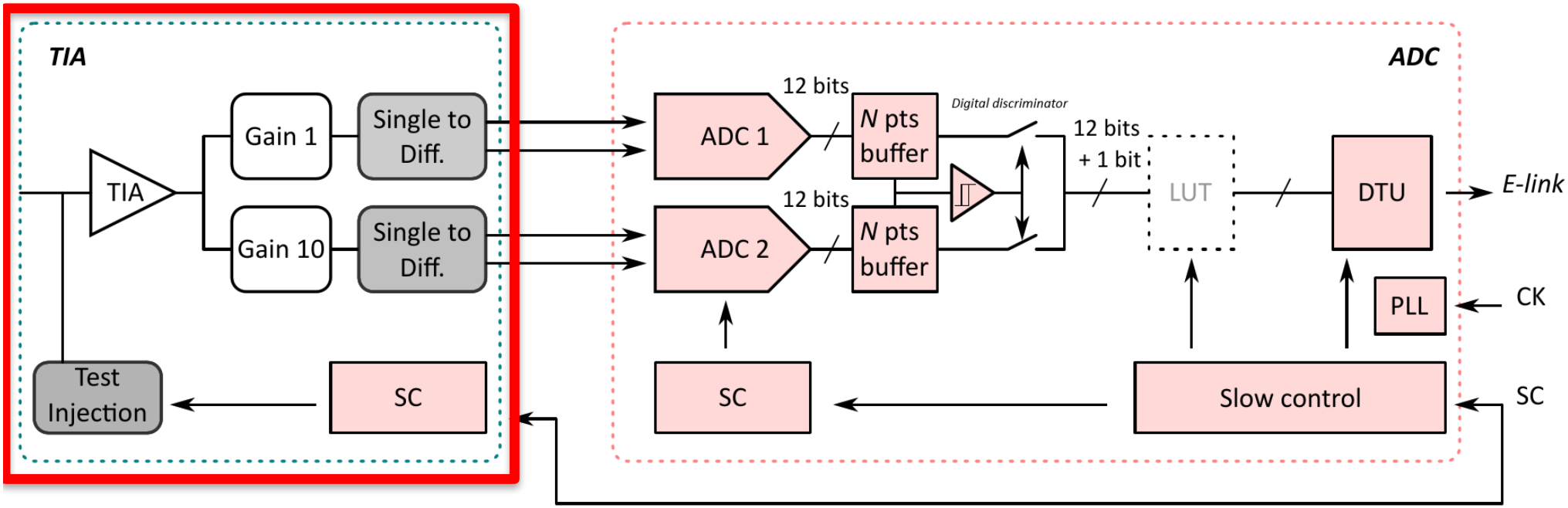


Leading edge provides the fast timing information

Fast responding pre-amp and high sampling rate to get precise timing

Shower fluctuations limit the timing resolution

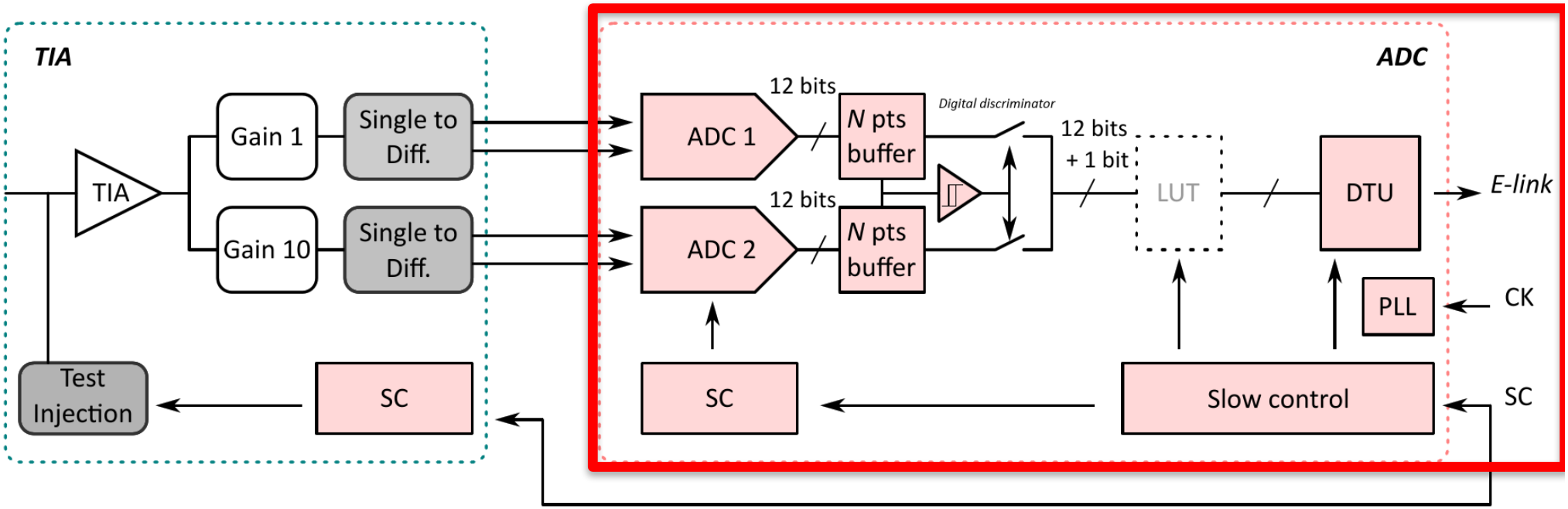
Very Front End (VFE) upgrade - PreAmp



- Transimpedance Amplifier (TIA) in 130nm CMOS for fast response to get precise timing
- Replaces legacy charge amplifier with CR-RC τ=43ns
- 12240 boards required

(See poster from Fabrice Guilloux etal on Calorimeter TIA (CATIA)ASIC)

Very Front End (VFE) upgrade- ADC-DTU

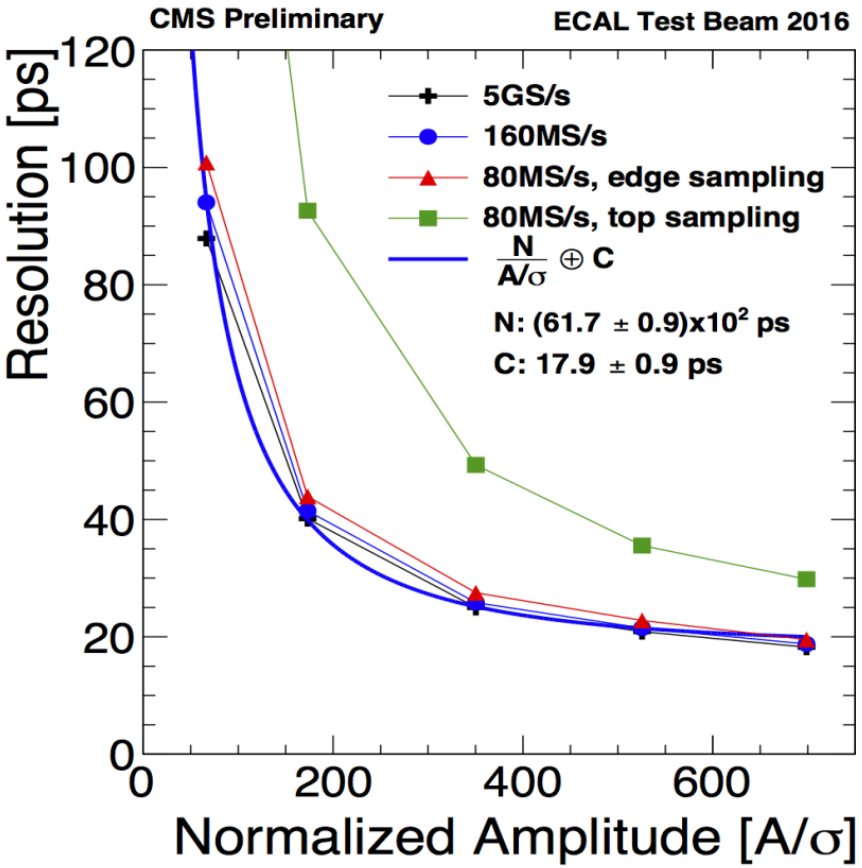


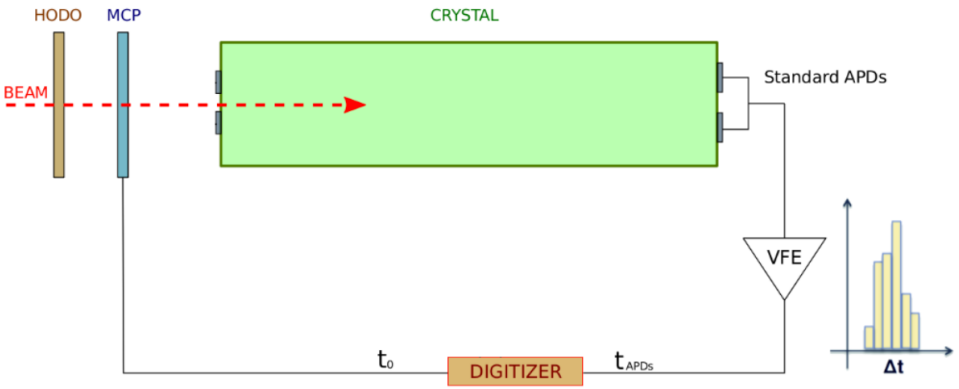
- ADC at 160 MHz versus 40 MHz in legacy system
- Data Transfer Unit (DTU) compresses (Huffman encoding) and serializes
- Commercial IP block for 12 bit SAR ADC integrated with custom DTU in 65nm CMOS

  (see poster from Simona Cornetti for more details)

Precision Timing in testbeam

$$\sigma(t) = \frac{N}{A/\sigma} \oplus C$$





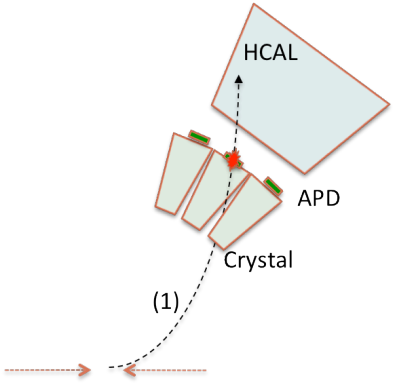
Crystal matrix with MCP to give t_0

Transimpedance VFE prototype with different sampling rates

30 ps resolution @ A/σ = 250.

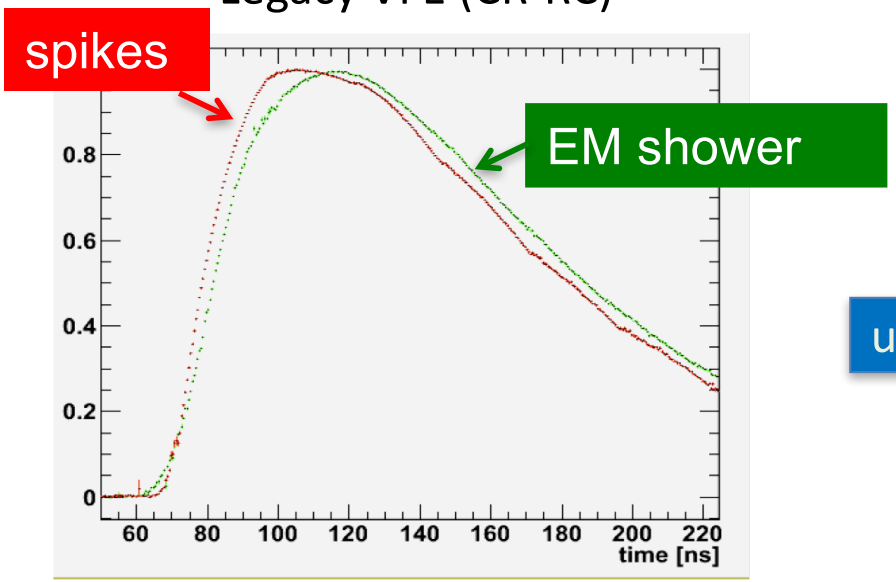
Equivalent to 25 GeV photons
(@100 MeV noise, HL-LHC start),
60 GeV (@240 MeV noise, HL-LHC end)

Precision Timing to remove Spikes



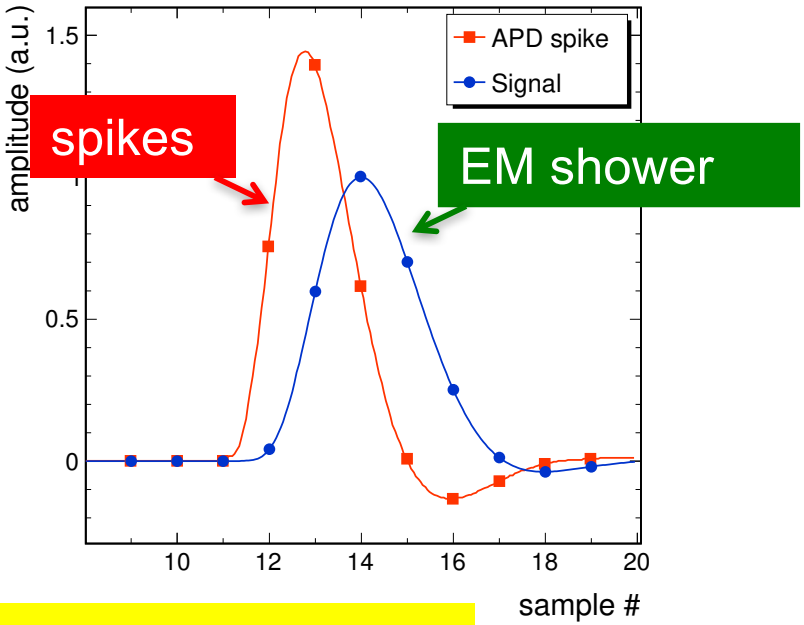
Spikes will saturate the L1 trigger bandwidth (750kHz) unless remediated with timing and isolation

Legacy VFE (CR-RC)



upgrade

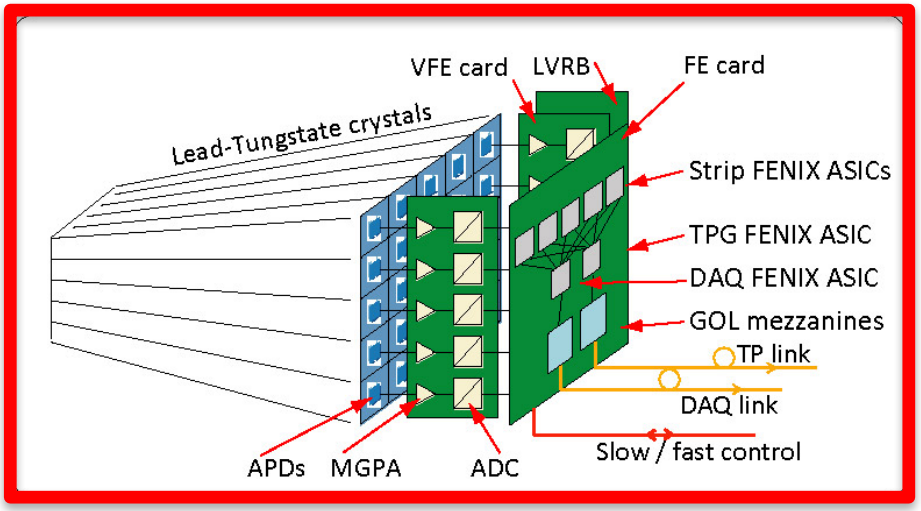
Upgraded VFE (TIA+ADC)



Shorter shaping with higher sampling allows spike discrimination with timing

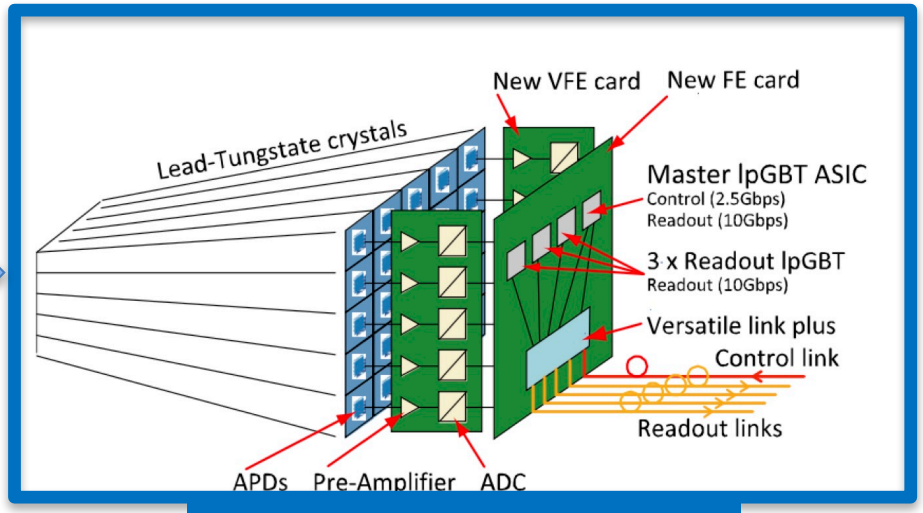
Front End Board Bandwidth Requirement

Legacy trigger tower



1.6 Gb/s output capacity

Upgrade trigger tower



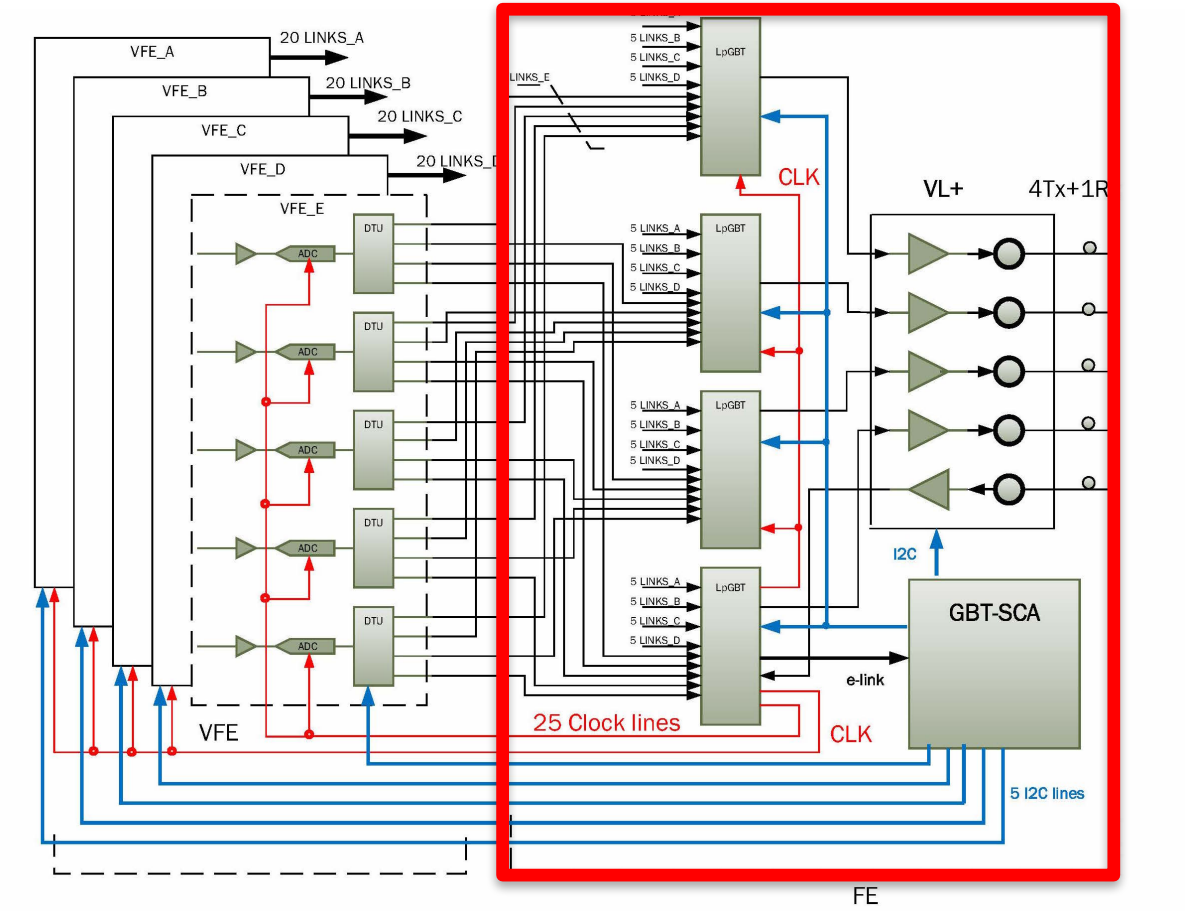
36 Gb/s output capacity

Front-End Board is functionally simpler than legacy because no trigger primitive formation (FENIX ASIC) on-detector

2448 Front-end boards required

160 MHz sampling and single crystal trigger primitive require the FE card to transmit 27 Gb/s after compression (52Gb/s with no compression)

Front End Board



Exploit CERNs low power gigabit Links (lpGBT and versalink+)

FEC5 @ 10.24Gb/s gives 8.96 Gb/s for the user data rate

4 lpGBT required for up links

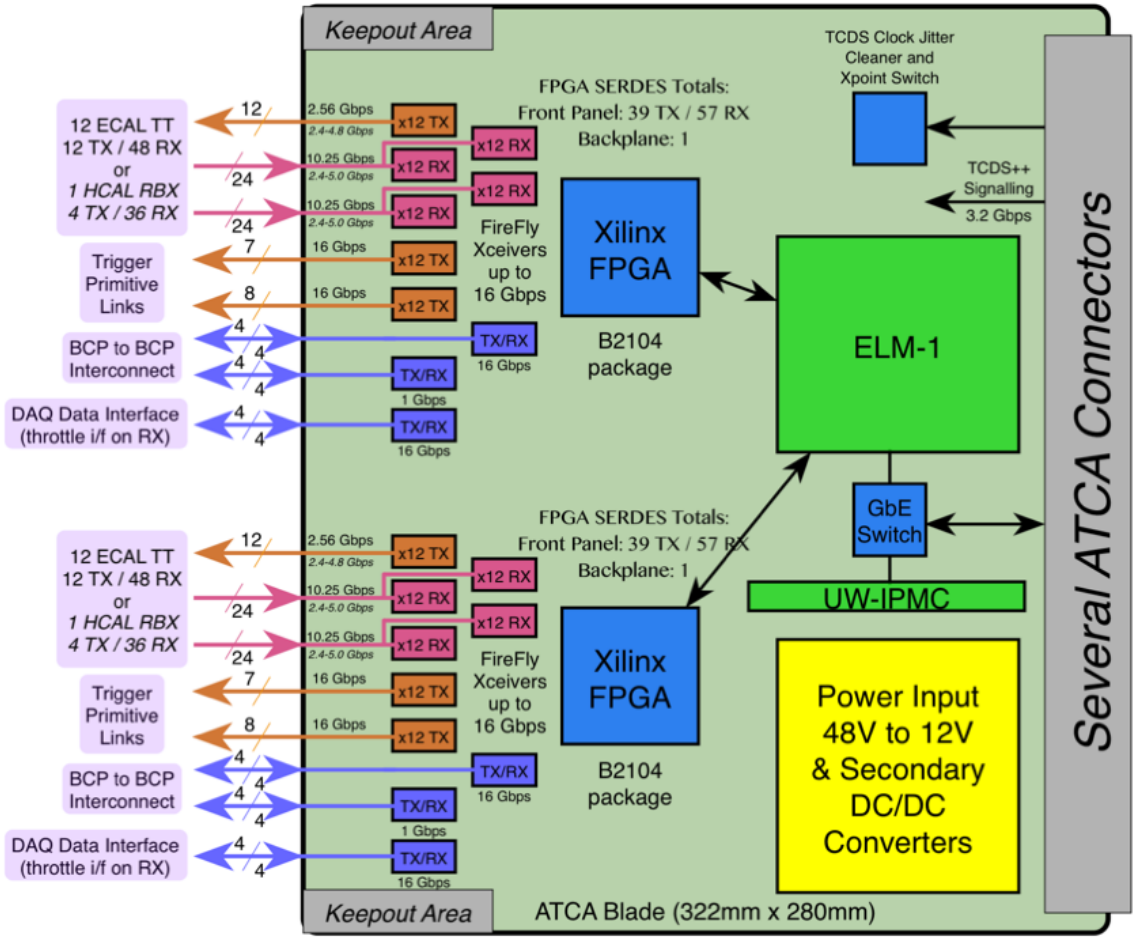
1 down link for clock and control

lpGBT has 5ps jitter spec so should be good for 30ps timing goal

Demonstrator FE with the 4.8 Gb/s GBT/versalink links produced. Awaiting lpGBT/versalink+ in 2018

UNIVERSITY OF NOTRE DAME

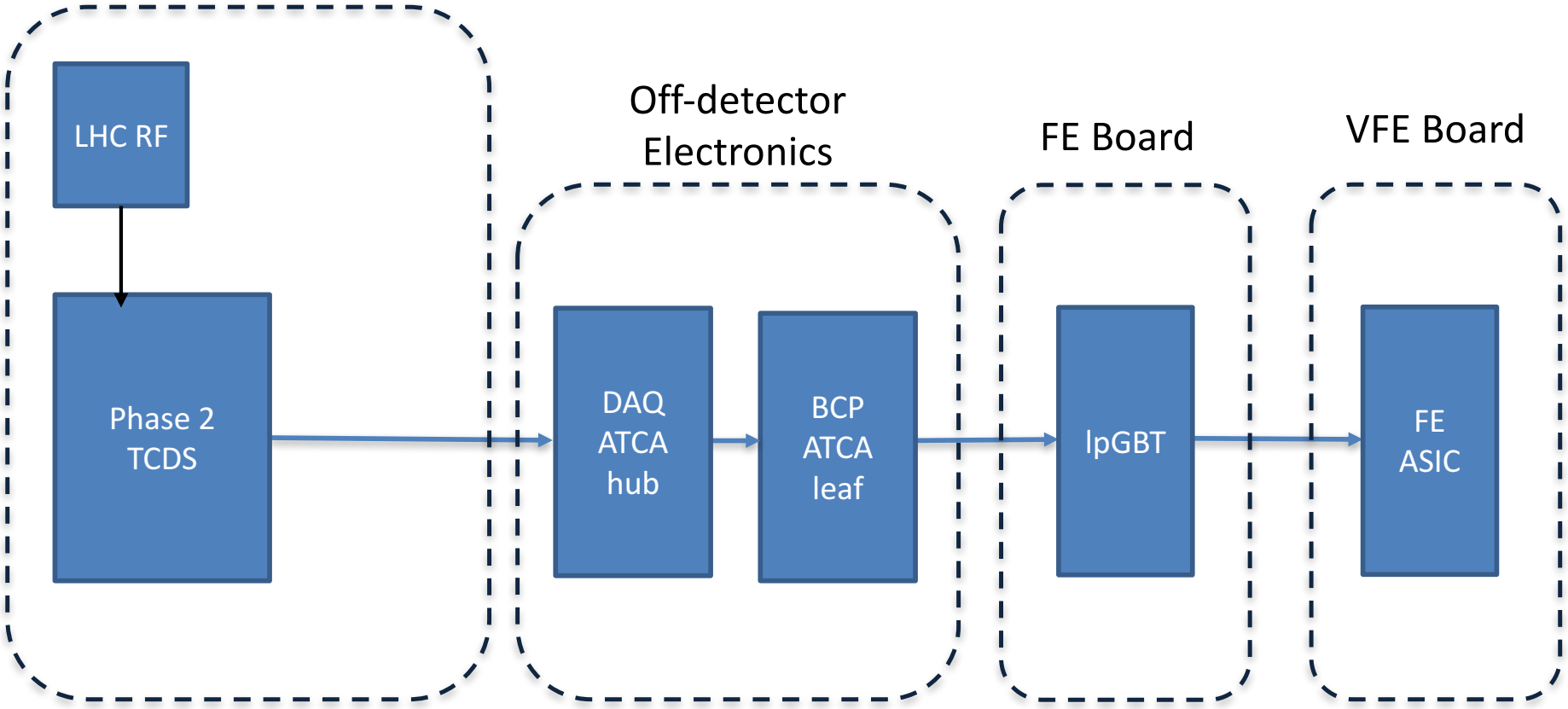
Barrel Calorimeter Processor



- 108 ATCA boards required
- Two Kintex Ultrascale XKCU115 FPGA's
- 96 input links @10.24 Gb/s from front end
- 12 output links @ 2.4 Gb/s to front-end
- 15 output links to trigger @ 16 Gb/s
- 8 outout links to DAQ @ 16Gb/s

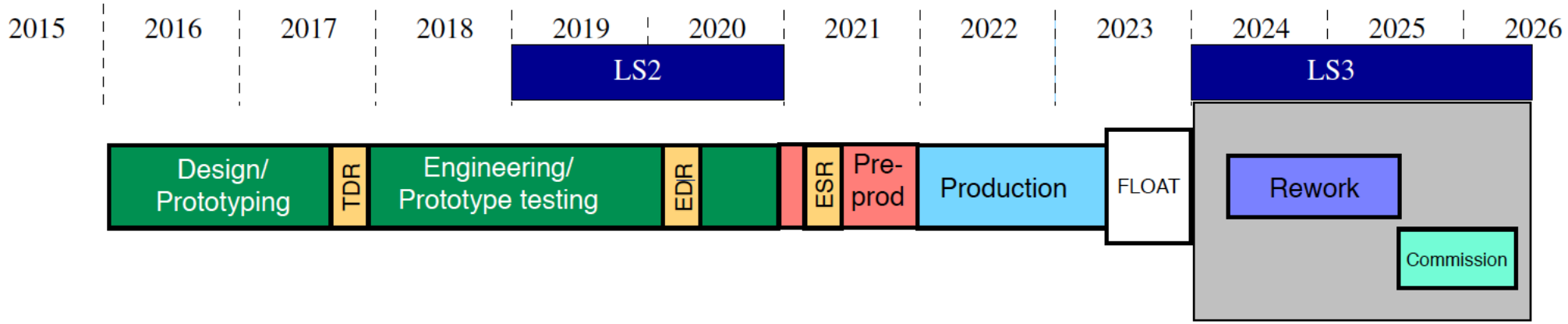
Single ATCA board replaces four boards in legacy system to perform data and trigger Concentration, clock and control (See poster from Stephen Goadhouse)

Clock Distribution



Precision timing requires precision clock distribution. Baseline is to transmit endcoded clock to front-end via lpGBT but ongoing R&D program underway to understand clock stability throughout the chain

CMS ECAL Upgrade Schedule and Status



Recently completed TDR for LHCC review

Demonstrators tested for VFE, SLVR, FE boards

On and off detector architecture specified

Summary and Conclusion

The upgrade of the CMS ECAL Barrel is central to the HL-LHC physics program

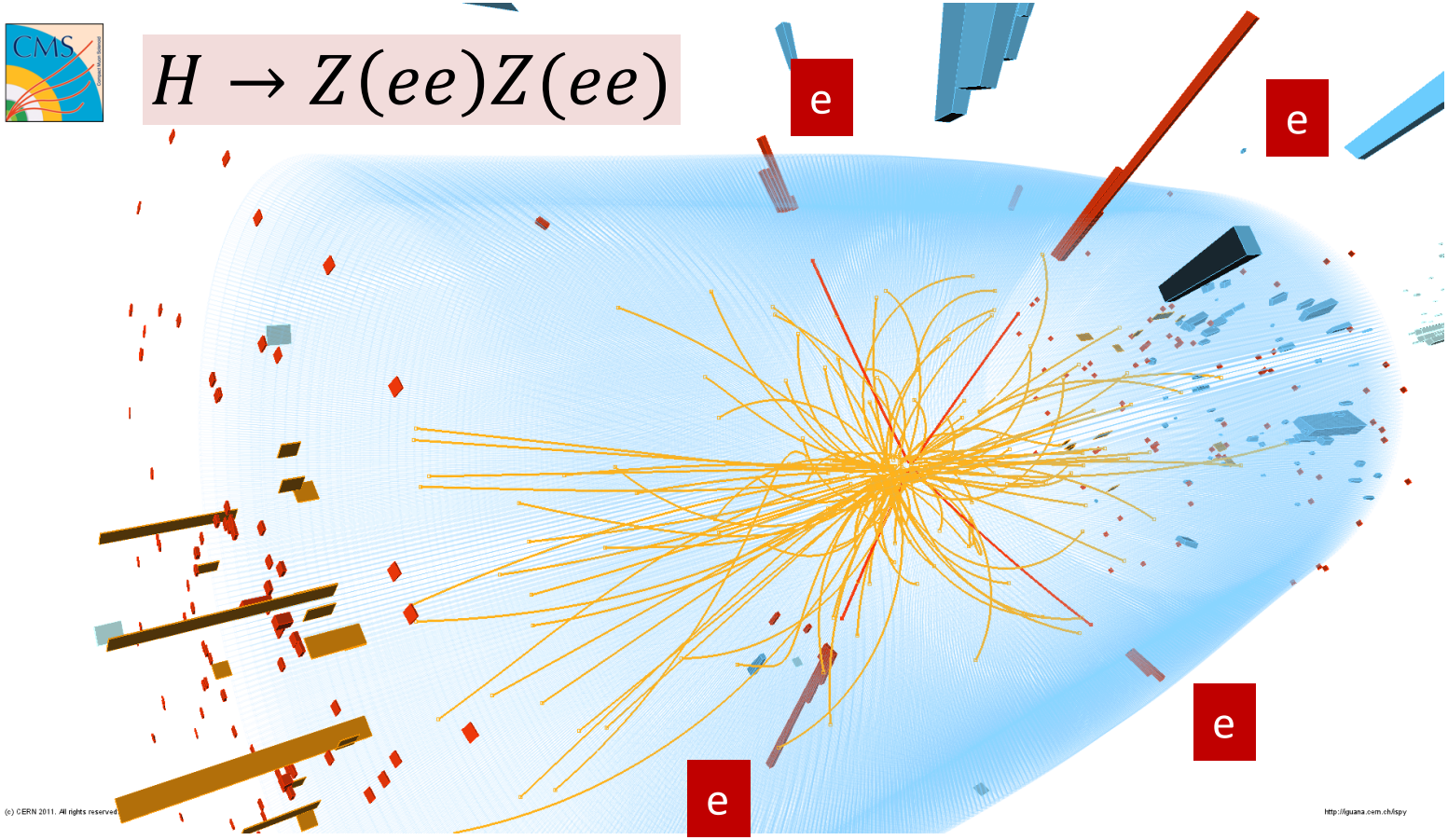
Precision timing a key component to meeting the upgrade specifications

Modern electronics (Custom rad hard ASICs, high speed optical links, powerful FPGAs make it possible to sustain the LHC performance in HL-LHC conditions

Good progress with demonstrator boards produced for on-detector components and Off detector architecture and board specified

ADDITIONAL MATERIAL

The ECAL HL-LHC Upgrade



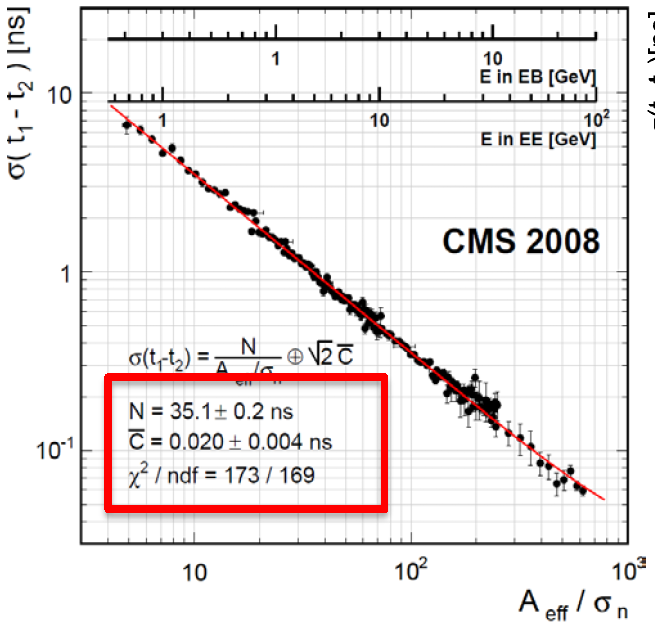
The upgrade will use modern electronics to enhance the performance and discovery capabilities of the barrel electromagnetic/hadronic calorimeter, particularly for Higgs Bosons

Present Timing in ECAL

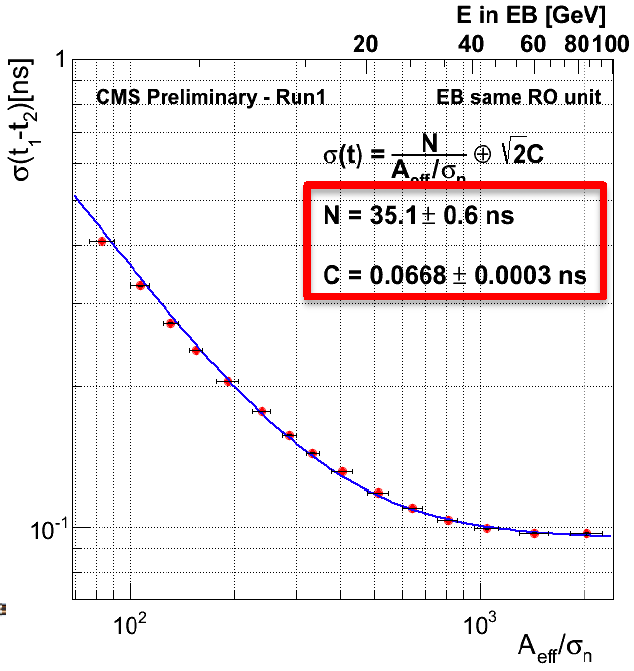
Results from test beams and pp collision data at LHC :

- **Electron showers from Z→ee decay Δt_{TOF} : ~270 ps, single channel : ~190 ps, without path length correction : ~380 ps**
- **Constant term of resolution : ~20 ps in test beam, ~70 ps in situ (same clock).**
- **Studies on jet timing vertex resolution suggest very promising performance.**

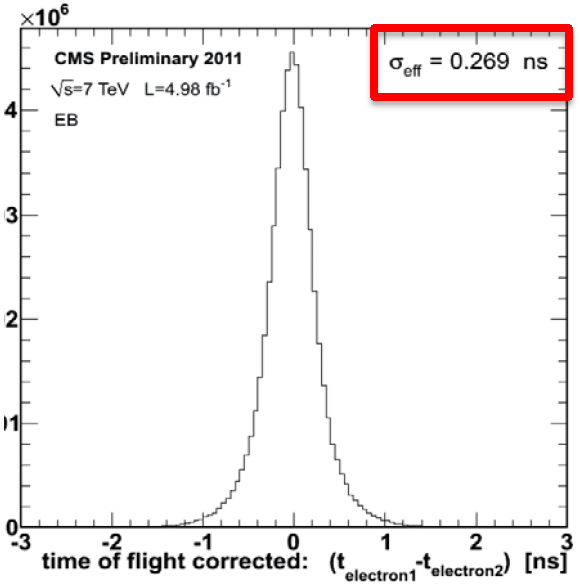
Test Beam



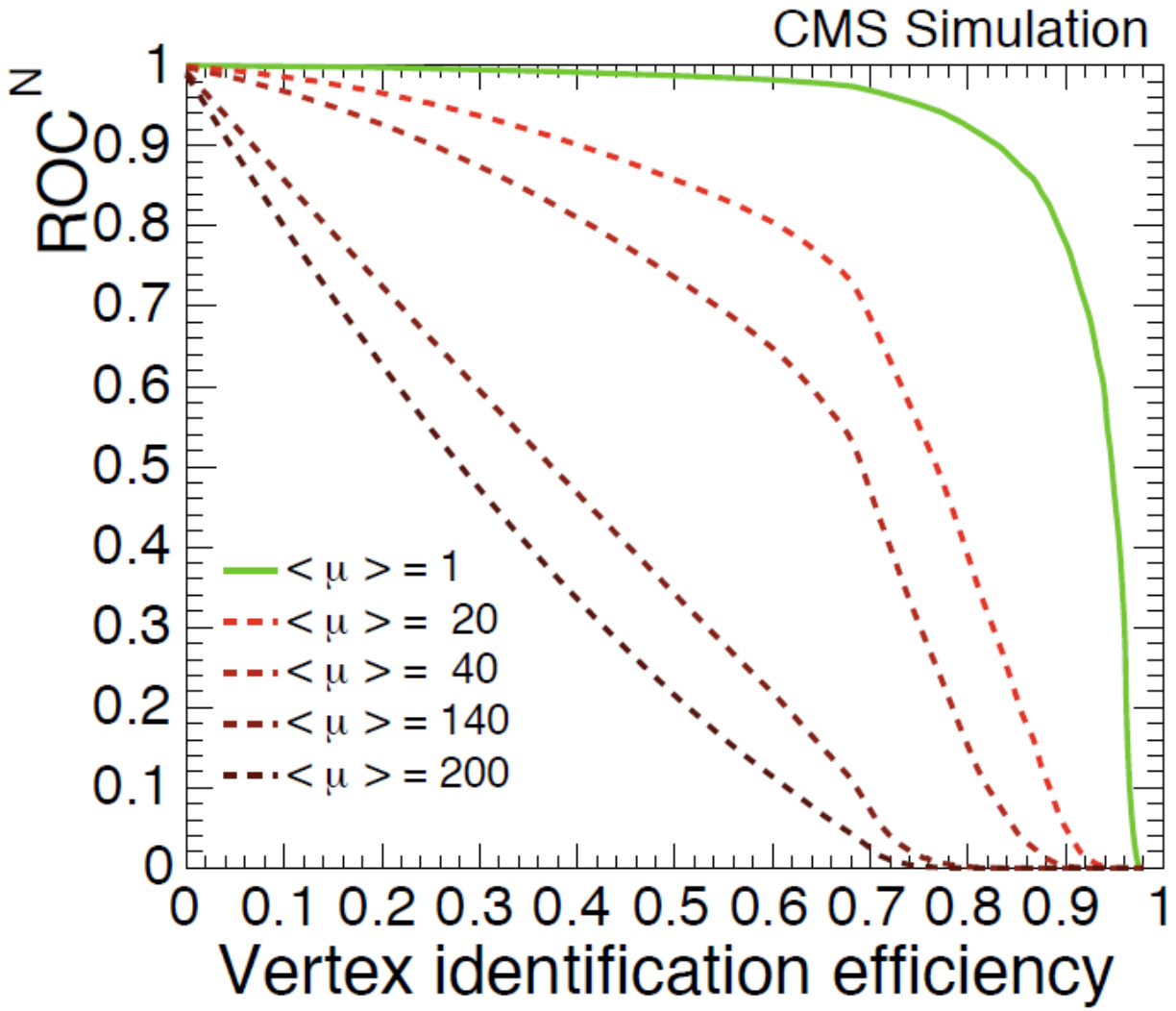
In-situ, cluster



In-situ, Z→ee

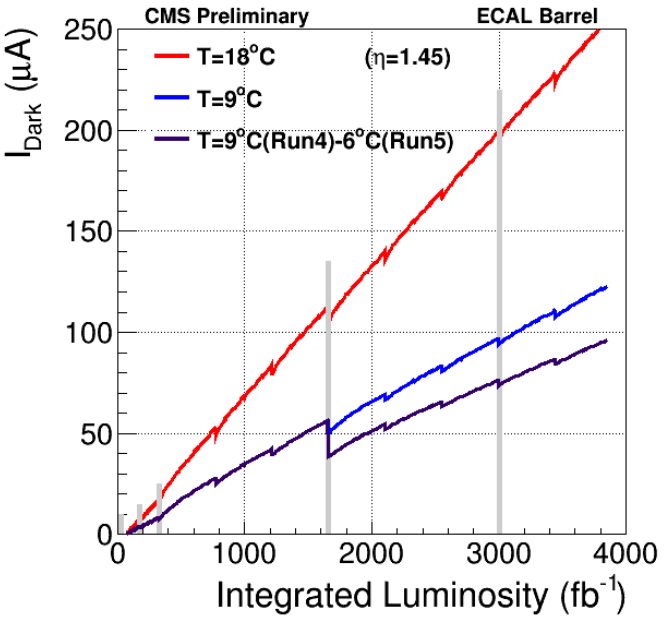


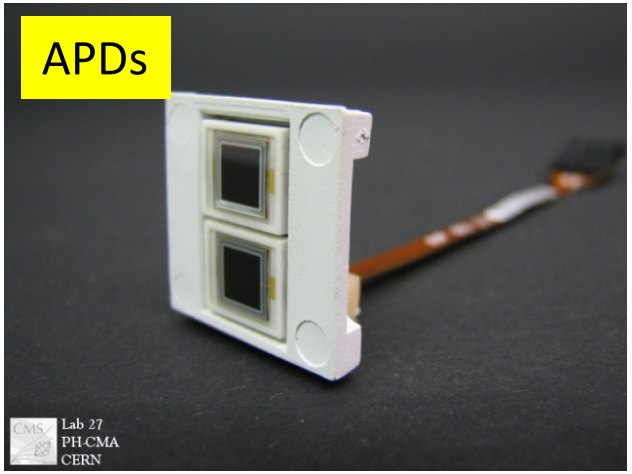
H→γγ Vertex Efficiency vs Pileup



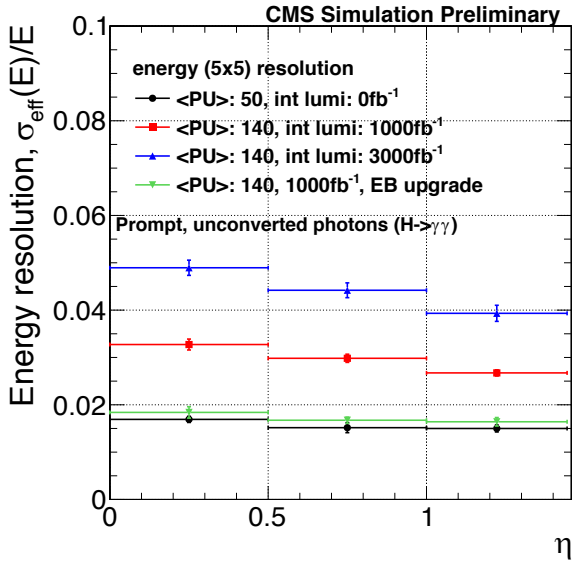
ECAL Photodetectors

- Crystals and the Avalanche Photodetectors will not be replaced (Crystals > 50% original light yield to 3000 fb^{-1})
- No failures in APD irradiation tests @ HL-LHC fluences but neutron damage increases dark current
- Cooling from 18°C to 9°C halves the dark current. 6°C being considered for Run 5.



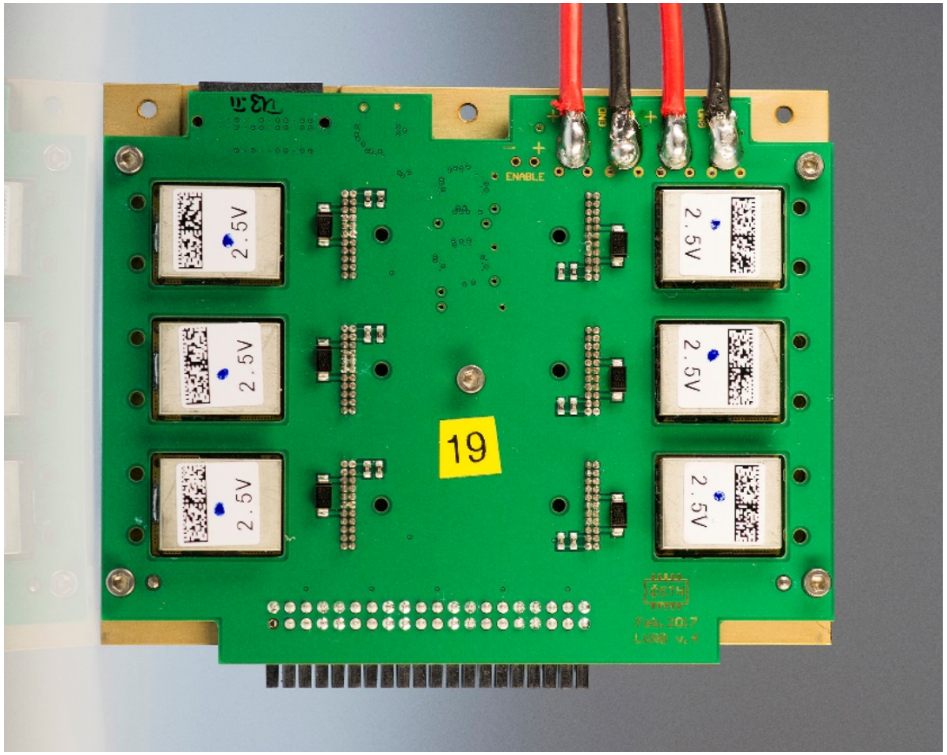


Cooling + shorter pre-amp shaping recovers resolution performance



Switching Low Voltage Regulator Board

Prototype SLVR Board



Electronics noise a limiting factor in calorimeter Resolution perfromance at low energy

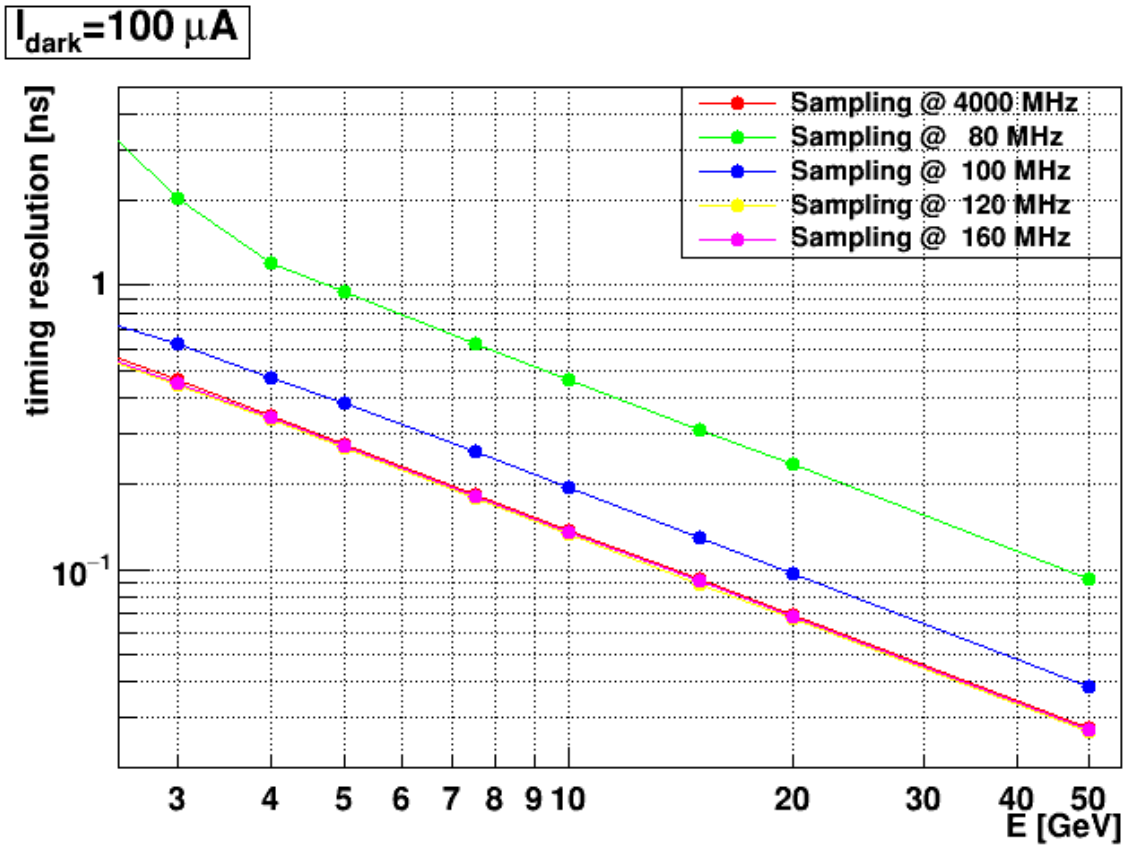
Uses CERN 's FEASTMP_CLP DC-DC switching converters to stepdown from 10V to 2.5V or 1.2V (legacy linear supplies)

Current draw per trigger tower (5VFEs + FE) reduced from 13.6A to 4A due to high efficiency (85%) of DC-DC converters

2448 SLVR boards required

The use of high efficiency DC-DC switching converters gives same noise performance as The legacy system but with much less copper cabling and commensurate power losses

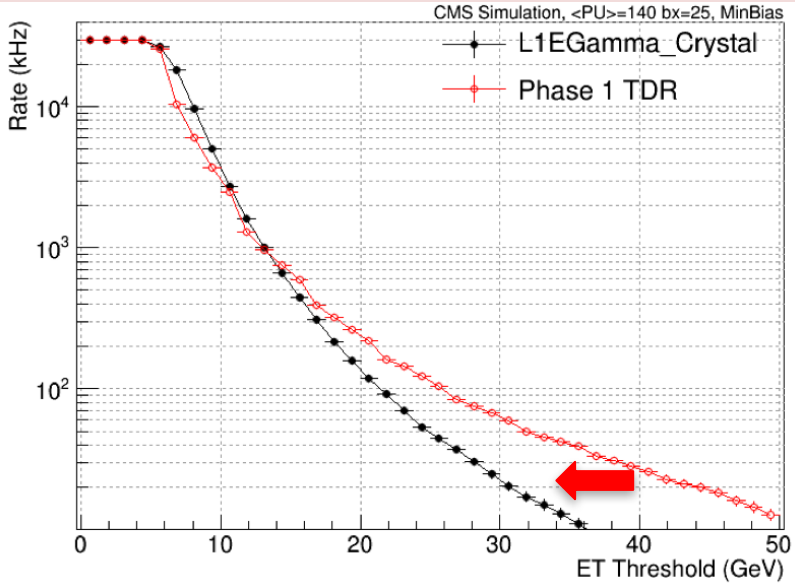
Sampling Frequency vs σ(t)



Effect of the sampling frequency on the timing resolution using the TIA architecture with 100 μA leakage current in the APD. Curves for 120, 160 and 4000 MHz are superimposed.

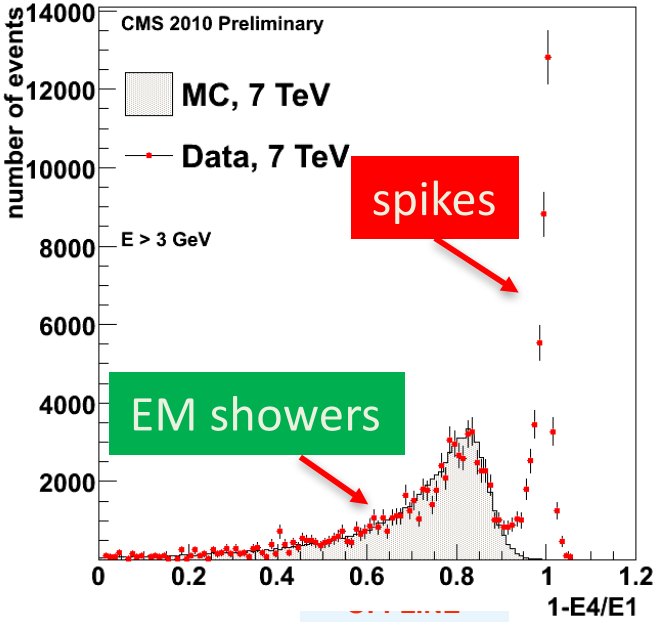
Benefits of Single Crystal Trigger Primitive

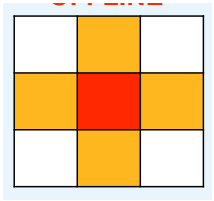
Trigger rate with w/wo single crystal data



Single crystal allows greater background suppression allowing lower Et thresholds

Isolation to suppress spikes further
Implemented online (vs offline in legacy system)





High bandwidth allows single crystal trigger primitive which match to tracks
In the new track trigger and better isolation for additional spike suppression