NumEriseur à Bande Large pour l'Astronomie

Wide band digitizer for radioastronomy

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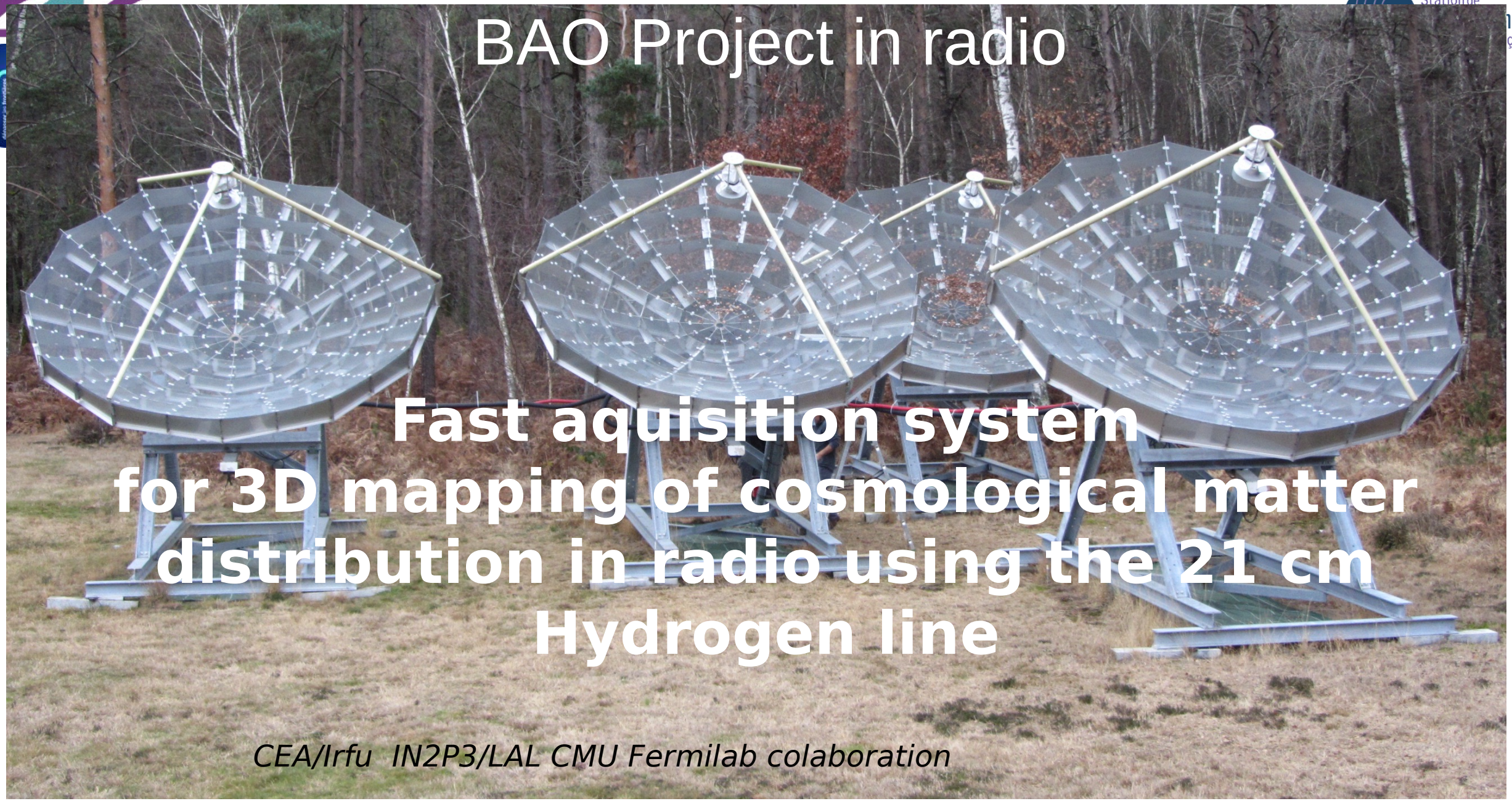
18330 Nançay, France

TWEPP 2017

Agenda

- The PAON IV prototype
- NEBuLA hardware description
- NEBuLA II

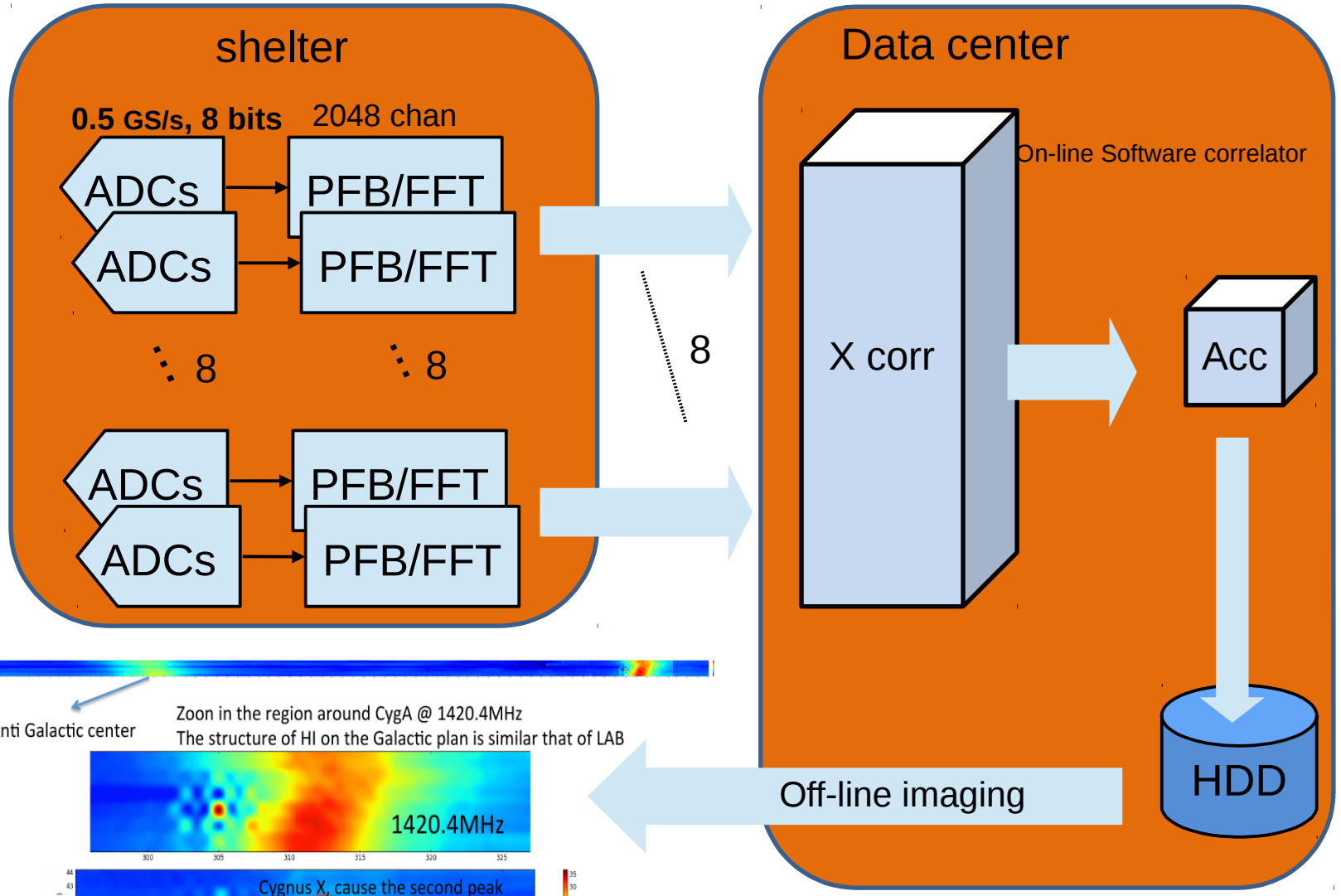
BAO Project in radio

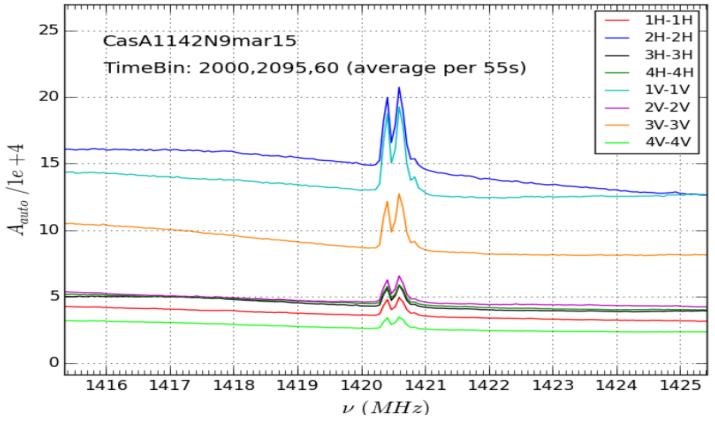


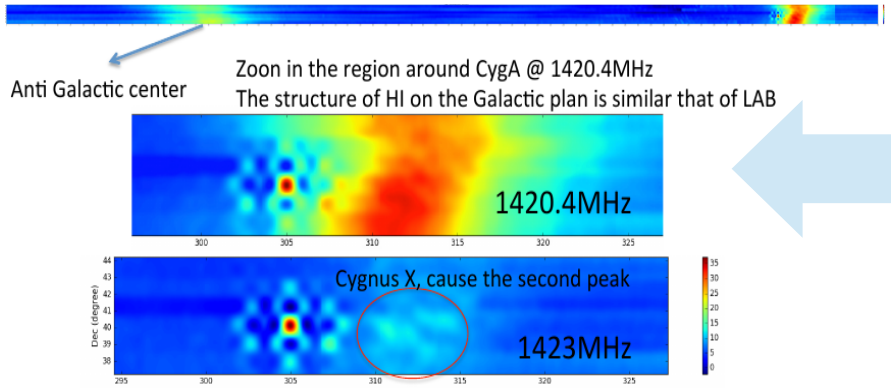
Fast aquisition system for 3D mapping of cosmological matter distribution in radio using the 21 cm Hydrogen line

CEA/Irfu IN2P3/LAL CMU Fermilab colaboration

Data processing for off-line beam forming

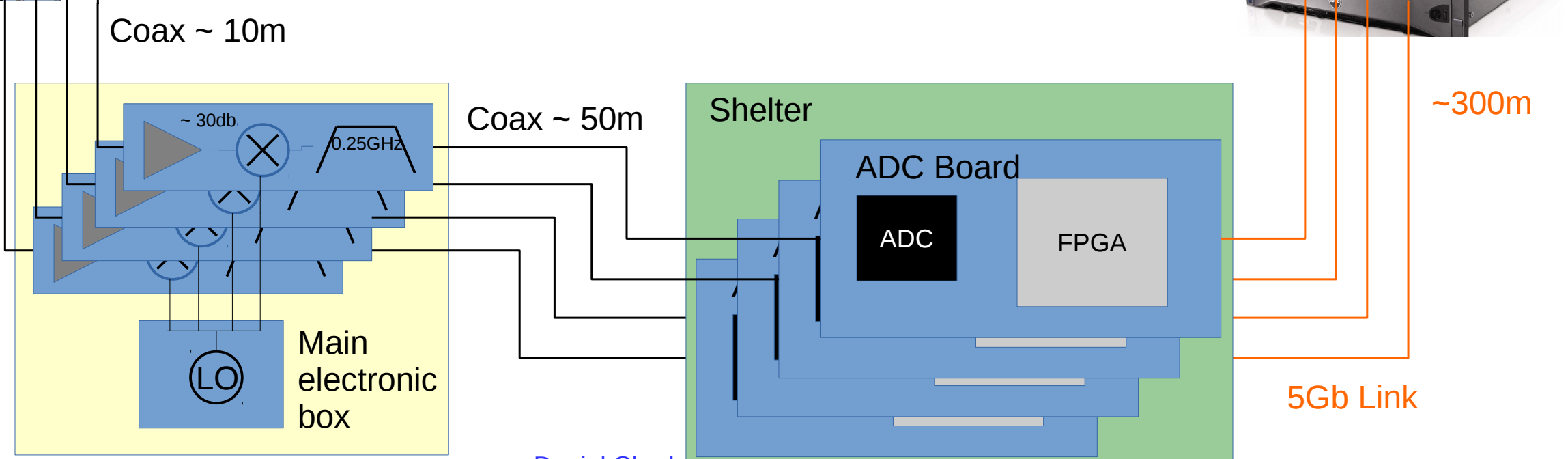






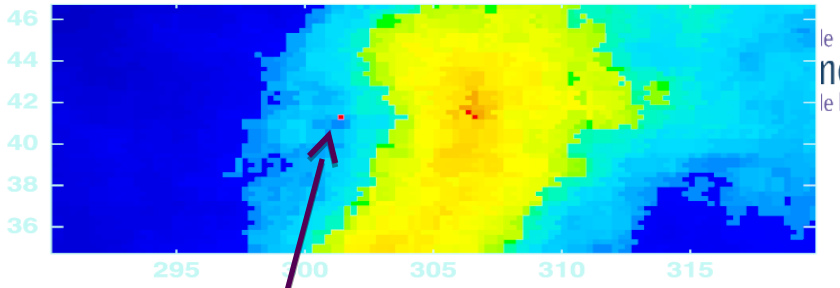
Paon IV acquisition chain

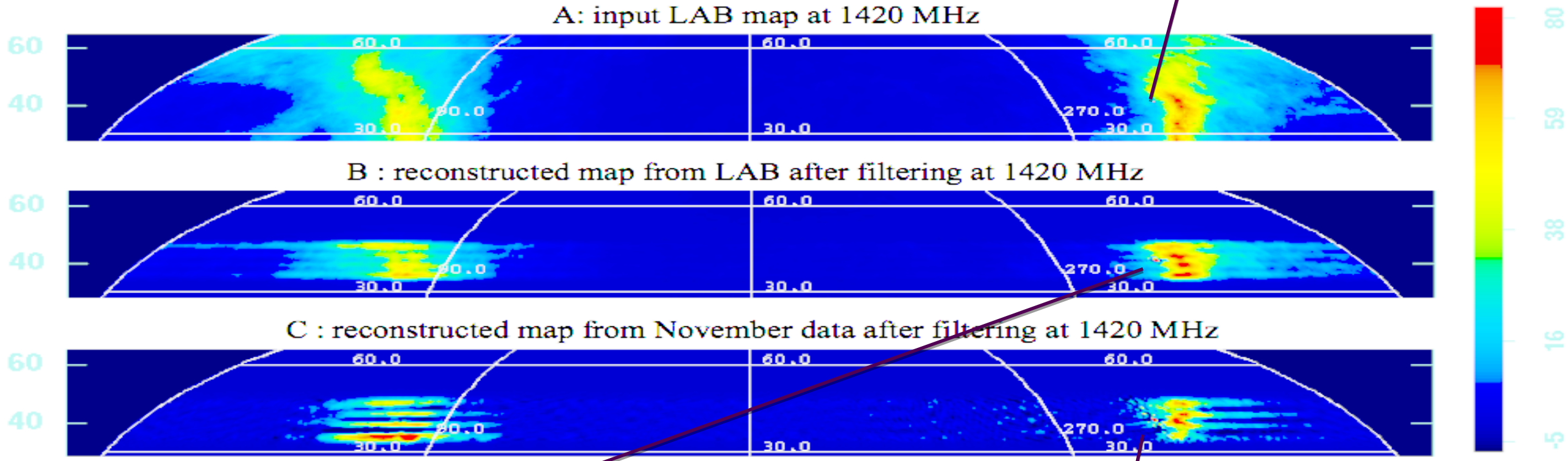
- Long HF coaxial ~ 5m.
- Long coaxial RF cable ~ 50m
- Down converter & Local oscillator not thermostatically controled
- Shelter mandatory for ADC board and the contol system
- Not easily scalable
- Dedicated protocol for data transfer



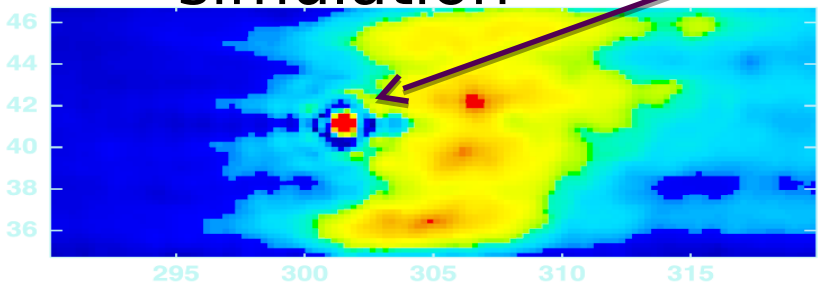
PAON IV data analysis (1)

Reconstructed map at 1420.4 MHz
from PAON-4 Nov.2016 observations

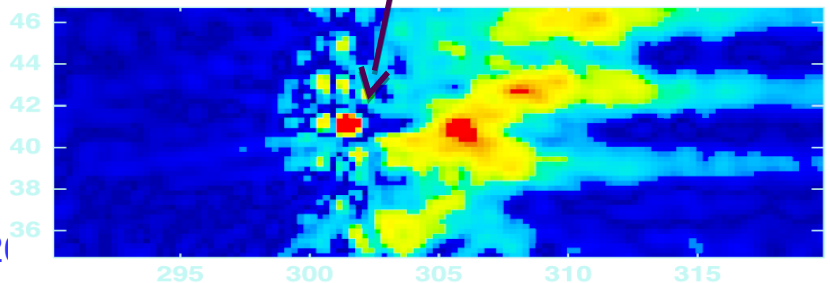




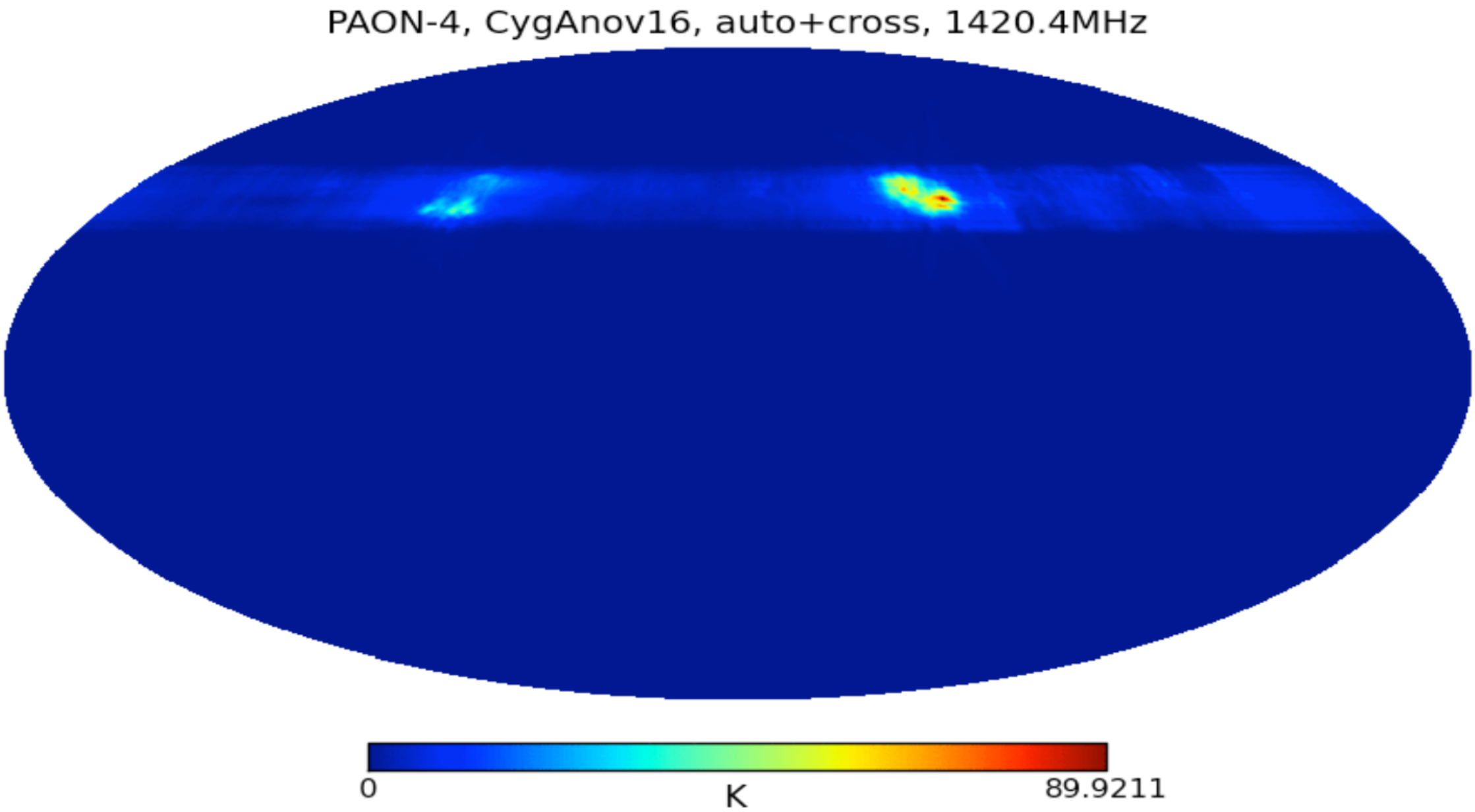
simulation



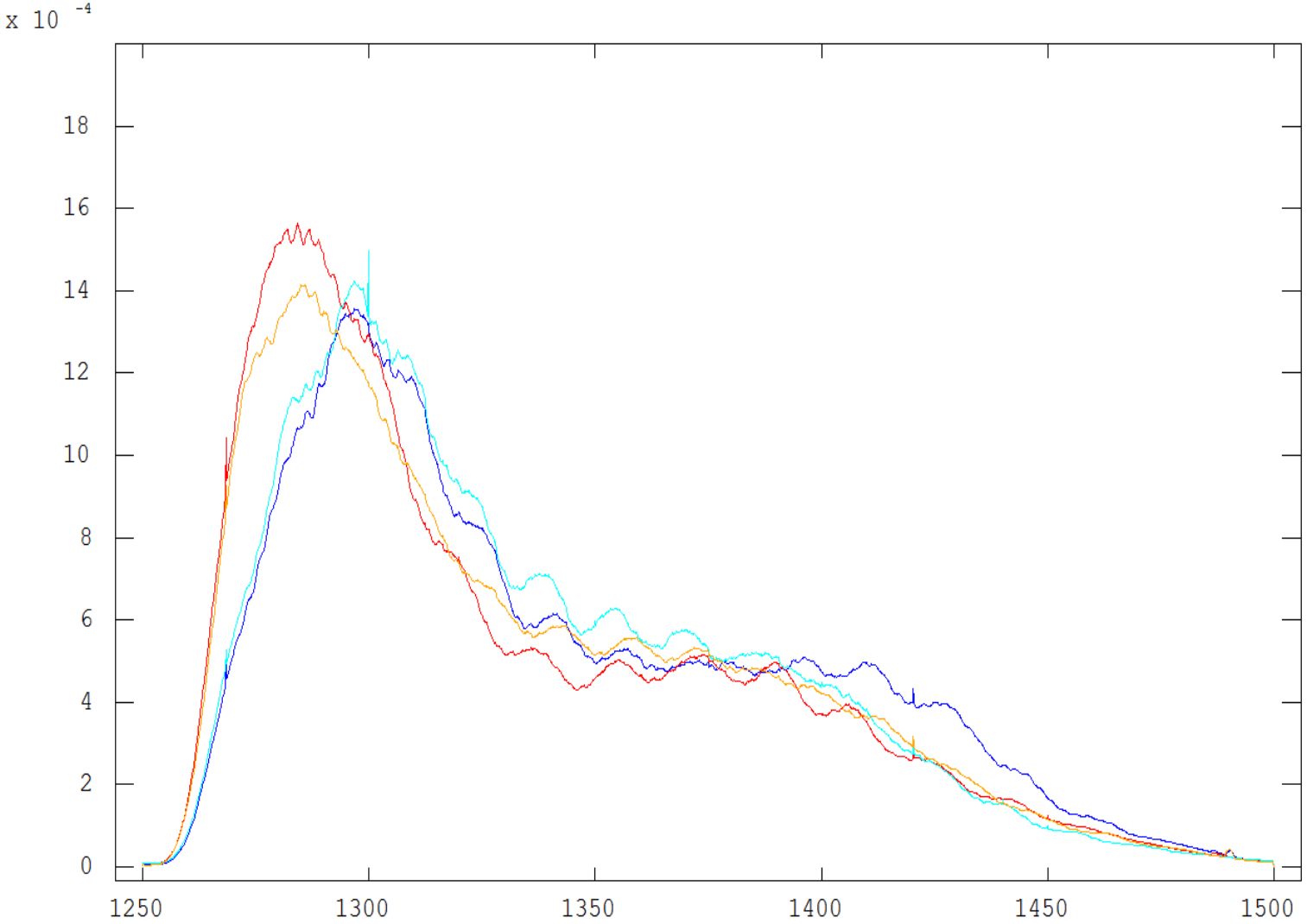
PAON-4 data



PAON IV data analysis (2)



Current analog limitations

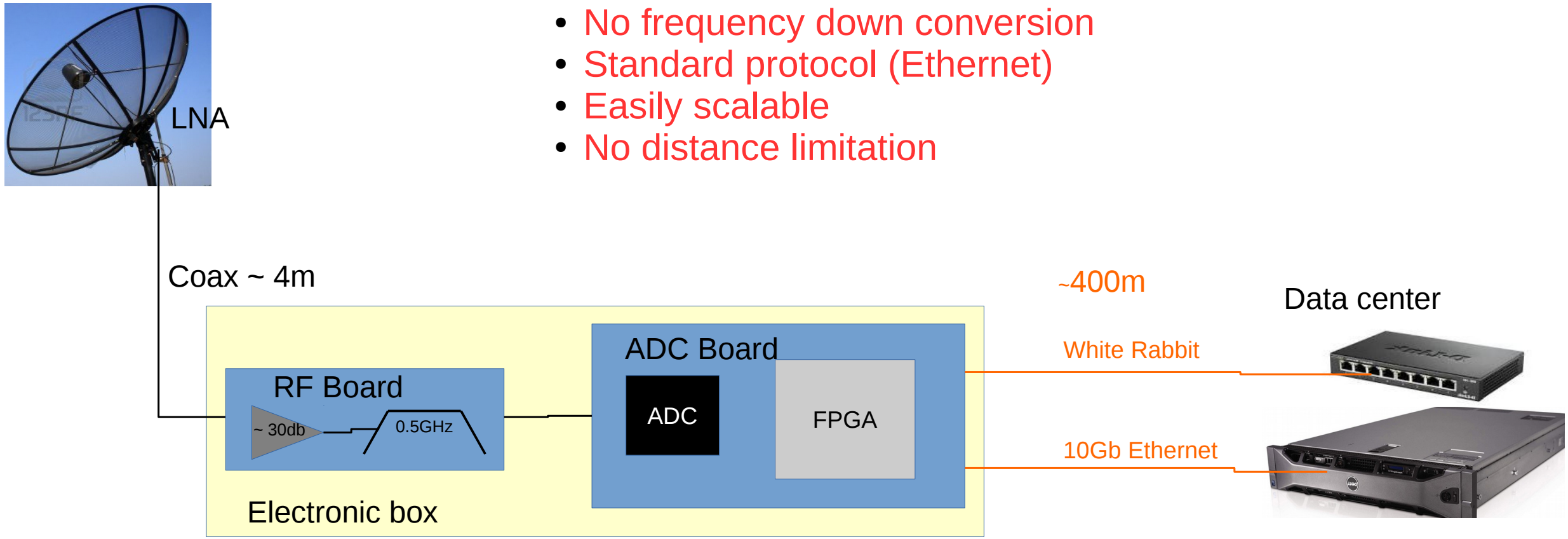


SWR depends on:

- long RF cables,
- adaptation mismatch,
- wide band acquisition
- frequency shifting
- technical constraints for packaging and array design / construction (LO distribution mechanical/thermal/electromagnetic shielding ...).

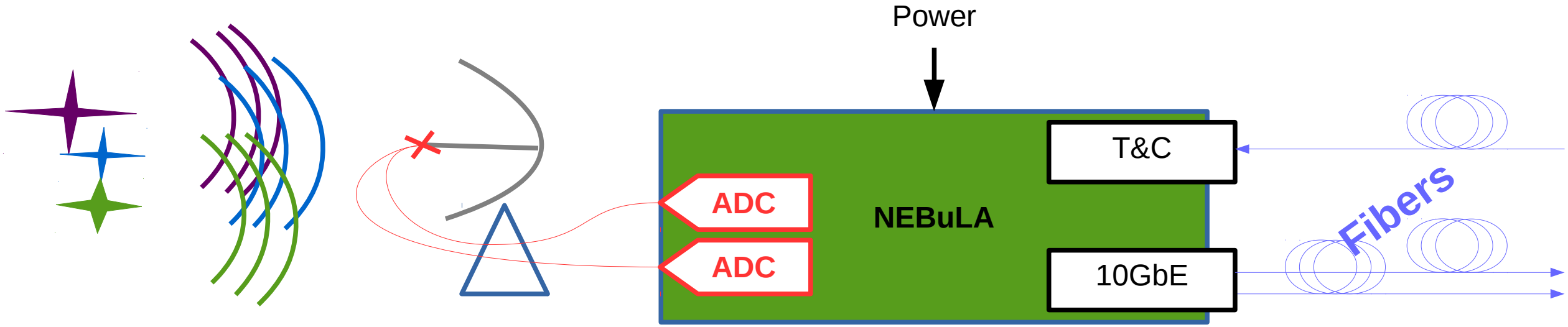
New PAON IV system

- Short HF coaxial < 5m.
- Clock distribution over fiber
- No frequency down conversion
- Standard protocol (Ethernet)
- Easily scalable
- No distance limitation

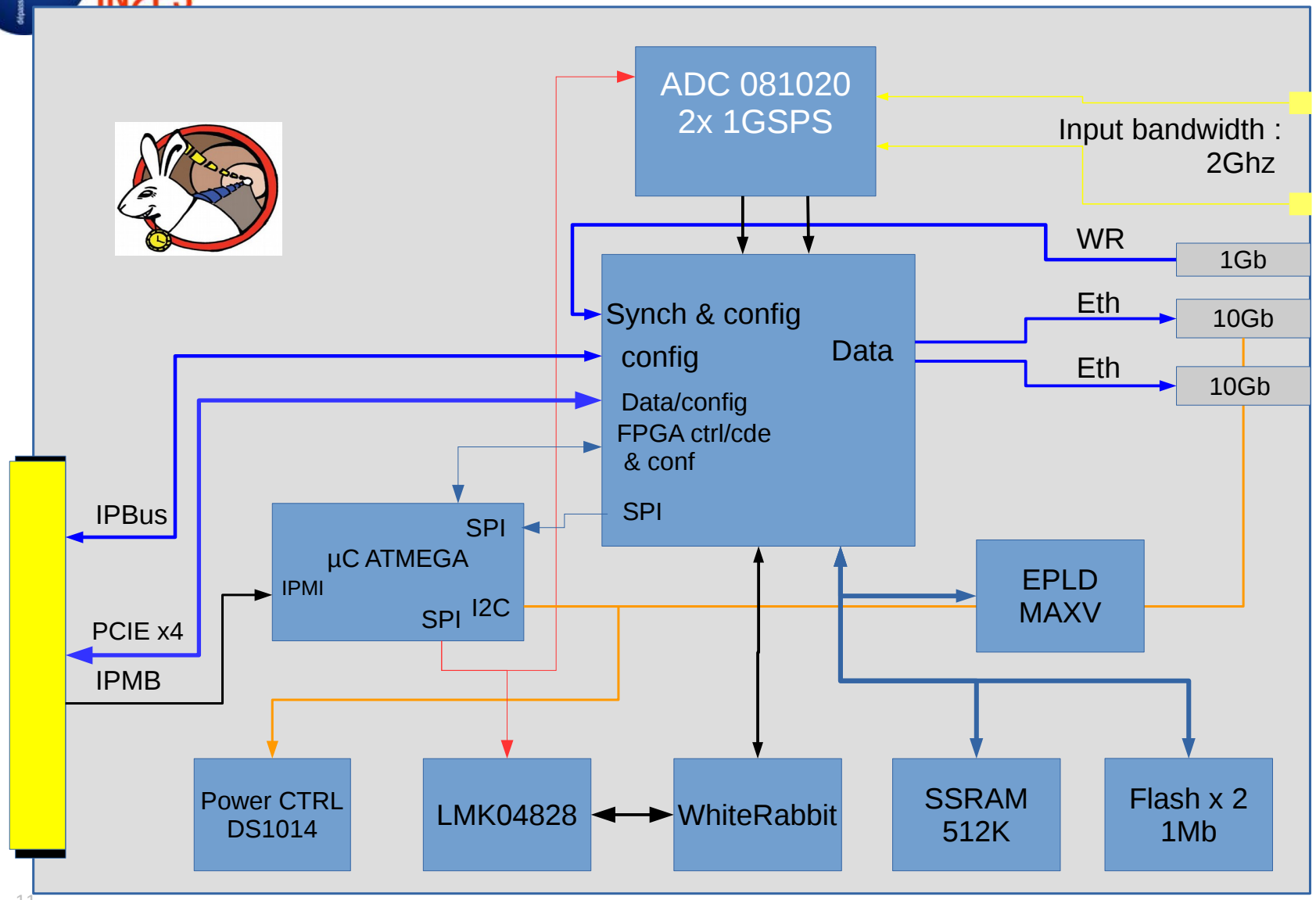


NumEriseur à Bande Large pour l'Astronomie

Wide band digitizer for radioastronomy



NEBULA board

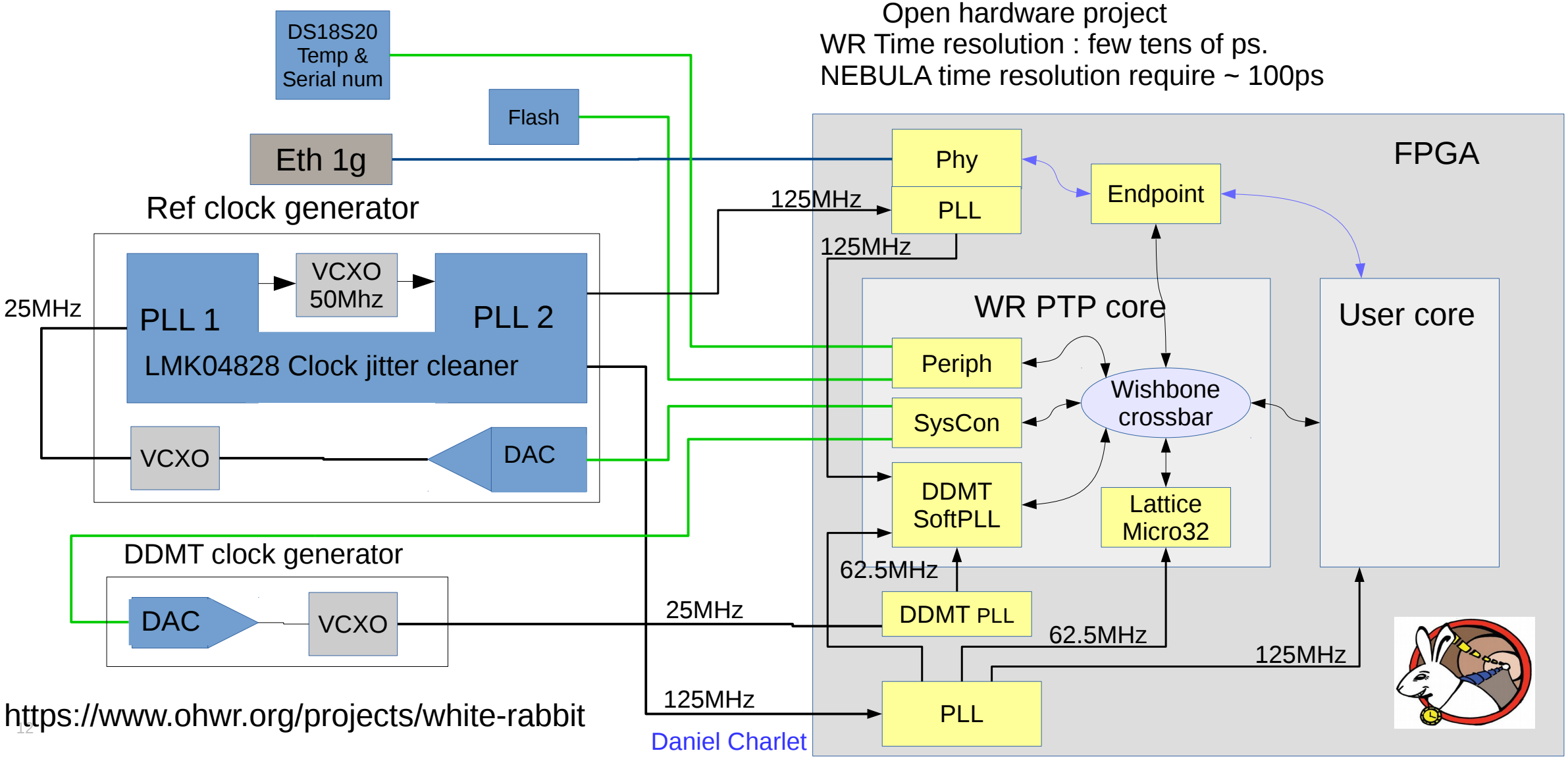


- MTCA 4.0 standard, Double-width, full size AMC
- FPGA : 5AGTMC7G3F31
- ADC 2 channel 1GSPS
- White Rabbit compliant.
- Front panel : WR SFP+
- 2x SFP+ 10GbEth
- Backplane connectivity :Gbe IP bus, PCI 4x Gen3, IPMB, CLK & trigger lane
- SSRAM 512k
- Stand alone mode (power)
- On board configuration (µC)
- FPGA configuration : passive parallel.
- Very low noise PLL cleaner LM04828

NEBULA WhiteRabbit Implementation

WR : Enhanced PTP protocol & synchronous Eth & DDMT
- Limited additionnal components.
- Based on network standard.
- Open hardware project

WR Time resolution : few tens of ps.
NEBULA time resolution require ~ 100ps

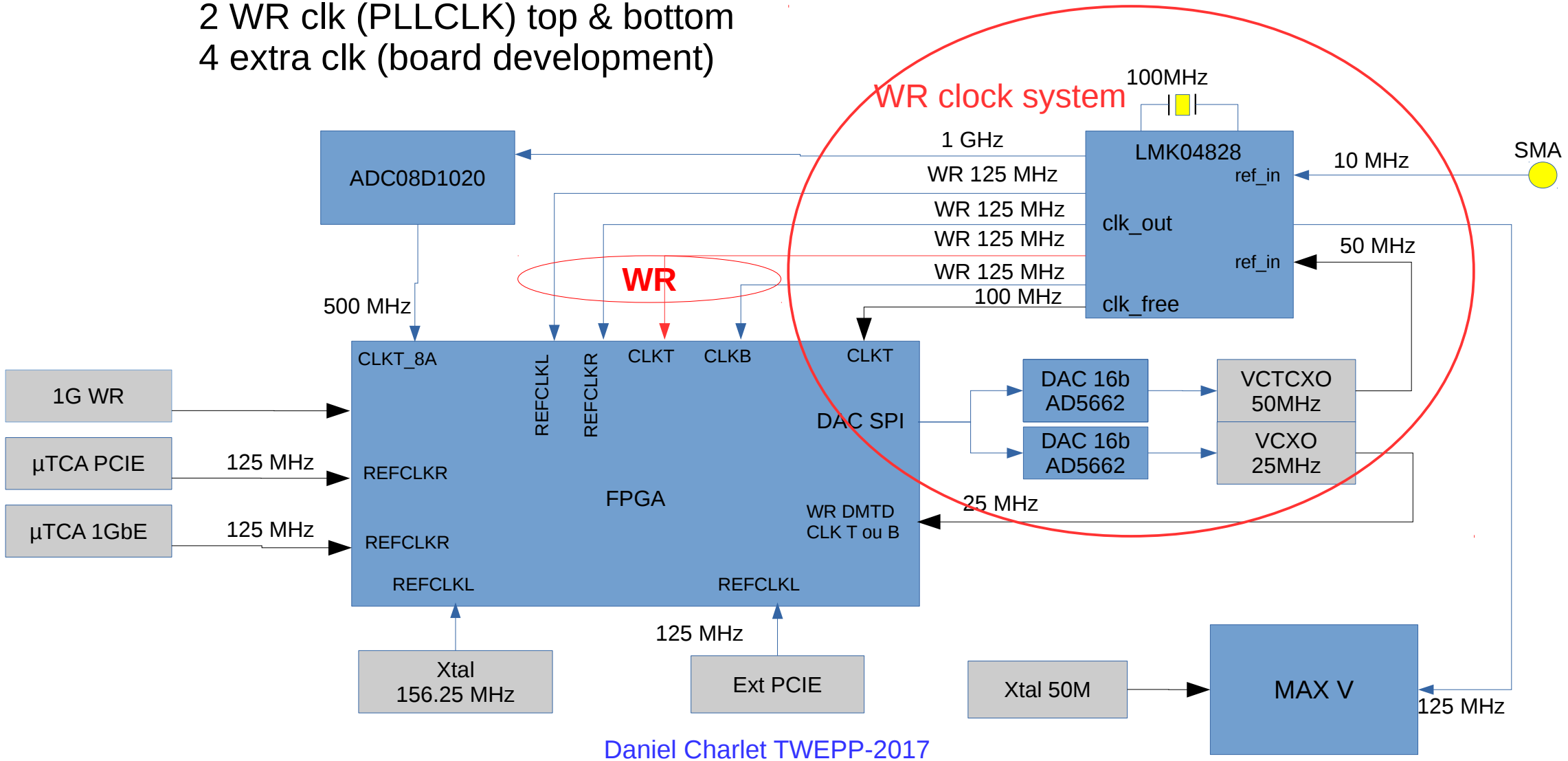


https://www.ohwr.org/projects/white-rabbit

Daniel Charlet

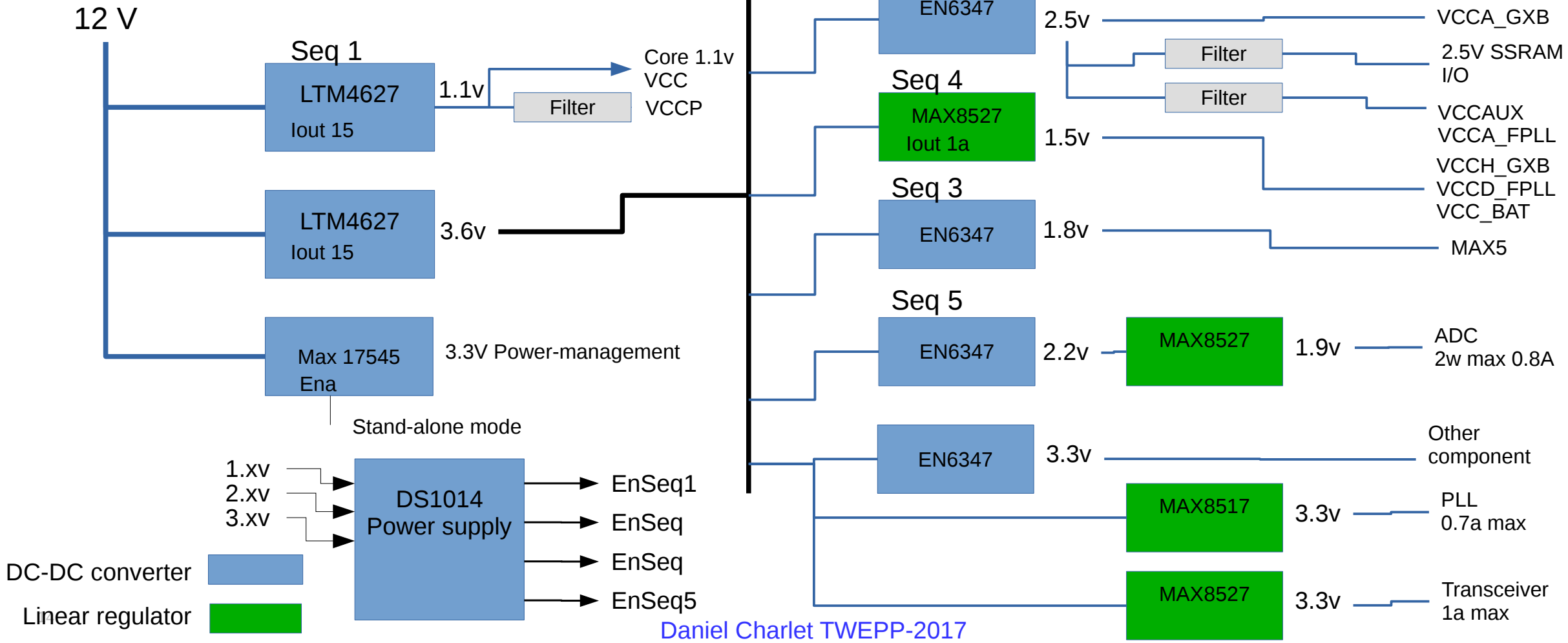
NEBULA clock tree

4 links clk (REFCLK): WR ,1GEth, 10GEth, PCIe
1 ADC clk (PLLCLK).
2 WR clk (PLLCLK) top & bottom
4 extra clk (board development)

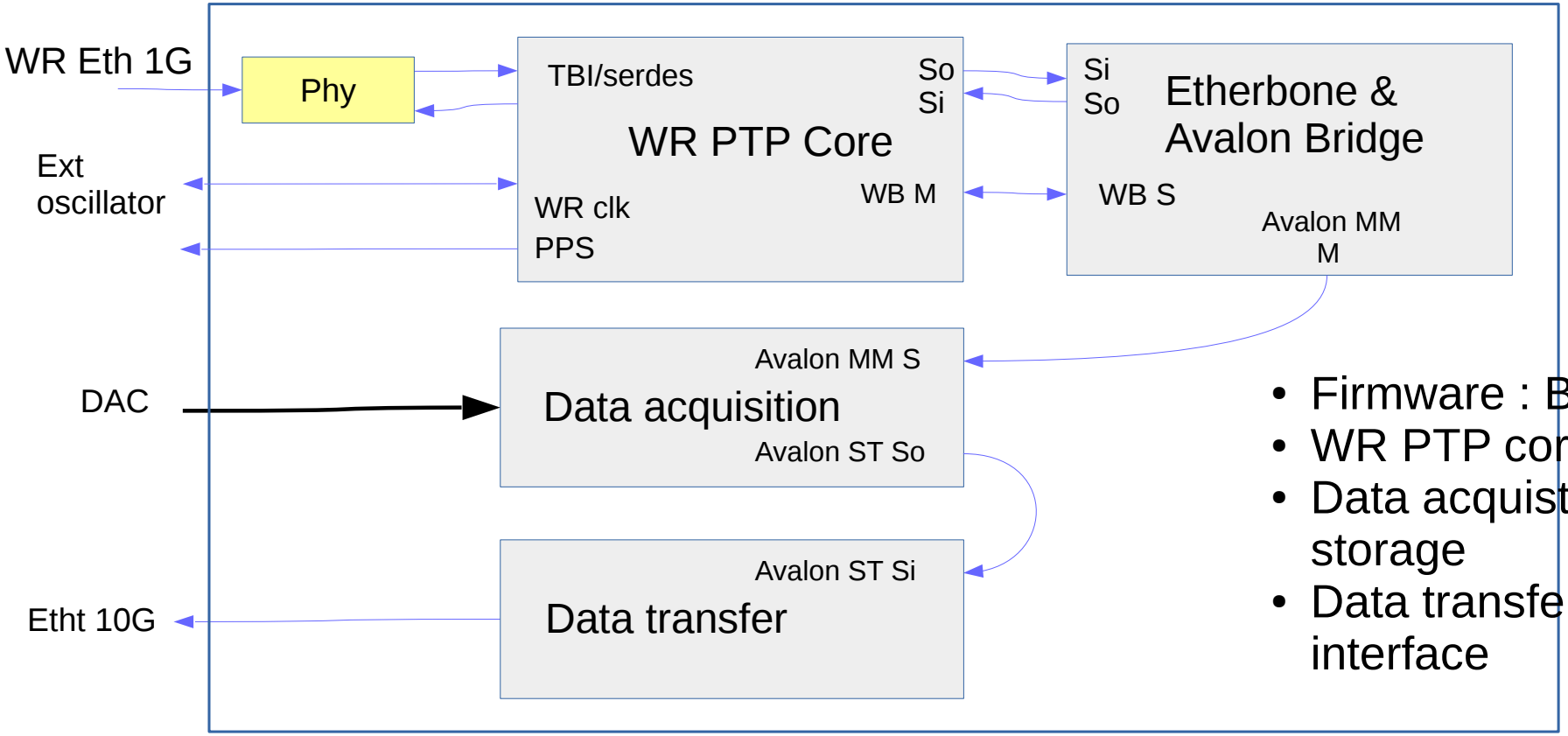


NEBULA Power tree

- Stand-alone mode : DC-DC converter for management power and control (I2C)
- All power Cd & CRTL by DS10104
- 12 V : xTCA crate or on-board connector
- 2 types of regulator : DC-DC or linear



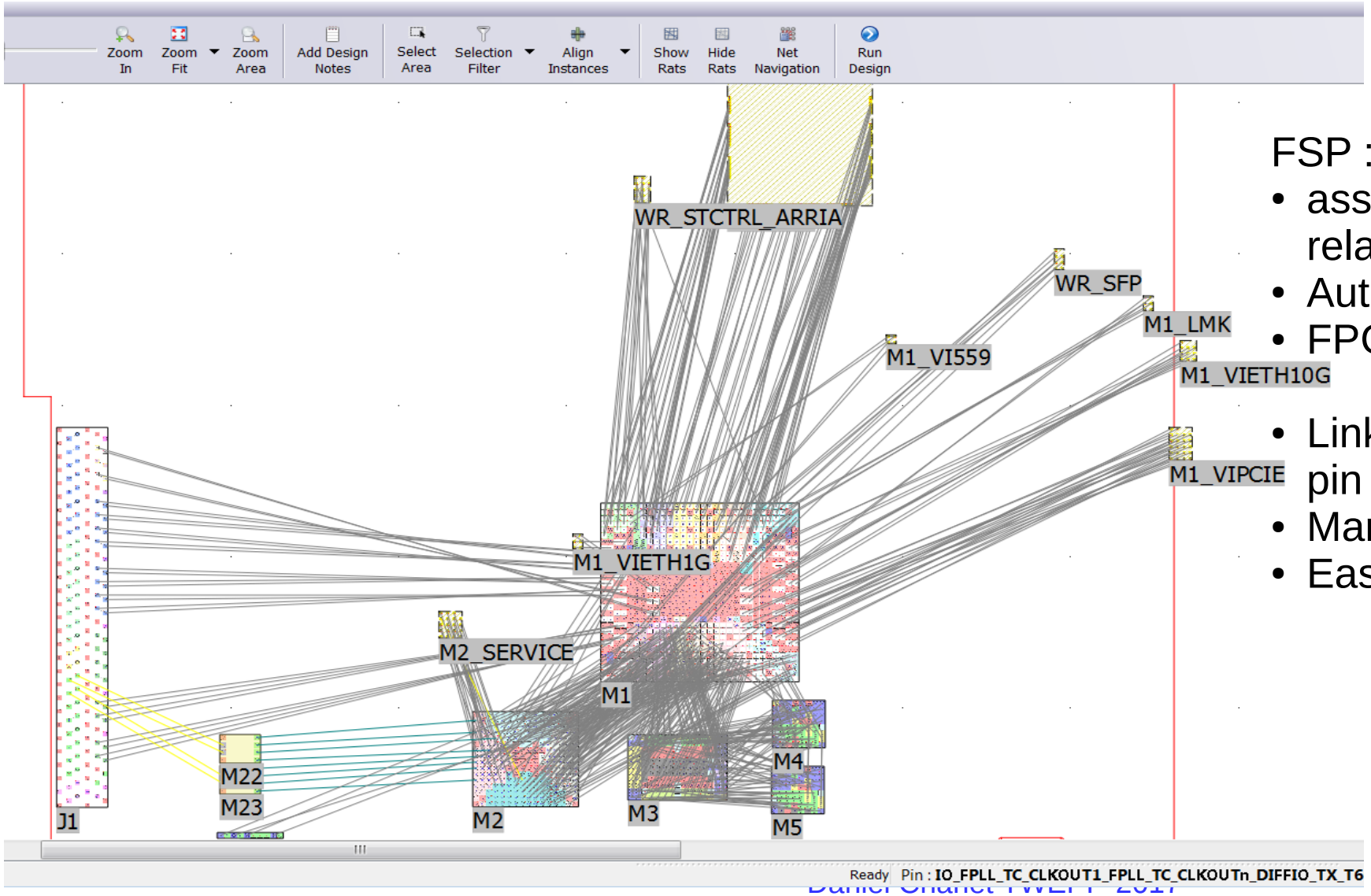
NEBULA FPGA synoptic



- Firmware : Based on GSI project
- WR PTP core : Manage timing
- Data acquistion : ADC interface, data storage
- Data transfer : Data framing, Eth10G interface

http://www.ohwr.org/projects/white-rabbit/wiki/WRReferenceDesign
https://github.com/GSI-CS-CO/bel_projects

FPGA routing optimisation FpgaSystemPlanner

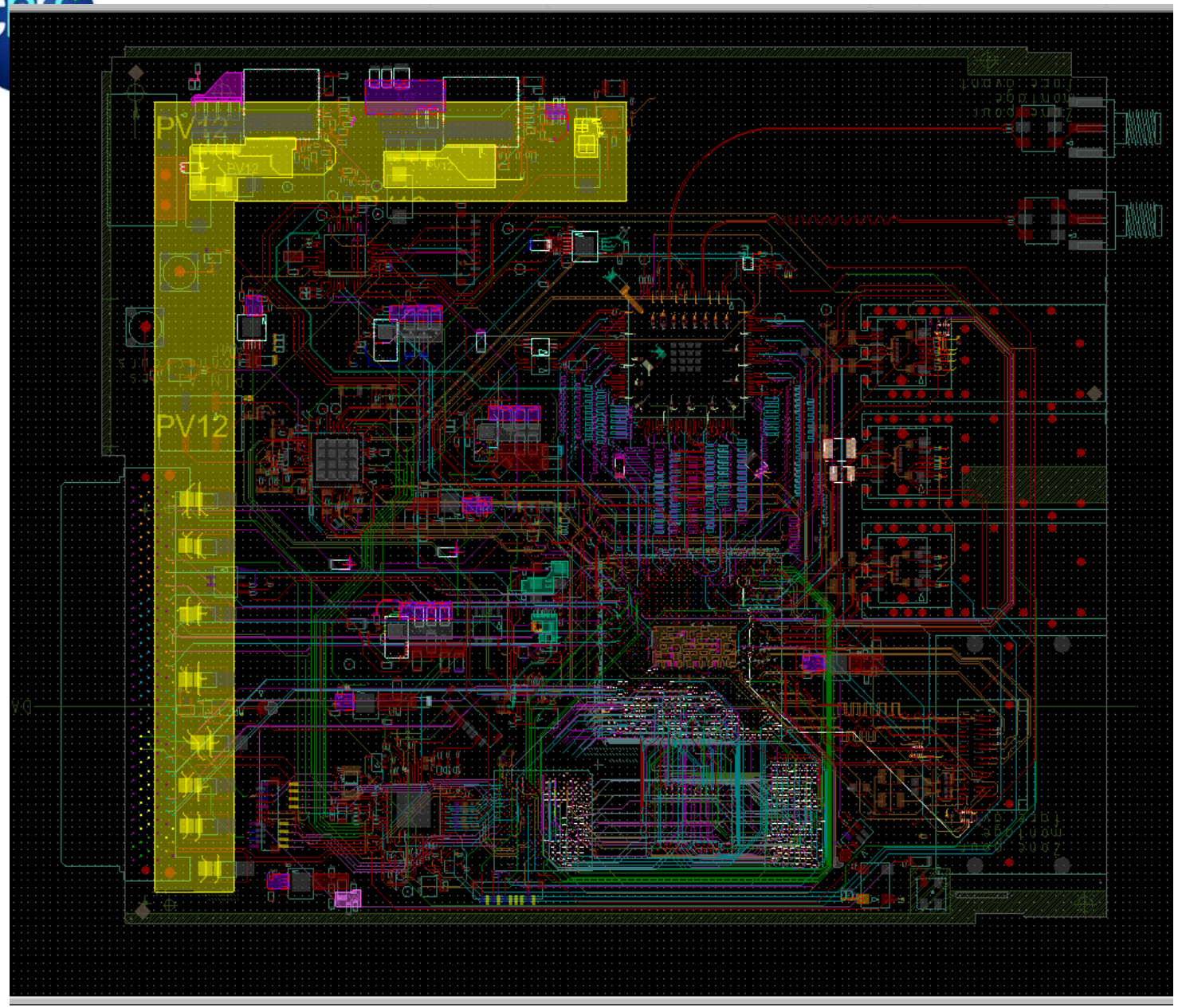


FSP :

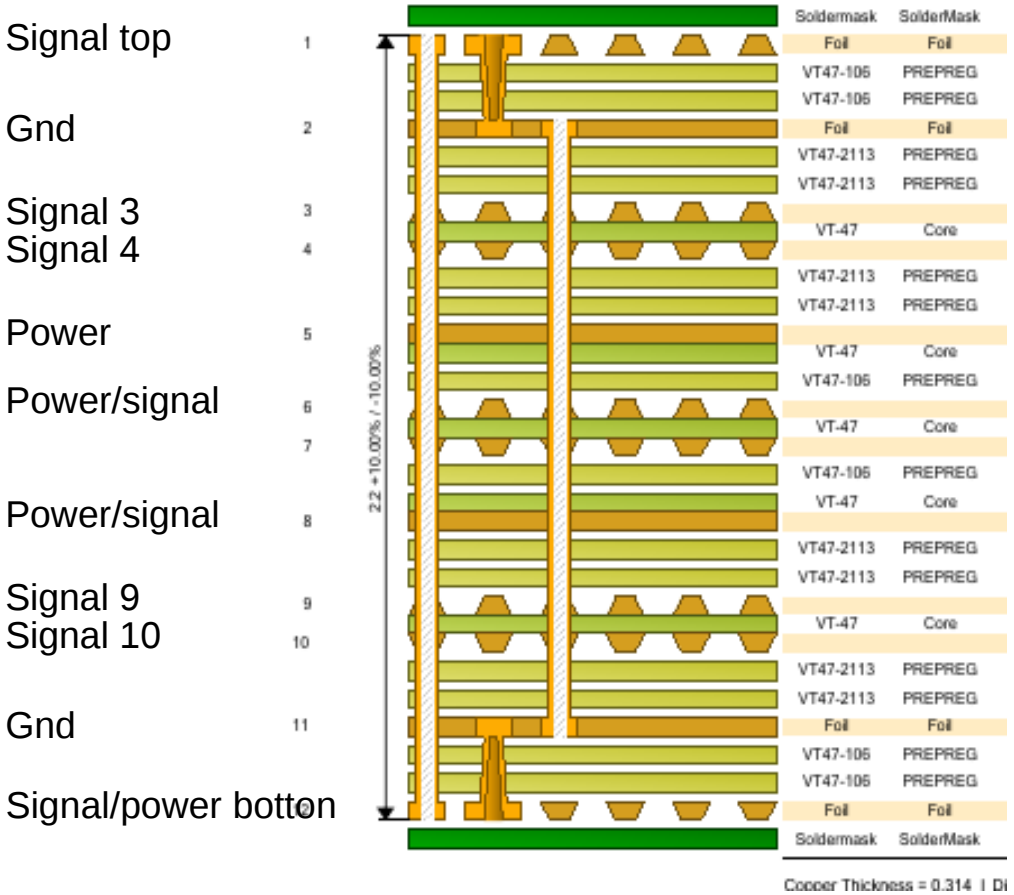
- assign FPGA pins, function of chips relative location.
- Automatic schematic production.
- FPGA pins constraint generation

- Link to allegro routeur : Dynamically pin swap capability.
- Managed decoupling capacitor.
- Easely FPGA change

NEBULA PCB



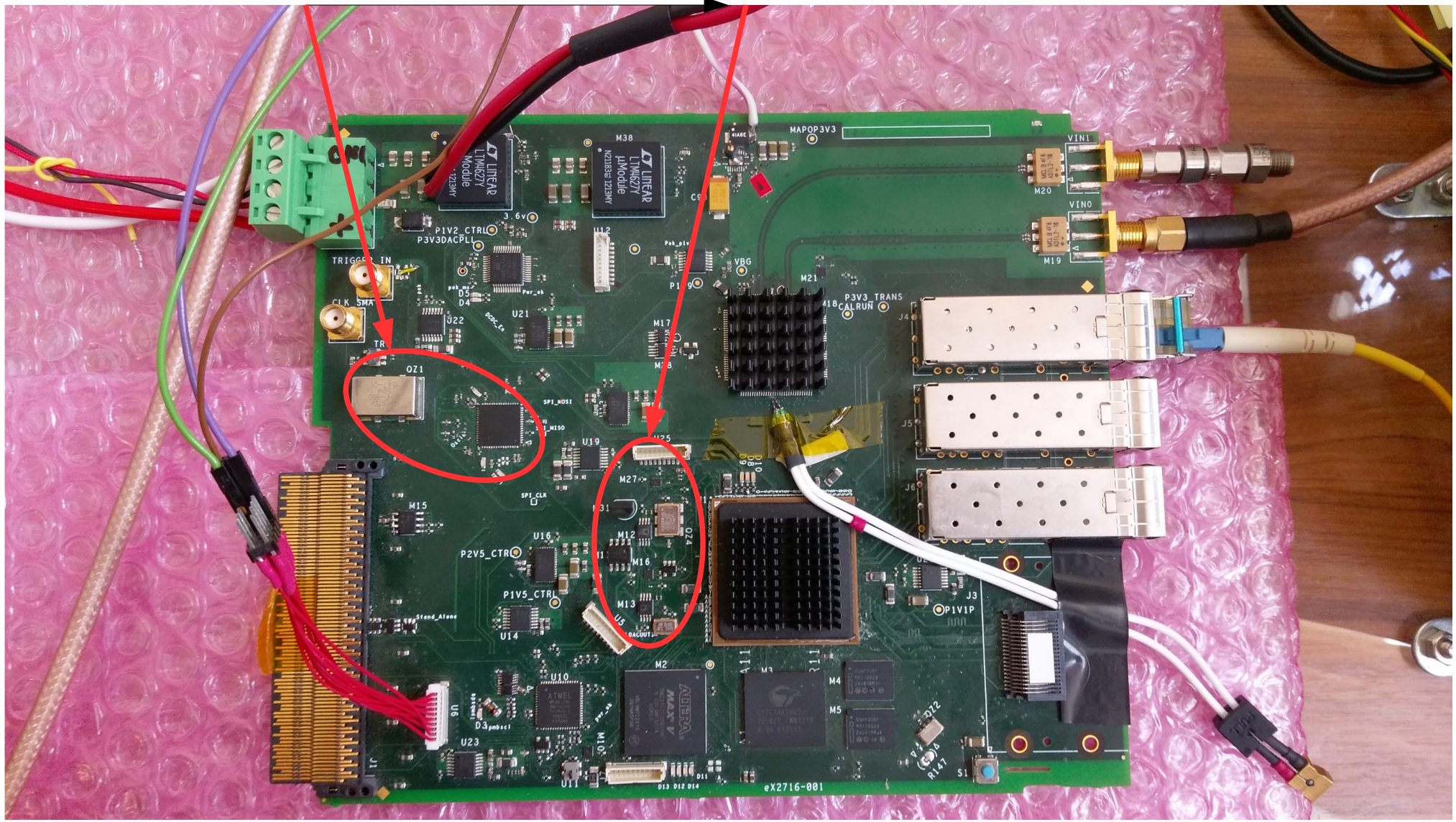
- xTCA for Physics Standard
- 12 layers PCB Design
- Laser via top & bottom
- Impedance controlled
- FR4 VT47 up to 10GHz



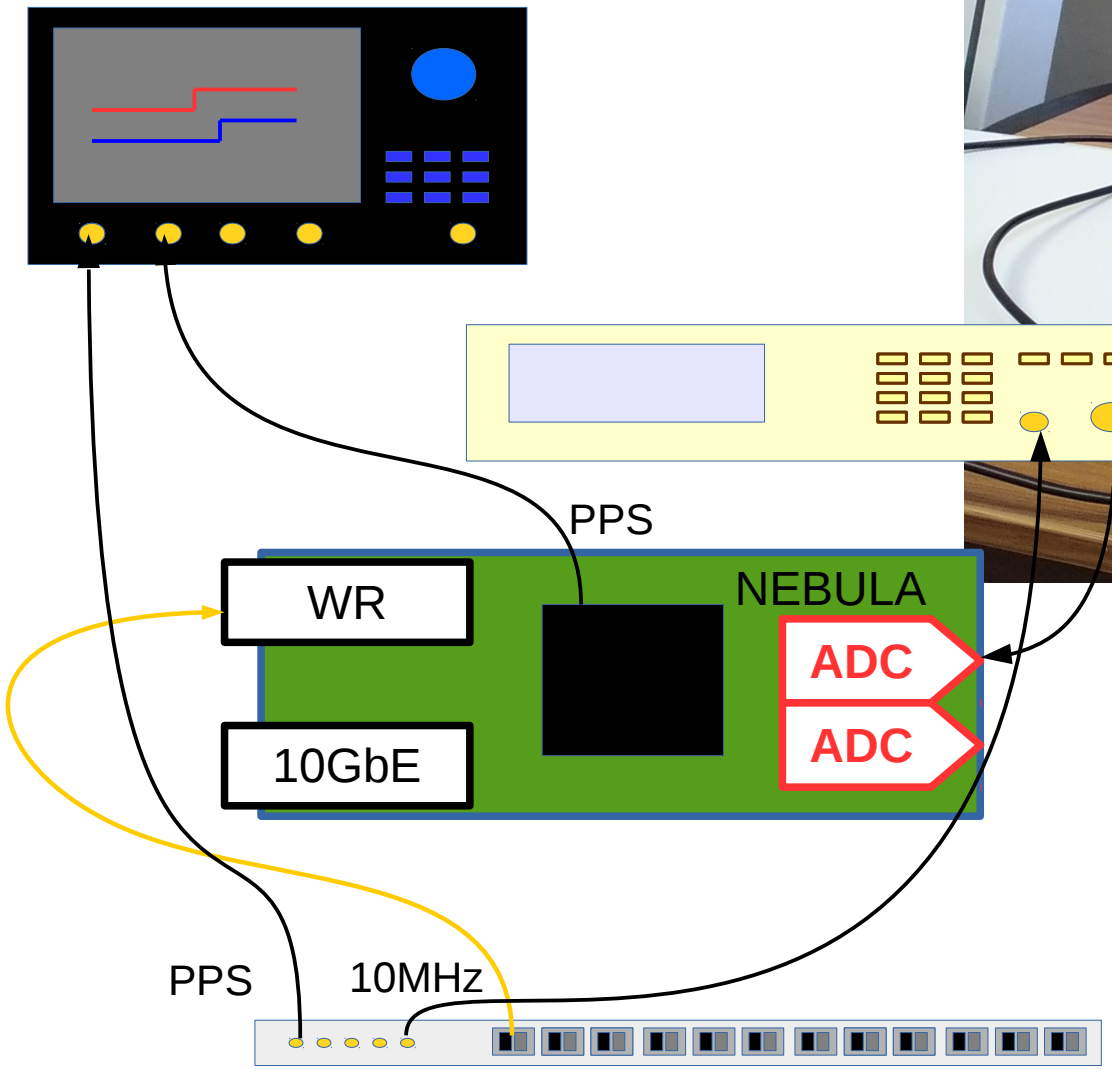
NEBULA Board

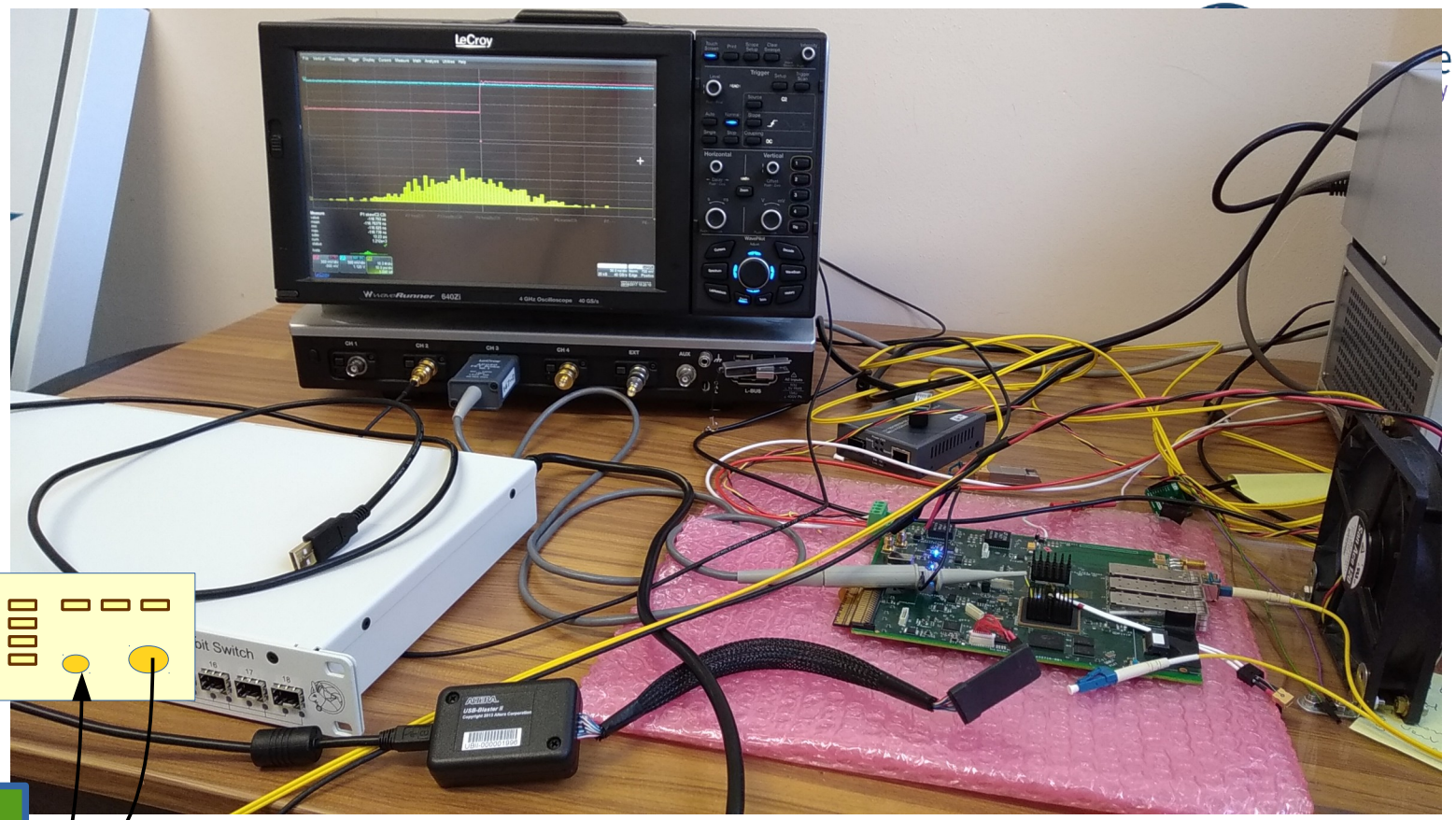
PLL Cleaner

WR components



NEBULA test setup

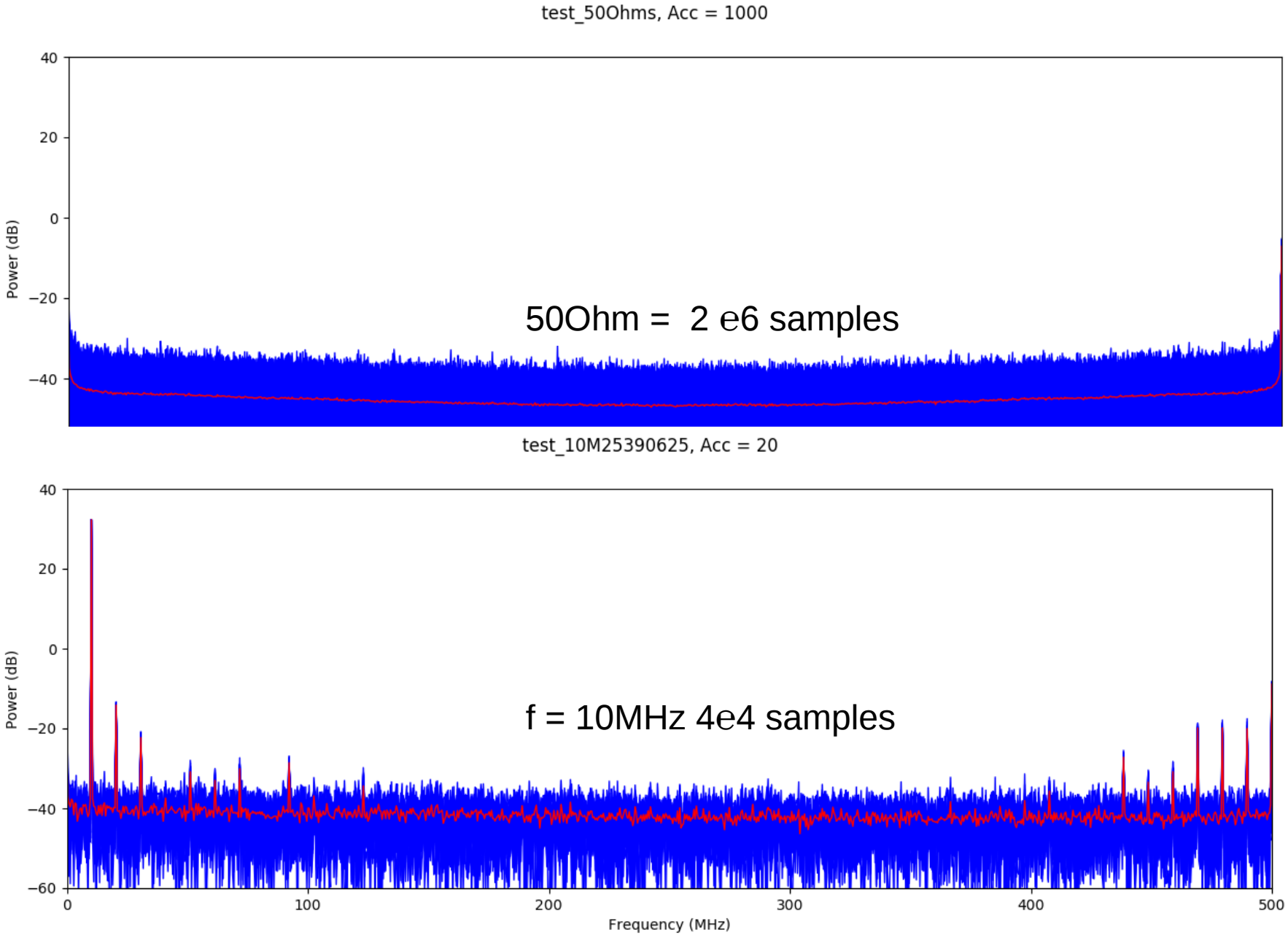




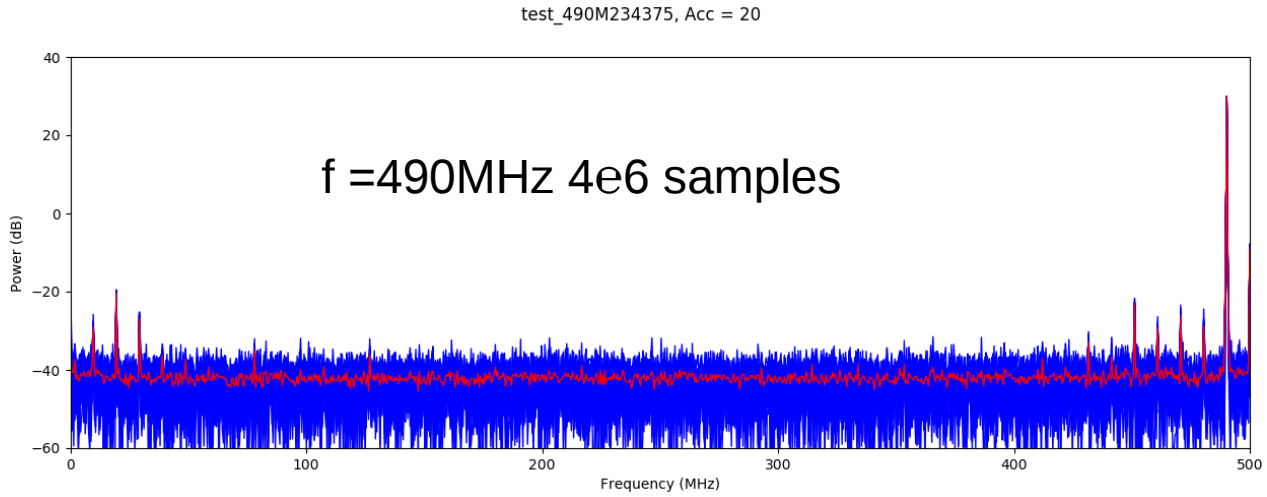
Scope : LecroyWave Runner 640Zi 40GS/s
SinWave generator : AGILENT E8257
White Rabbit Swich: EPQ_WRS_01

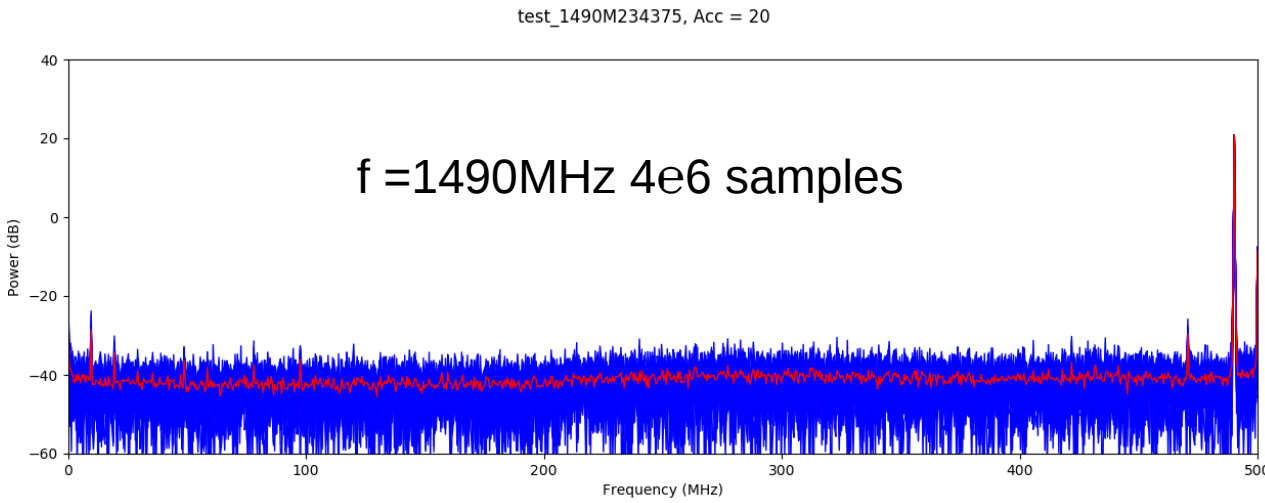
10Mhz for synchronous sampling

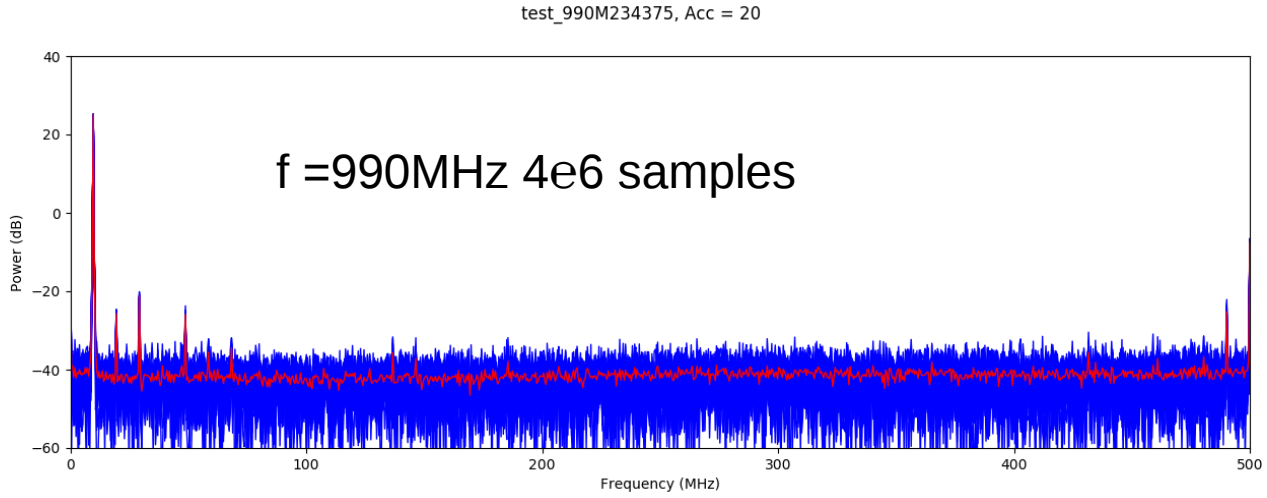
NEBULA analog results (1)

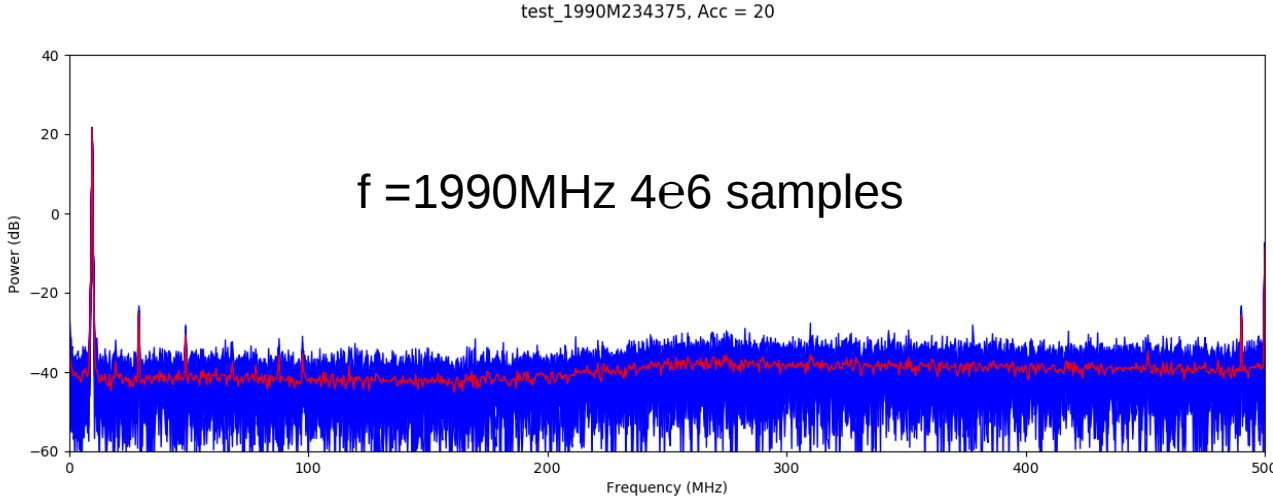


NEBULA analog results (2)

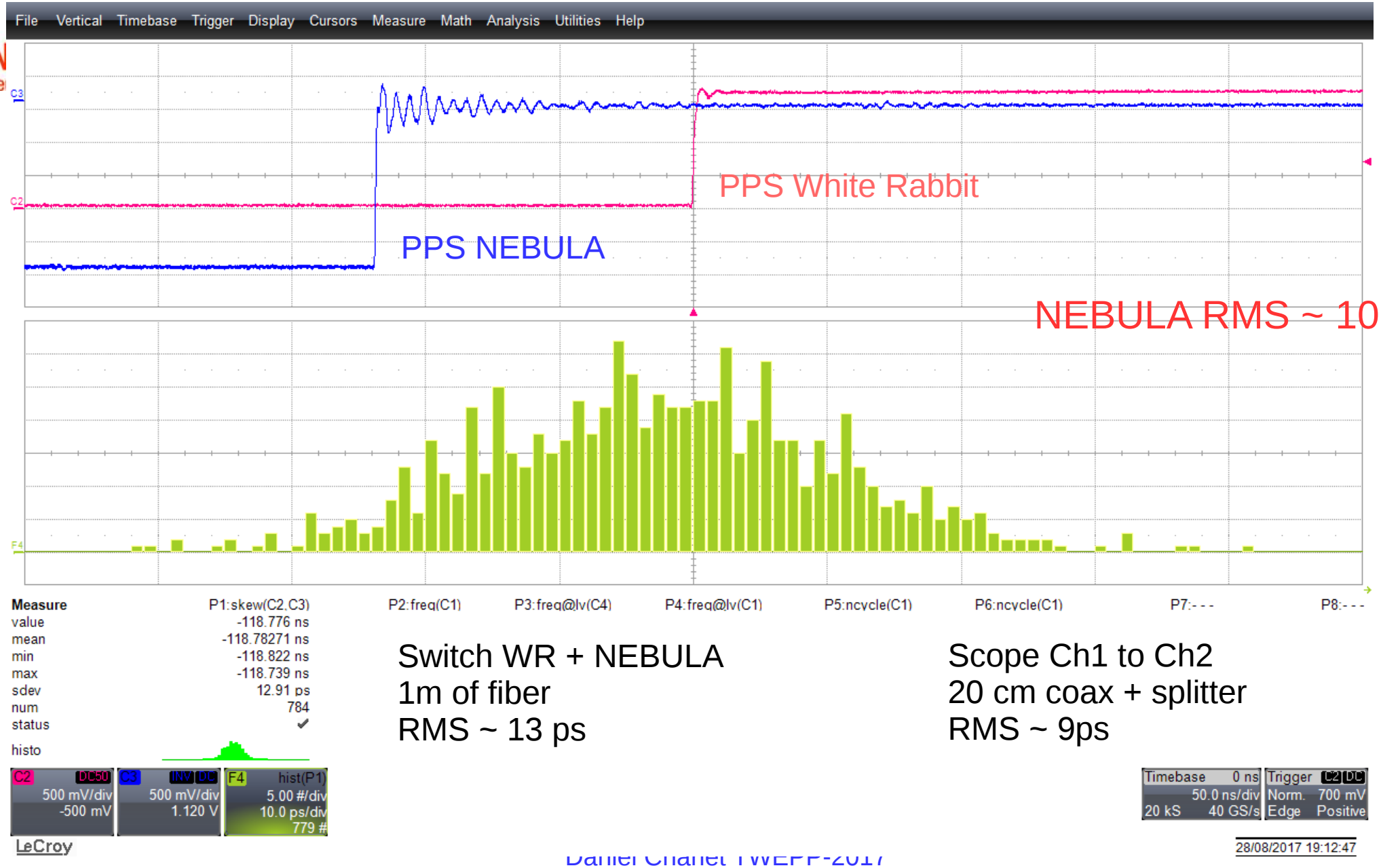








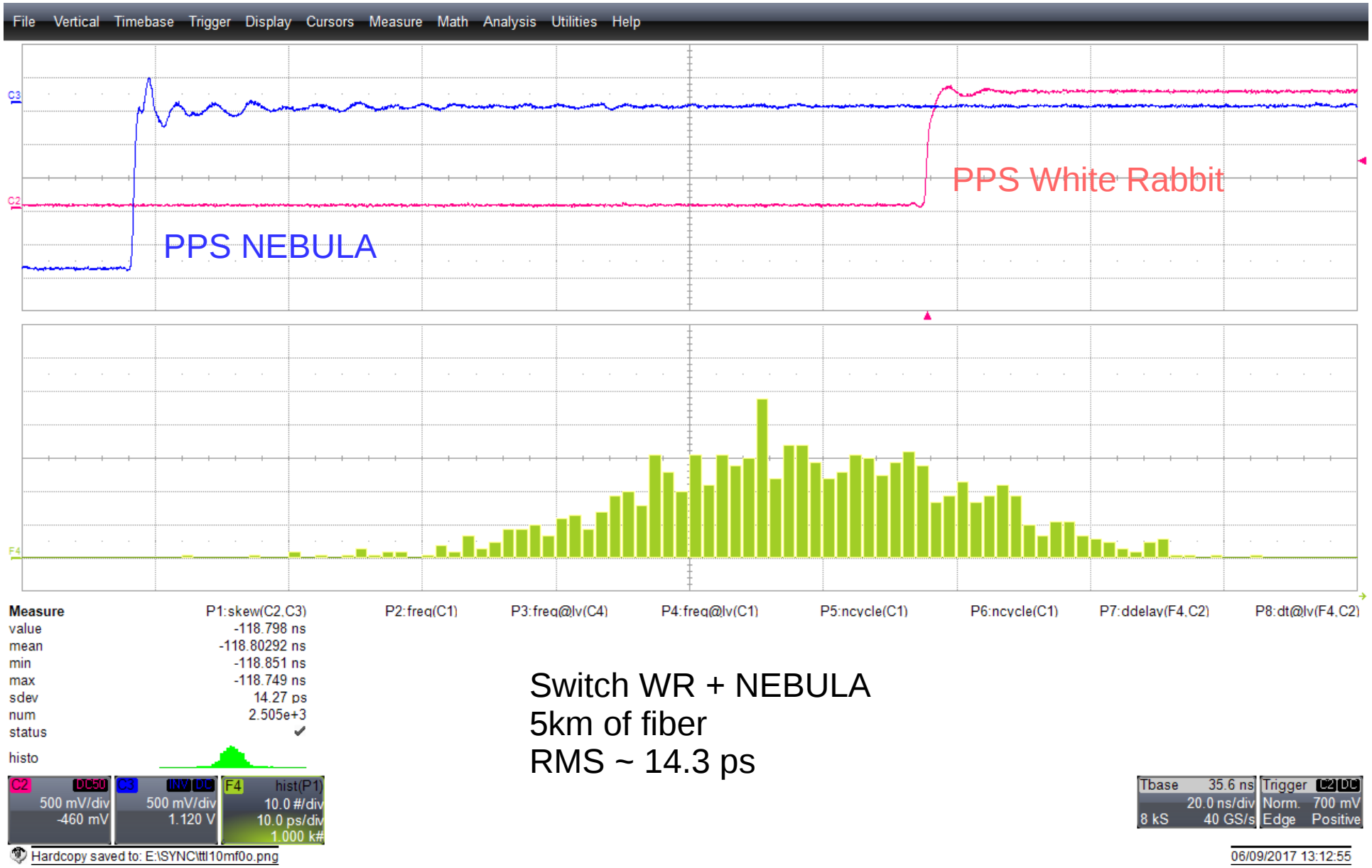
NEBULA timing results (1)



Switch WR + NEBULA
1m of fiber
RMS ~ 13 ps

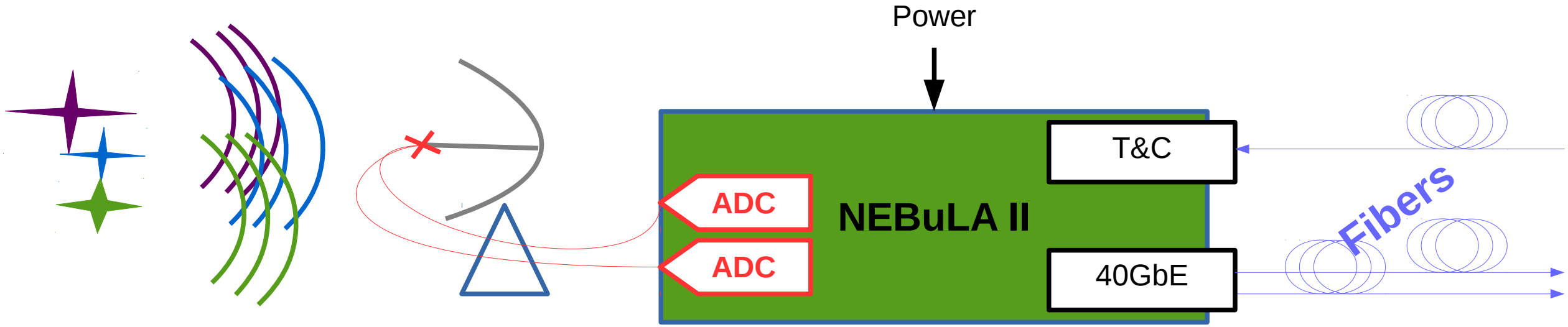
Scope Ch1 to Ch2
20 cm coax + splitter
RMS ~ 9ps

NEBULA timing results (1)

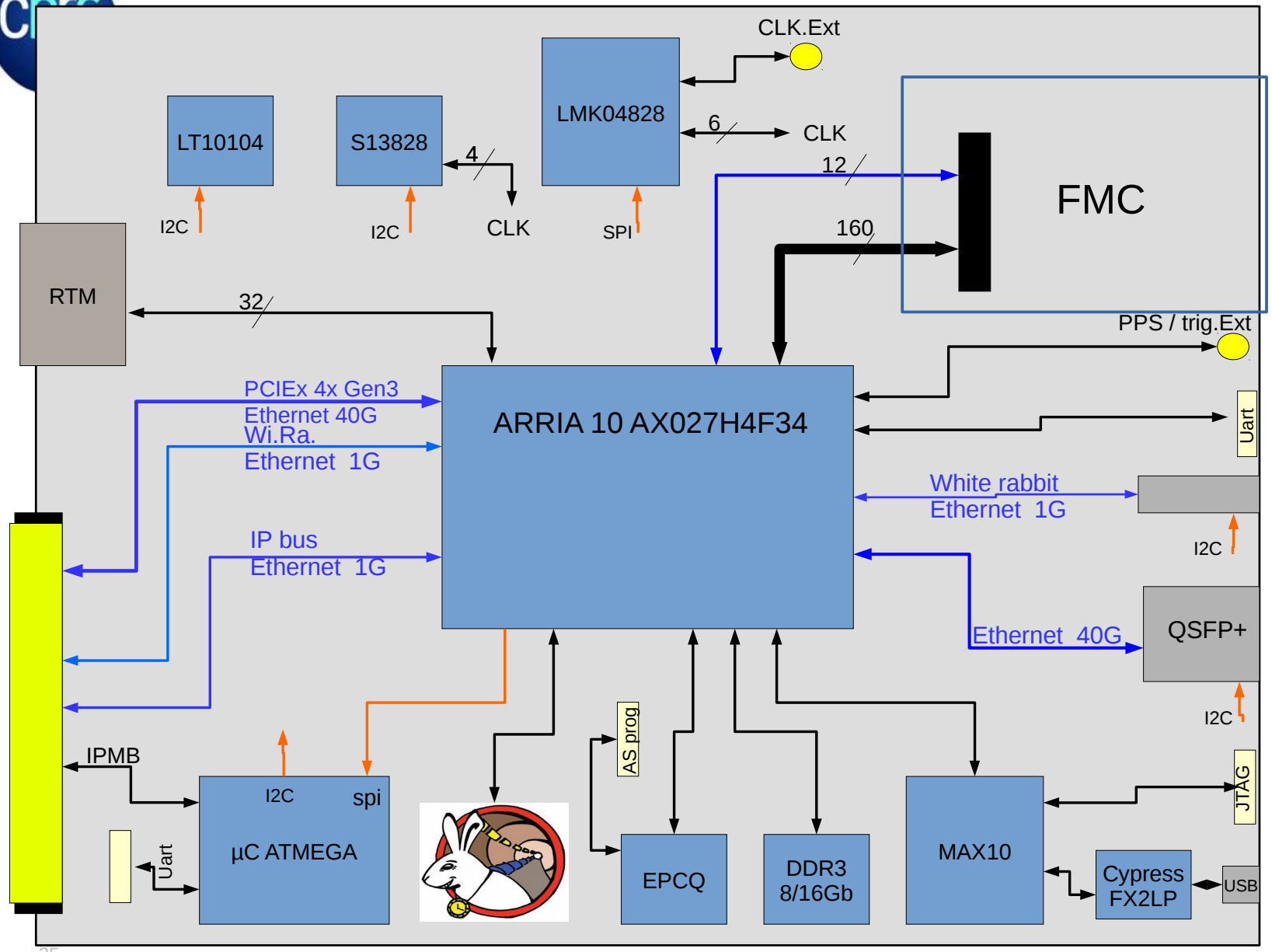


Switch WR + NEBULA
5km of fiber
RMS ~ 14.3 ps

NEBULA II



NEBULA II

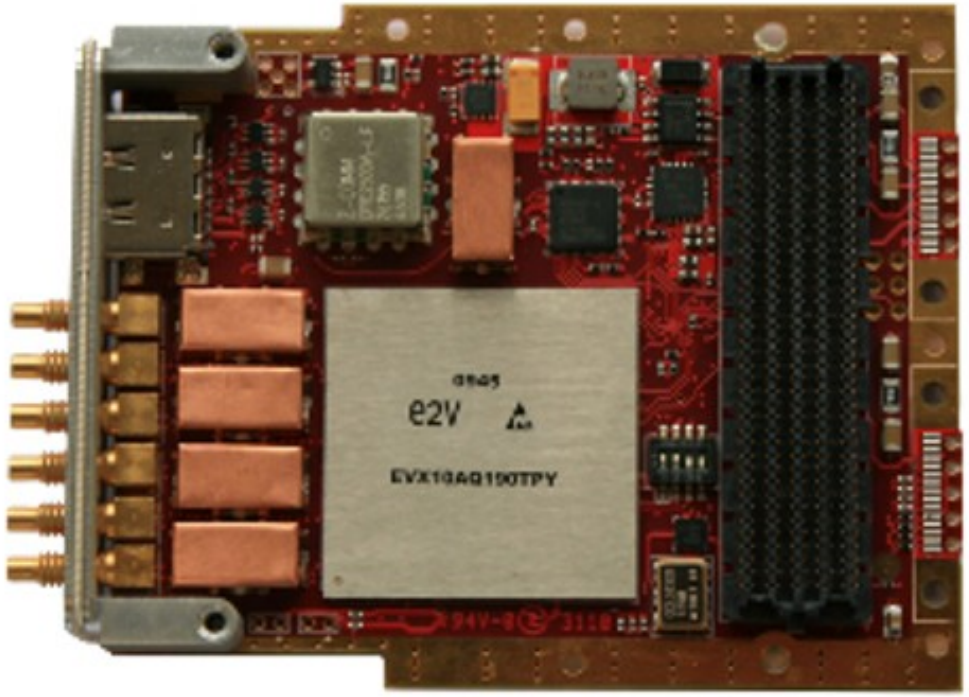


- MTCA 4.0 standard, Double-width, full size AMC
- FPGA : A10GX027H4F34
- FMC : HighPinCount FMC slot
- White Rabbit compliant.
- Front panel : WR SFP+, USB, QSFP+ 40GbEth, UART
- Backplane connectivity : Gbe IP bus, PCI 4x Gen3/40GbEth, IPMB, CLK & trigger lane, RTM connector, Gbe
- Memory : SDRAM DDR3 8/16Gb
- Stand-alone mode
- Intergrated USB-BLASTER II
- FPGA configuration : Active serial.
- Stand-alone configuration (µC).
- Very low noise PLL cleaner LM04828

Conclusion

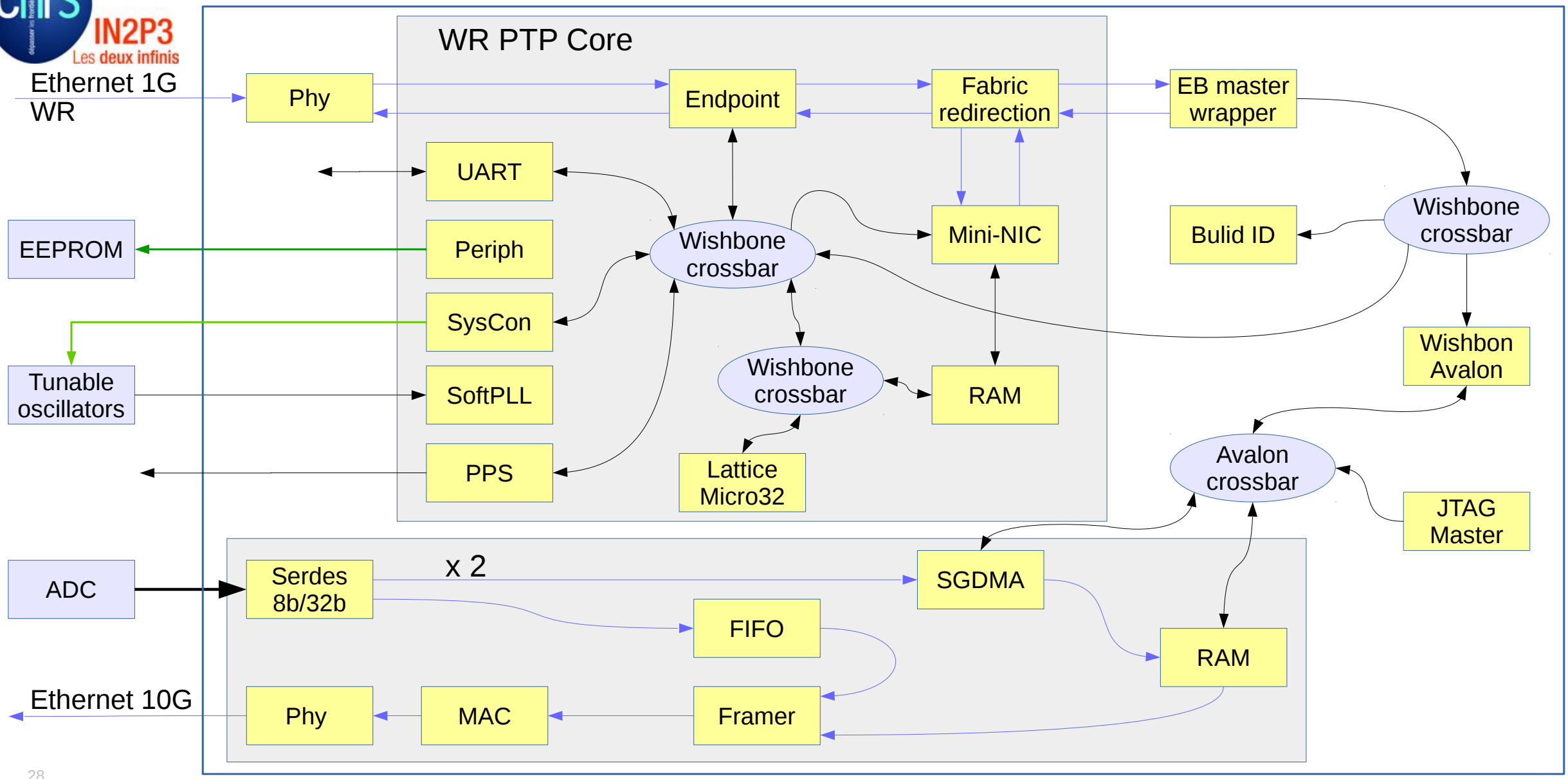
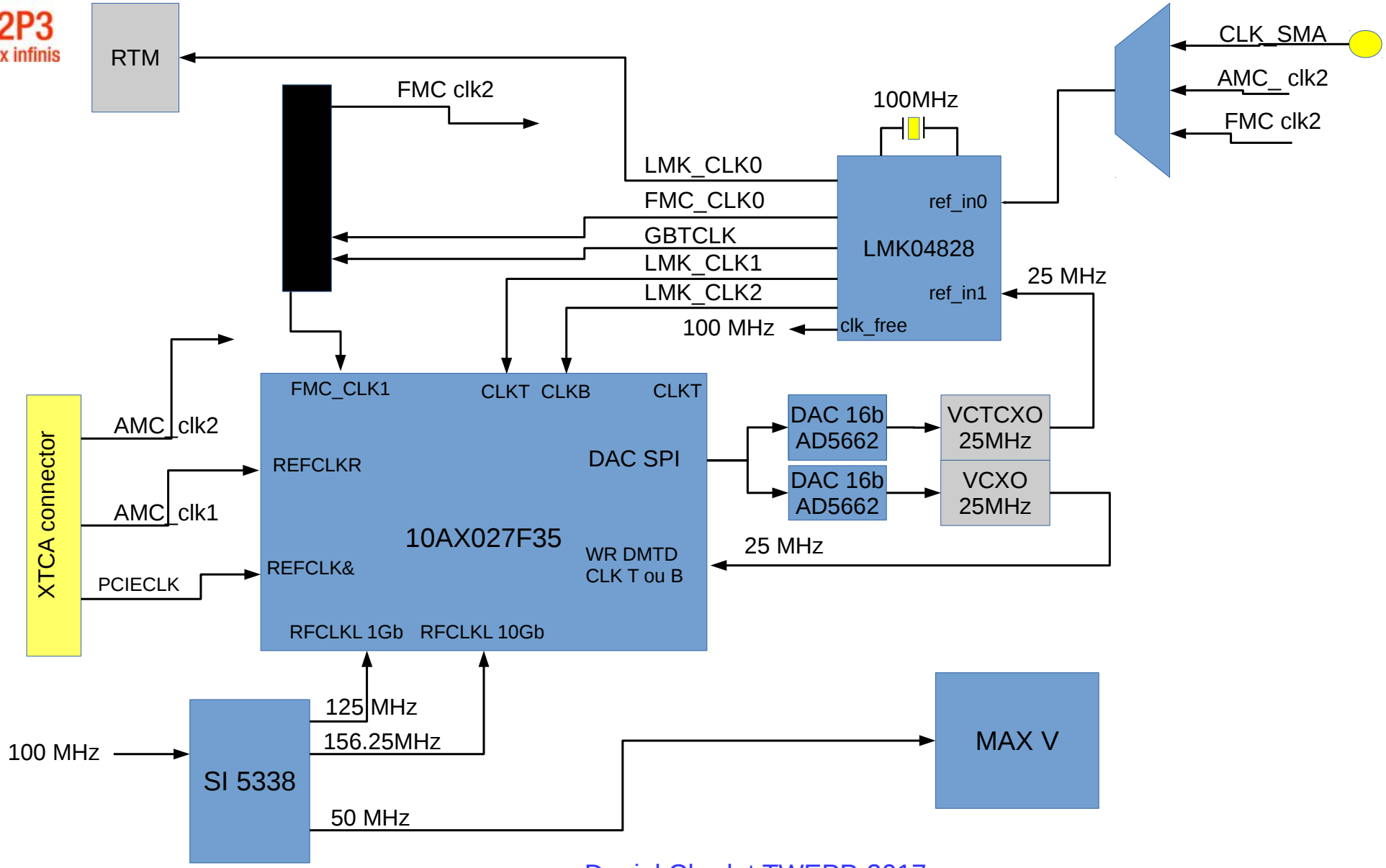
- NEBuLA
  - Validation of the main technical concept : WhiteRabbit and High band ADC
  - Soon: 2 10Gbe data transfer
- NEBuLA II
  - 2 boards : Calibration for subns precision
  - Time difference between 2 Boards
  - 40Gb Ethernet Data transfer

4DSP FMC 125



- Form Factor FMC
- Cooling Air, Conduction
- Function Analog Input
- Data Rate 5000 (1 Ch) or 2500 (2 Ch)
- 1 250 (4 Ch)
- Channels 1 , 2 or 4
- Coupling AC
- Resolution 8-bit
- FMC Connector HPC
- Signaling LVDS

NEBULA FPGA synoptic



NEBULA II Clock tree