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NEBULA Large Band Digitiser for Radio Astronomy

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NEBuLA is a large band autonomous digitiser under development, with use cases in radio astronomy.
We present the scientific rationale and the specifications of the project, We describe the board overall architecture,
the implementation of the different links: synchronisation, command, control and data transfer. We present the solution adopted to fulfil the main requirement of the project which is the possibility to synchronise the clocks of multiple boards separated by distances up to several km. Finally, we present the firmware and the software that we have developed for debugging, control and configuration and data transfer.

Summary

The PAON is the demonstrator of a transit radio interferometer radio devoted to make 3D map of the hydrogen in the universe through observation of the 21 cm emission of the atomic hydrogen at 1420 MHz.
Paon IV is composed of 4 dishes, with a diameter of 5 meter, and uses interferometric beam forming technique to map the sky. Each antenna is equipped with a dual polarisation feed connected to 2 acquisitions'channels of 250Mhz bandwidth at 1375 MHz.
A frequency down conversion is performed by modules located under the antenna. A centralized VME crate including ADC boards, which sample the analogue signal at 500Mz, performed 8096 points FFT and transfer data on optical fibre to a PC farm for visibility computation.

One of the limitation of the current centralised acquisition system is the long length of coaxial cables, which are responsible of modulation by standing waves. This modulation limits the system performance and complexities the offline data processing. To deal with this problem we have developed a distributed architecture with ADC boards that could be deployed directly on the antennas. As a consequence, an efficient distributed clock synchronisation is mandatory, as well as a very low level EM field emission.

The Nebula board is an xTCA full size board base on ARRIA V GT FPGA which can also work in stand alone mode. It requires 12 V power supply and 2 optical links. It also include one 2 channels 1Gsp ADC a ADC08DC1020 from TI .
The clock synchronisation and the time distribution is performed by the white rabbit protocol which allows also the transmission of control and configuration signals of the board. The data transfer is handled by 2 x 10Gb links.
For the ADC clock, we can tolerate a maximum jitter of 300 fs. To obtain this low jitter level we use a LMK04828 in the white rabbit loop, the latter generates all the clocks of the board (10Gb Ethernet, 1Gb Ethernet, ADC, FPGA system). On chips configuration bus and the IPMI protocol is done by uC ATMEGA128. QDRII and FPGA parallel flash configuration are also implemented. When NEBULA boards are plugged in a crate, the Ipbus should be used in place of the White Rabbit to configure and control the board.
For reading data, PCIe 4x Link is connected to the backplane. We mainly use the QSYS tool to develop the system firmware . All the FPGA functions are interconnected by the Avalon bus. A specific interface has been defined for a dedicated link : white rabbit and Ipbus. A Control panel has been developed in QT for board debugging. Specific data acquisition and visibility computation software, as well as data visualisation tools using the SOPHYA C++ class library
has been developed and runs on the PCs farm.
A more advanced version of the NEBuLA board is under development, to add local computation capability

and to have a more versatile system, based on ARRIA 10Soc and replacing the ADC by one FPGA Mezzanine Card (FMC) socket.

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