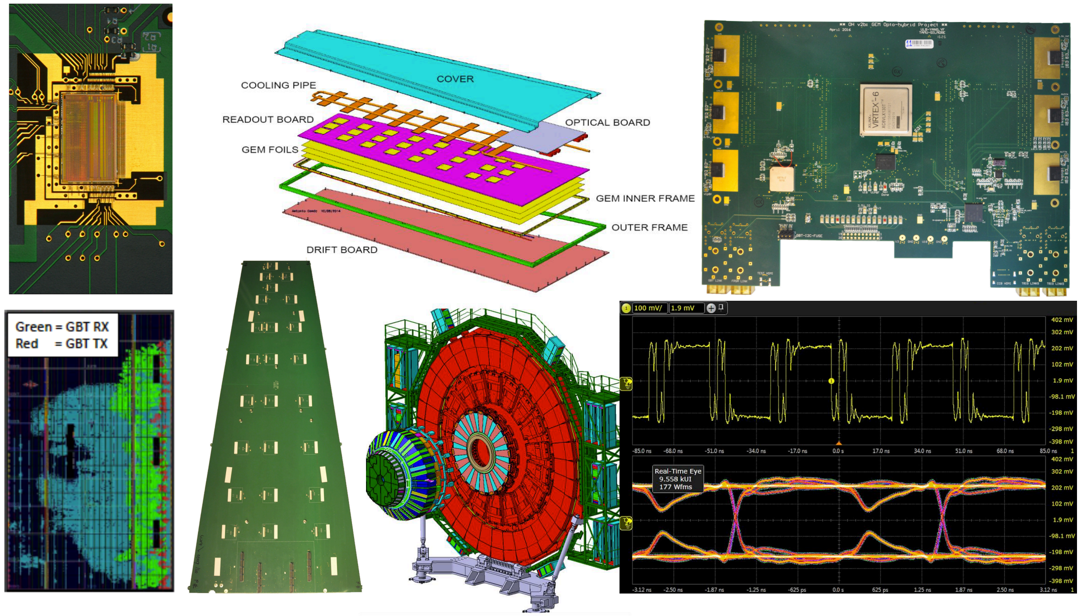
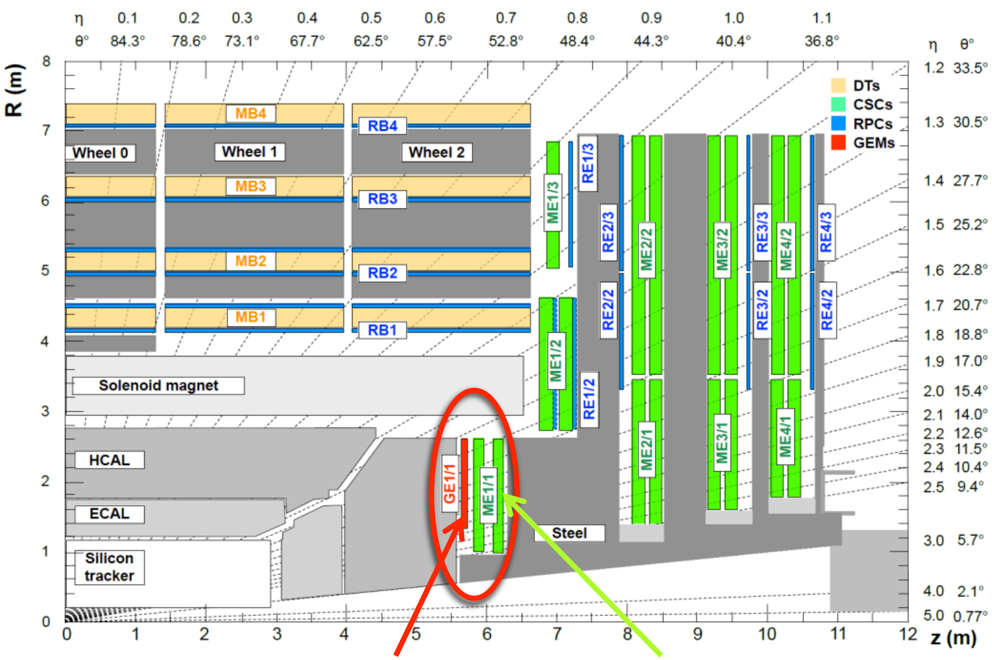
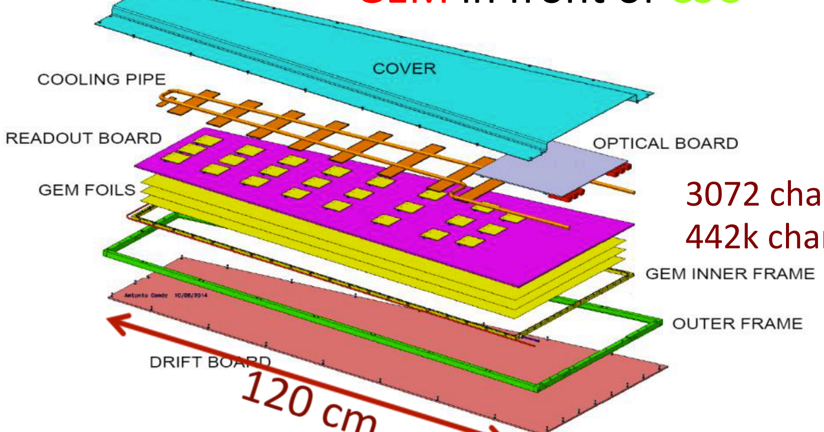
Development of the readout system for Triple-GEM detectors for the CMS forward muon upgrade

G. De Lentdecker (ULB), on behalf of the CMS Muon Group



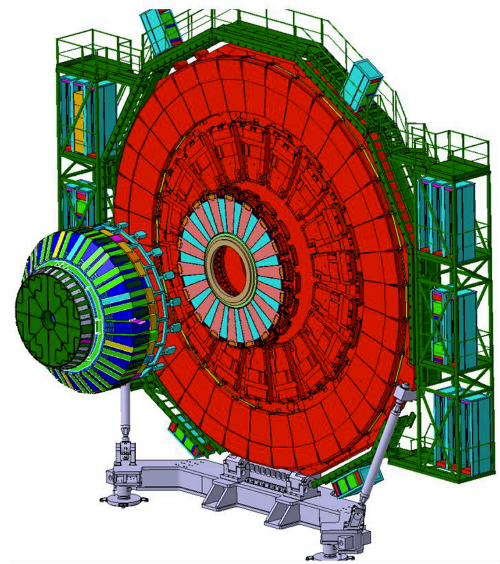
CMS GEM upgrade (aka GE1/1)



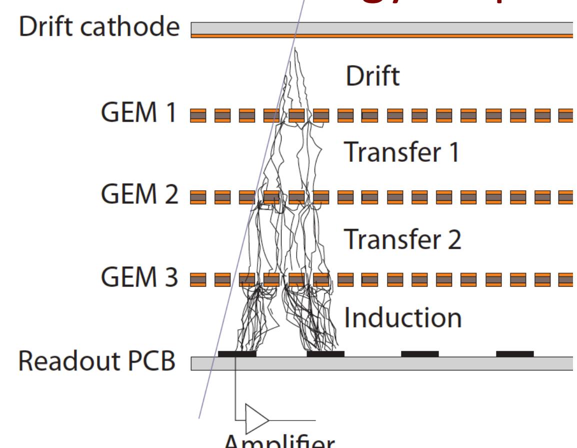


3072 channels/detector
442k channels in GE1/1

- Planned for 2nd LHC Long Shutdown (2019-2020)

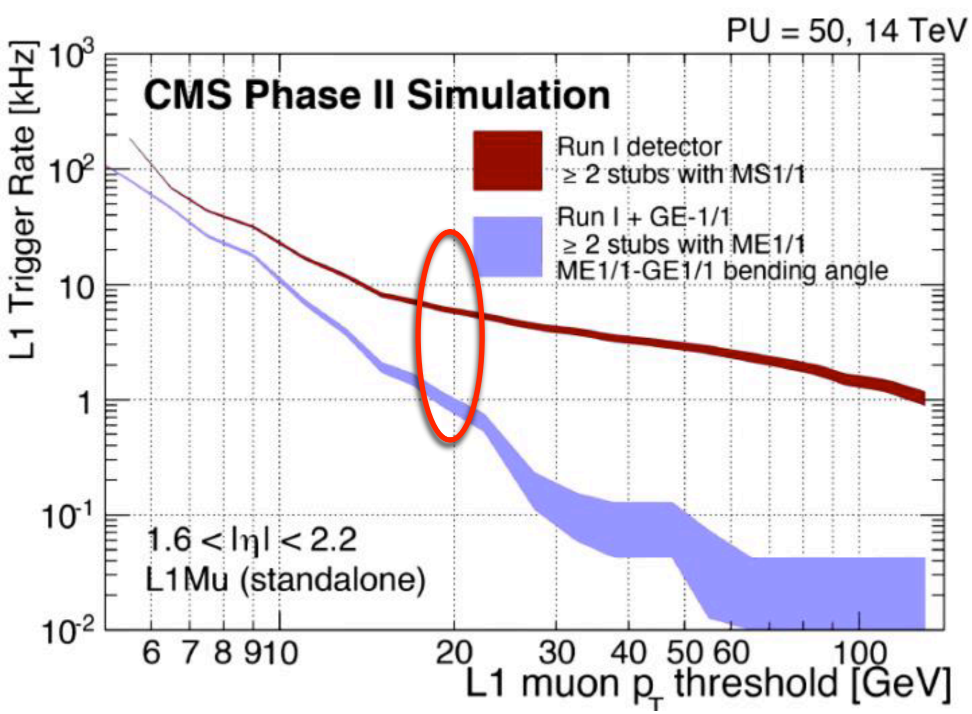


- Detector technology: Triple-GEM



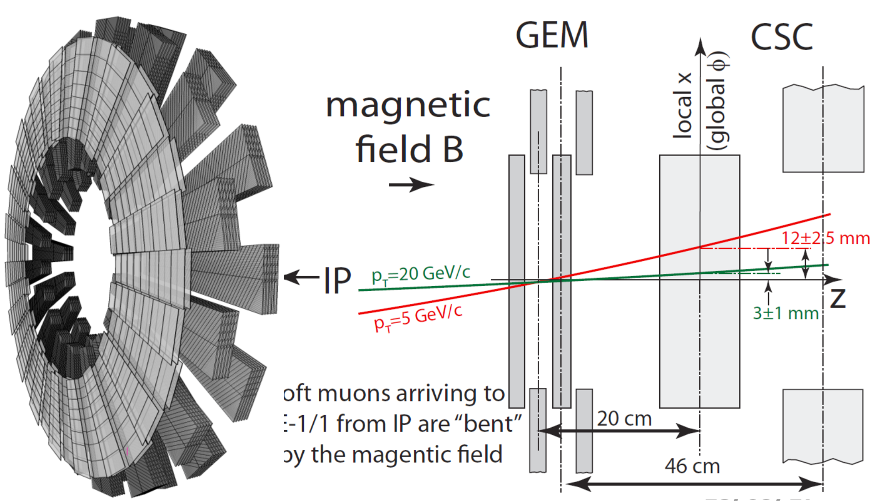
Physics motivations

- Need to maintain excellent trigger performance for forward muons during Phase II
  - 100 kHz allocated for all muon triggers at Level-1



Problem: Level-1 trigger rate "flattening"

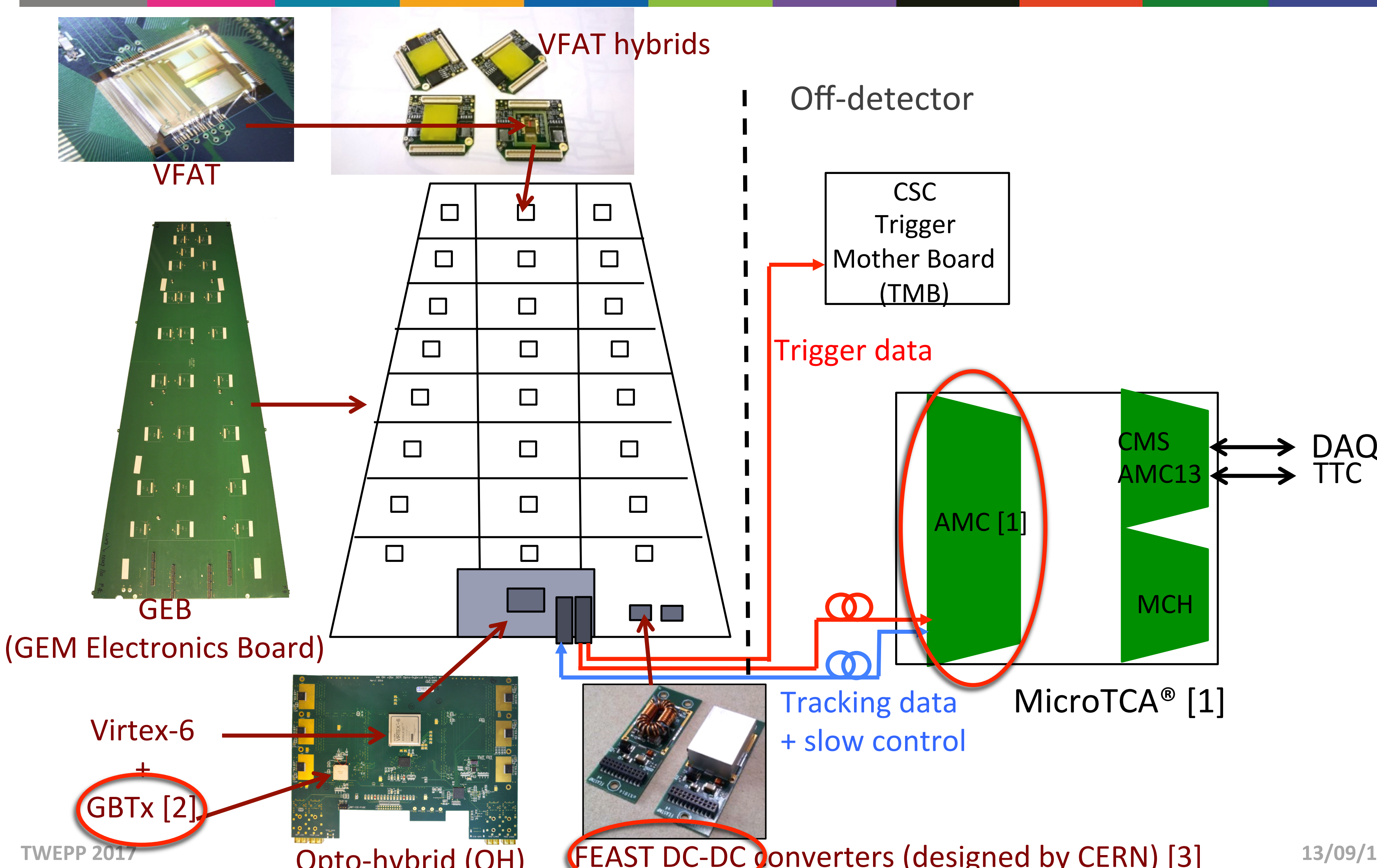
- Soft muons scattering can occasionally have stubs aligned like for a high-P_t muon (rare, but lots of soft muons)
- Level-1 muon-trigger momentum can be improved by measuring the bending angle combining GEM & CSC data:



Outline

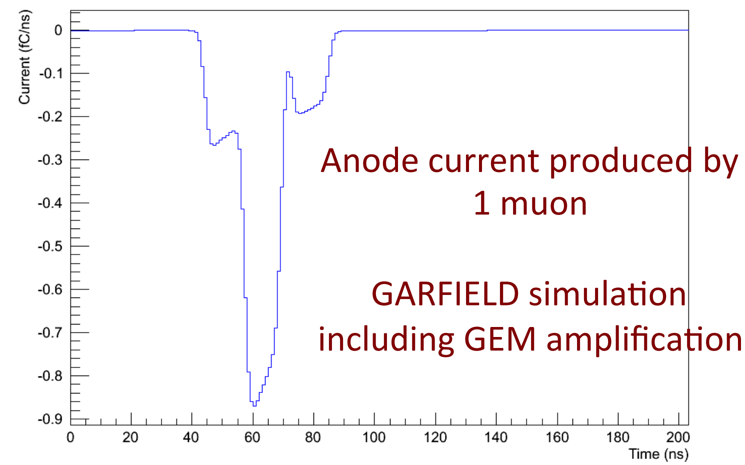
- GE11 Electronics Overview
- Specifications
- Slice Test Demonstrator
- GE1/1 electronics architecture
- VFAT3
- GE1/1 electronics status
- Further upgrades

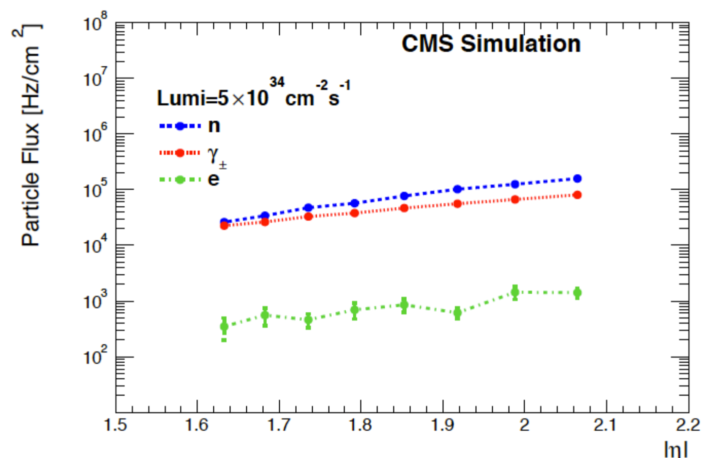
GEM Electronics overview



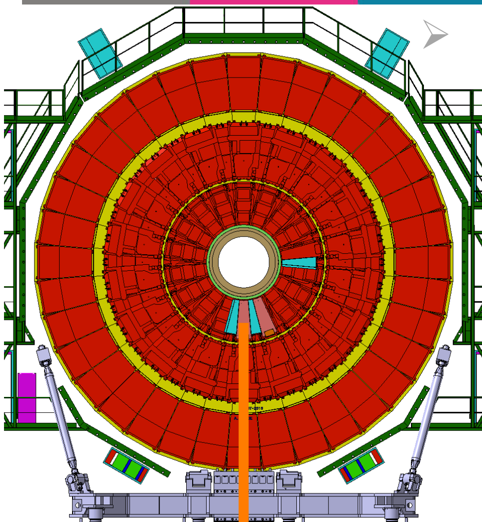
CMS GE11 Electronics specs.

- CMS Triple-GEM
  - signal length: ~60 ns
  - detector capacitance: 10-30 pF
  - charge range (MIP): 4-110 fC
- Expected particle rate
  - up to 2 x 10^5 Hz/cm^2
  - mainly neutron background
- CMS Level-1 latency: up to 12.5 μs
- CMS Level-1 Accept rate: up to 1 MHz
- Total irradiation dose: up to 10 krad
- Data volume (per detector)
  - Trigger: < 100 Mbps (zero suppressed)
  - Tracking (at L1A = 1MHz): 5 Gbps (not zero suppressed)



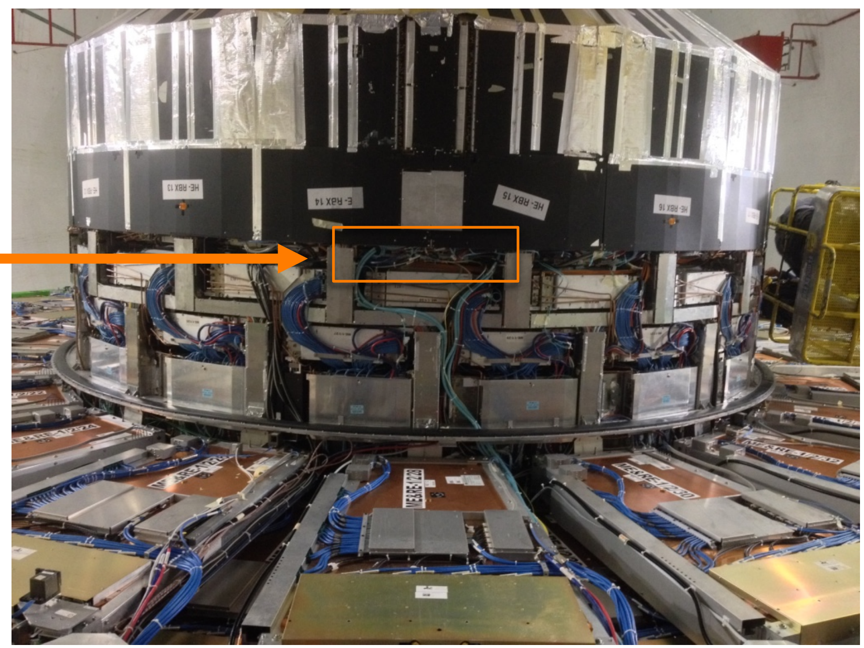


Winter 2017 : demonstrator aka slice test

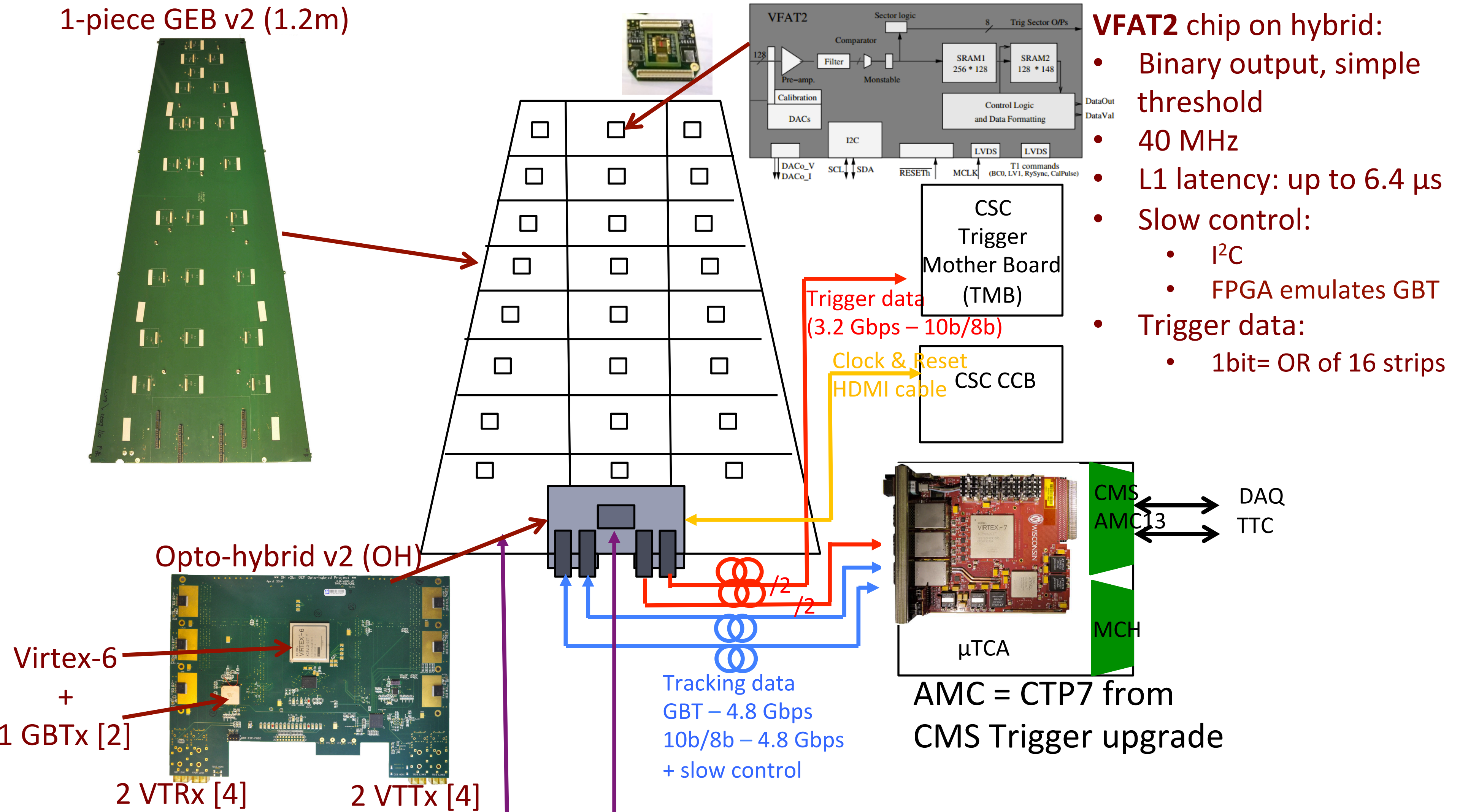


➢ To gain experience in installing, commissioning and operating in CMS 5 back-to-back Triple-GEMs have been installed

- To study detector and electronics performance in CMS (noise, efficiency, timing, …)
- To test trigger data path to CSC trigger electronics
- Equipped with front-end electronics prototype versions
  - VFAT2, Opto-Hybrid v2, GEB v2
- Back-end components are production version

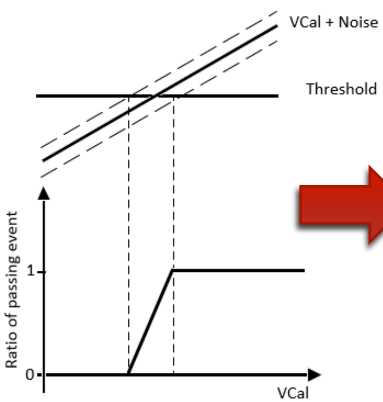


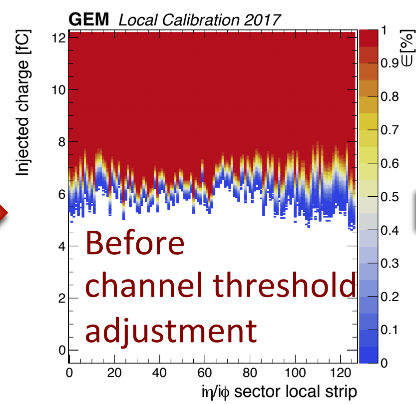
Slice test electronics

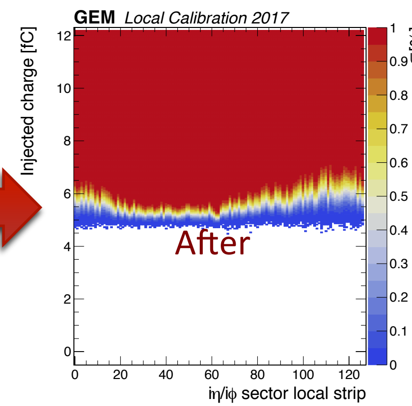


Commissioning

- First results:
  - Calibration of the Front End chip and noise characterization
  - Use VFAT2 built-in calibration feature: s-curve

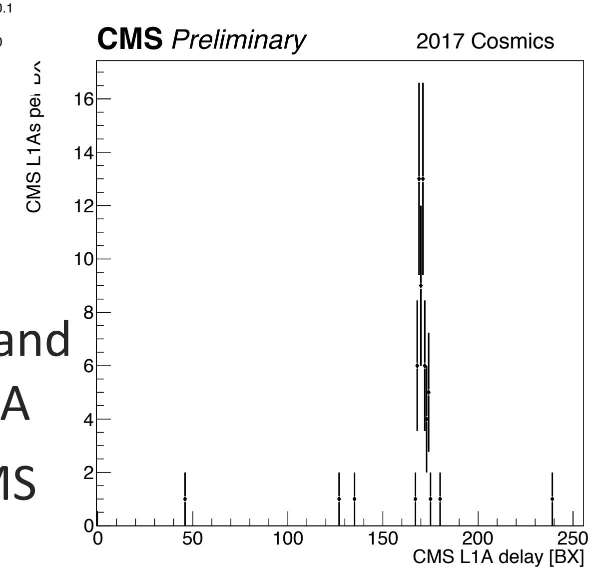






More uniform SNR

- Starting to time-in the system
  - Time difference between the CMS L1A signal and the chamber trigger data, counted by OH FPGA
  - 1st muons (cosmics) seen by Triple-GEM in CMS



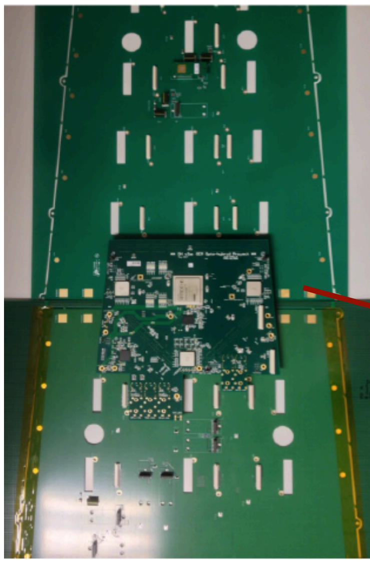
Next steps

- Mainly software
  - GEM DAQ & Detector Control System (DCS) integration to central CMS online system
    - Will allow to combine GEM & CSC data
    - GEM data currently stored on local disks

- Note: LHC is running well and CMS is taking physics data while the commissioning of the GEM demonstrator is ongoing
  - This not optimal for commissioning ;-)
  - GEM demonstrator can't interfere in any way with the smooth CMS data taking
    - Some times have to wait for long time before performing any tests

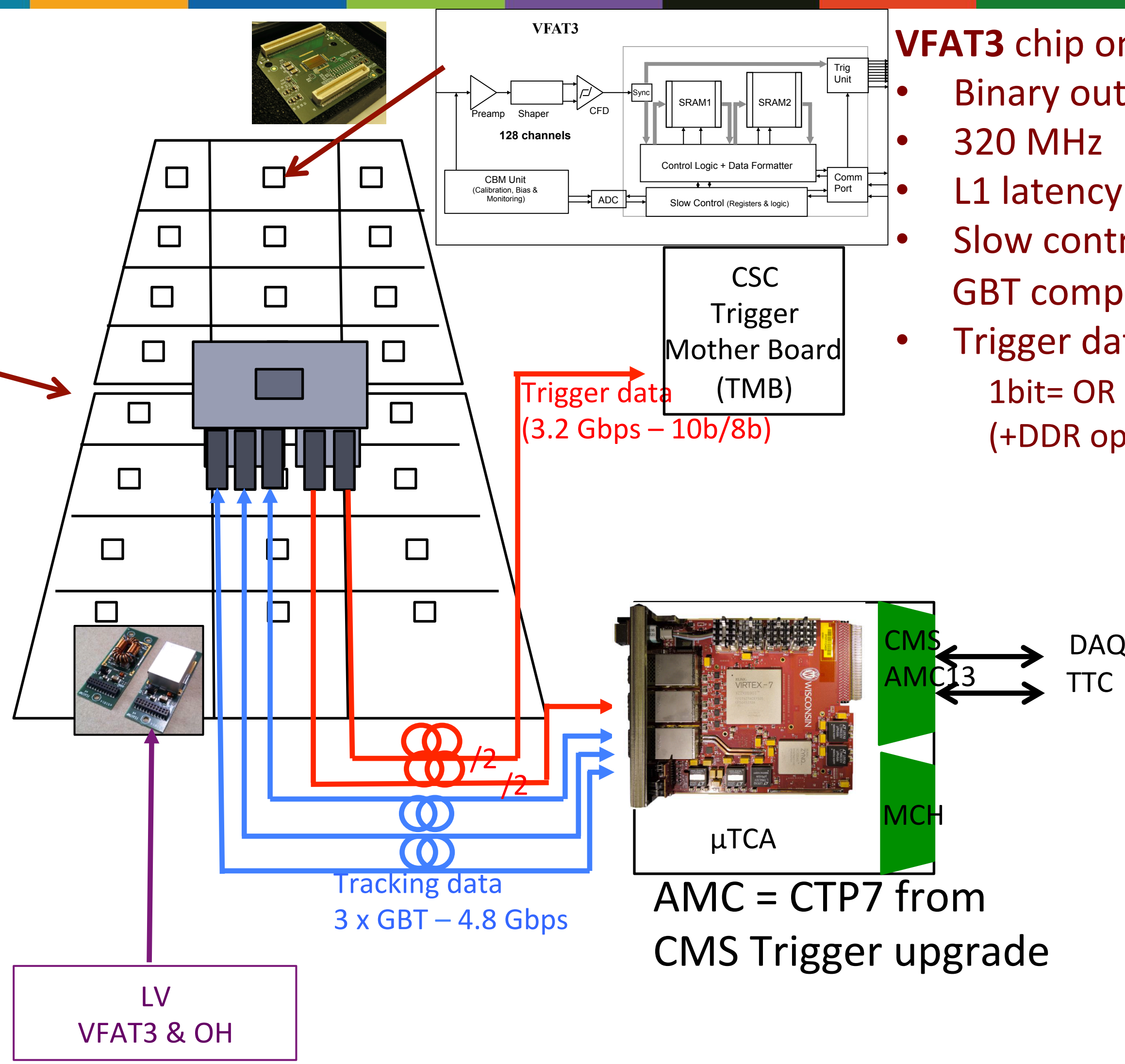
Final GE1/1 electronics

2-pieces GEB v3 (1.2m)



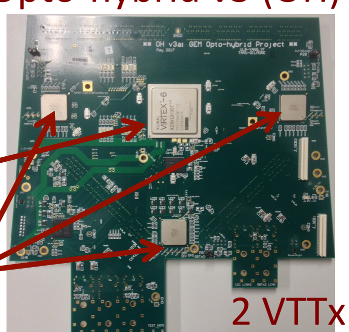
VFAT3 chip on hybrid:

- Binary output, CFD
- 320 MHz
- L1 latency: up to 12 μs
- Slow control: ePort, GBT compatible
- Trigger data:
  - 1bit= OR of 2 strips (+DDR option)



AMC = CTP7 from CMS Trigger upgrade

Opto-hybrid v3 (OH)

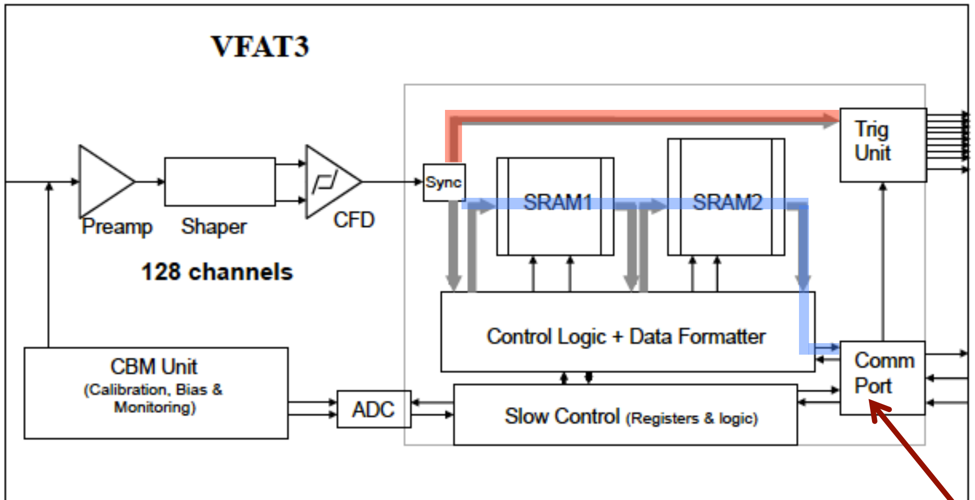


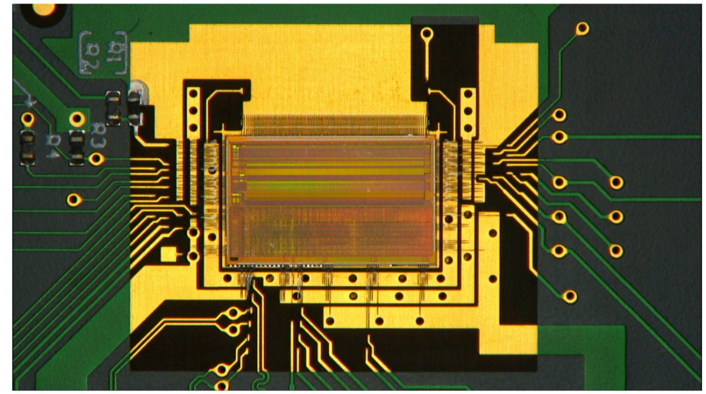
Virtex-6 + 3 GBTx

2 VTTx

3 VTRx

VFAT3





VFAT3, TSMC 130 nm
Wafers received in December 2016

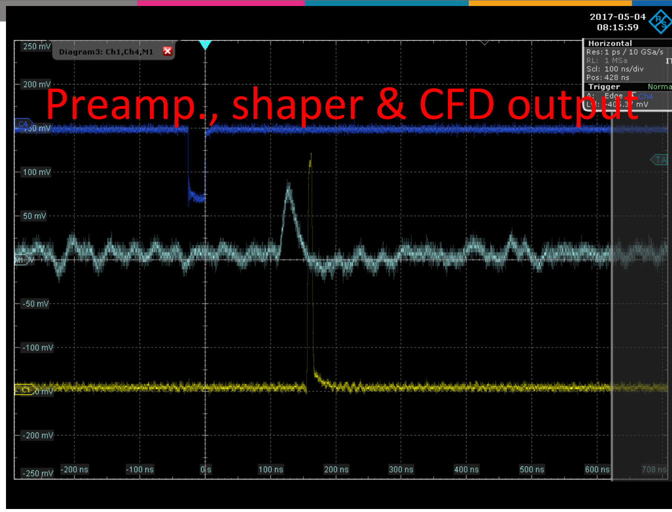
- Detector capac.: 10-90 pF
- Polarity: +/-
- Peak. time: 25, 50, 75, 100 ns
- ENC: <1000 e- (C_d= 20pF, 50ns)
- Power: <2.2 mW / channel

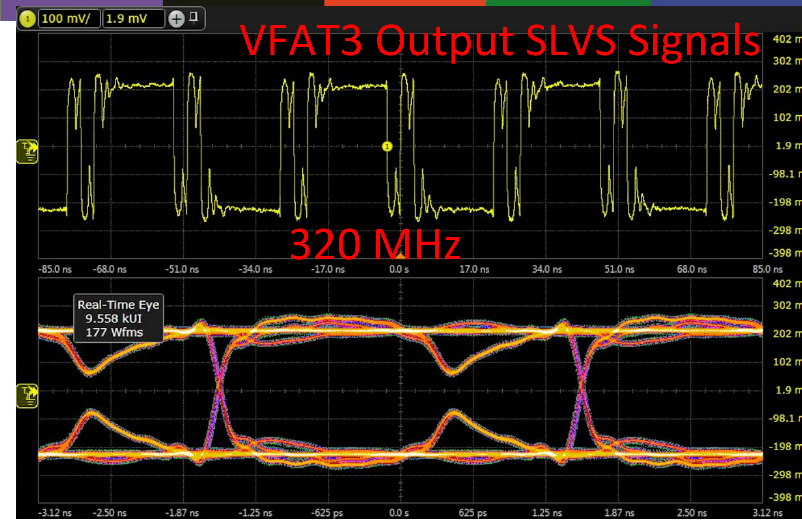
Trigger path: fixed latency
8 SLVS pairs @ 320 MHz 64bits/BX (128bits/BX if DDR)
1 bit (Sbit)= OR of pair of channels
Different data format:
- Lossless
- Partitions
- Double Data Rate (DDR)

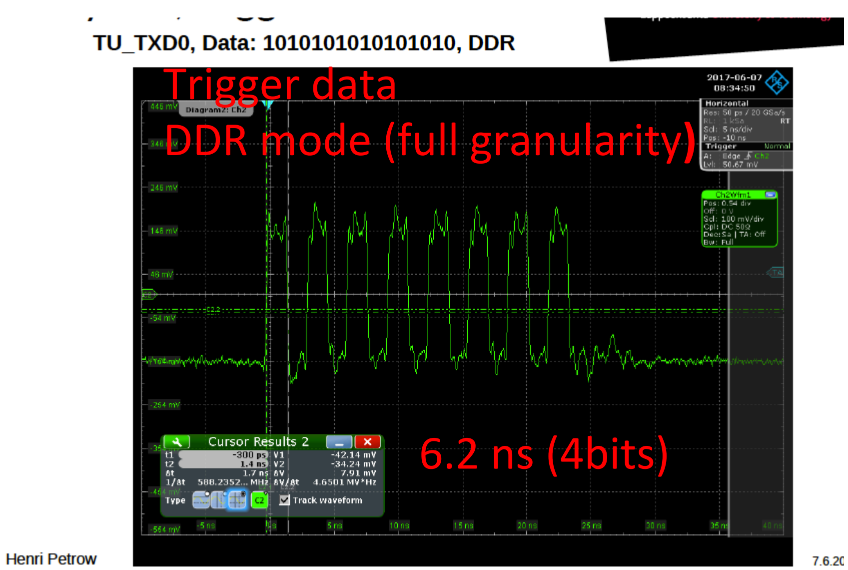
Tracking path: variable latency
Full granularity
L1 latency up to 12.5 μs
L1A rate up to 1 MHz

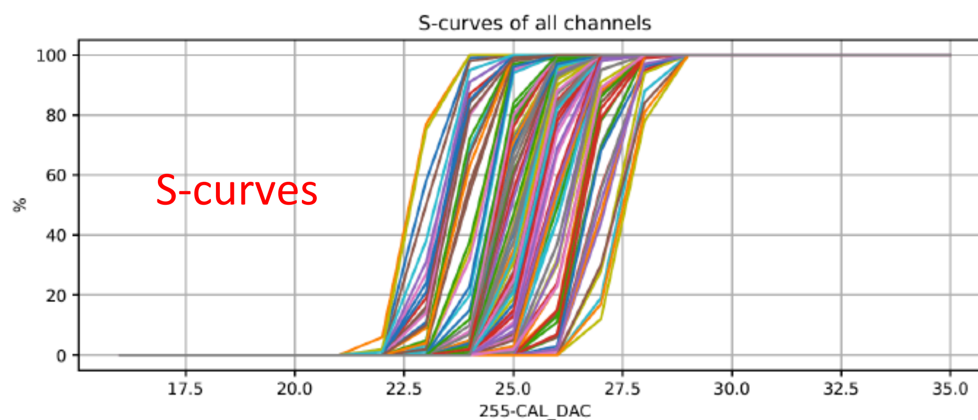
Comm-Port:
Communication interface to GBT
Bidirectional: calibration, bias and monitoring as well as data readout through a single port

VFAT3 functionality test





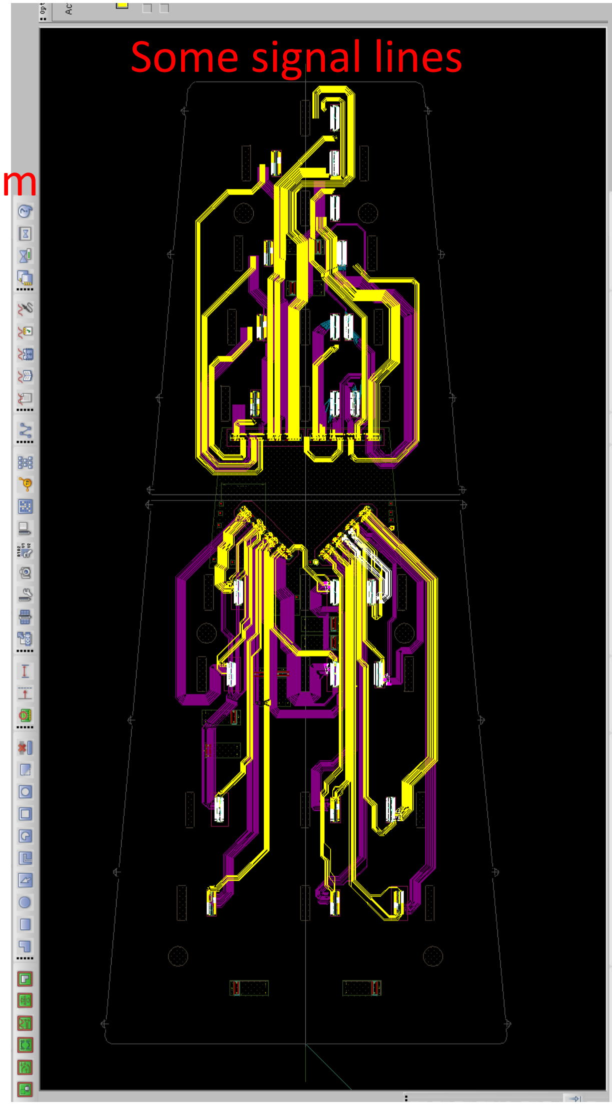


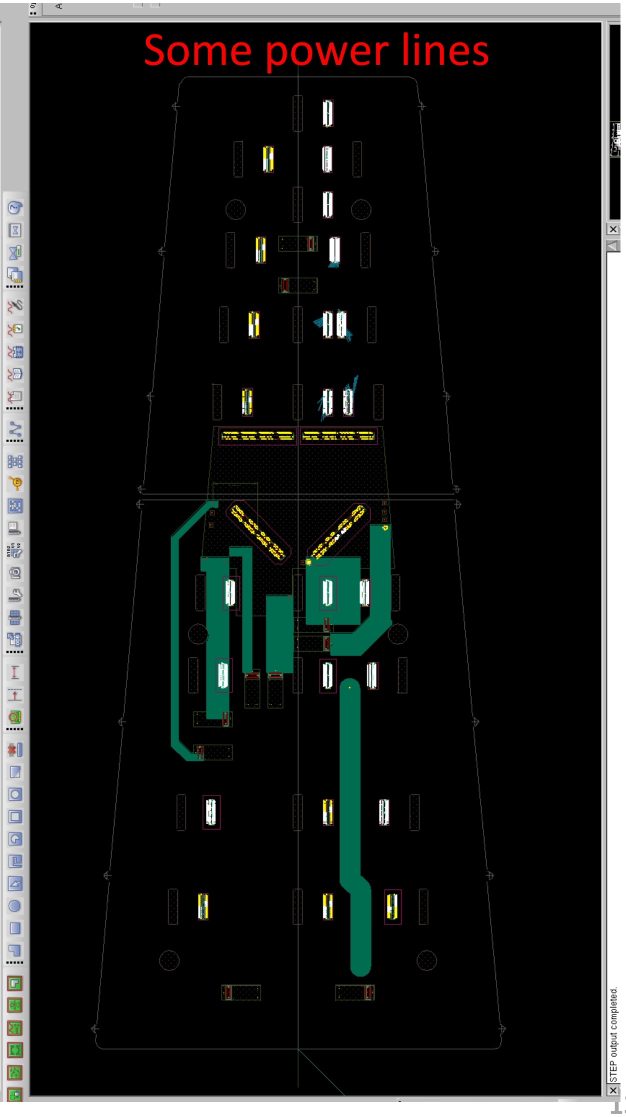


Full VFAT3 characterization is ongoing

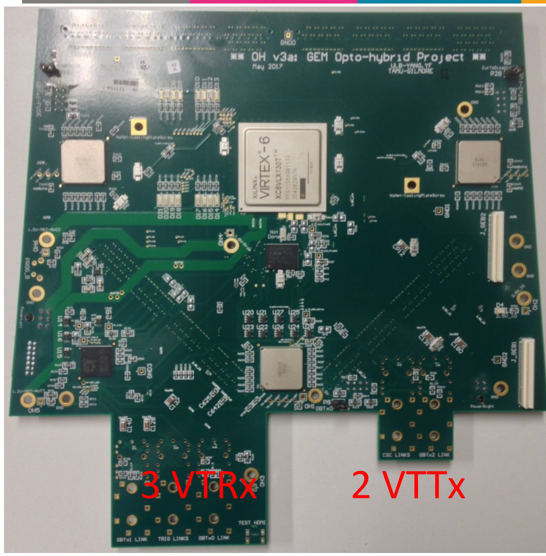
GE11 GEB

GEB v3:
8 layer PCB
Thickness limited to 1.1 mm



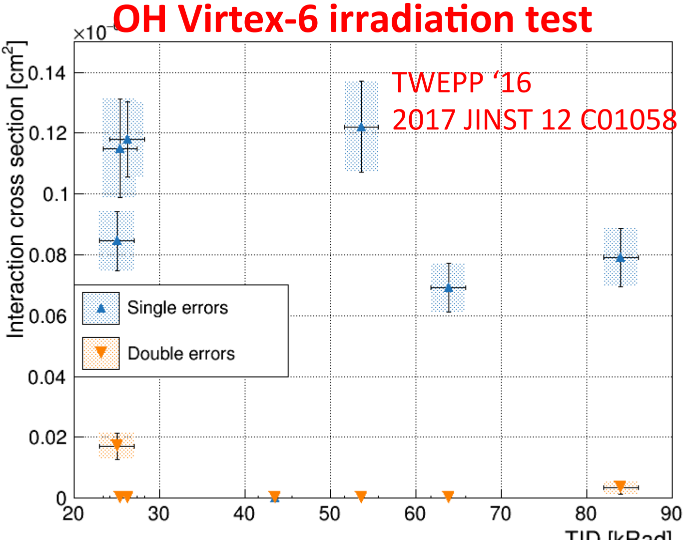


GE 1/1 Opto-hybrid



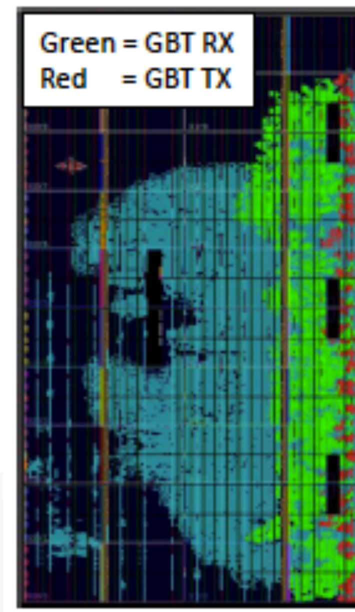
- 3 GBTx chipsets
  - Each GBT can handle up to 10 FE chips @ 320 MHz
- Each VFAT3 communicates with the backend electronics without intervention from OH FPGA
- Only the trigger data transit through FPGA
- One GBT link has JTAG connection (through GBT-SCA chip) with FPGA
  - For FPGA control & programming
  - This was an option in slice test demonstrator but it is now the baseline
- To mitigate possible EEPROM radiation ageing
  - PROM-less reconfiguration implemented

OH Virtex-6 irradiation test

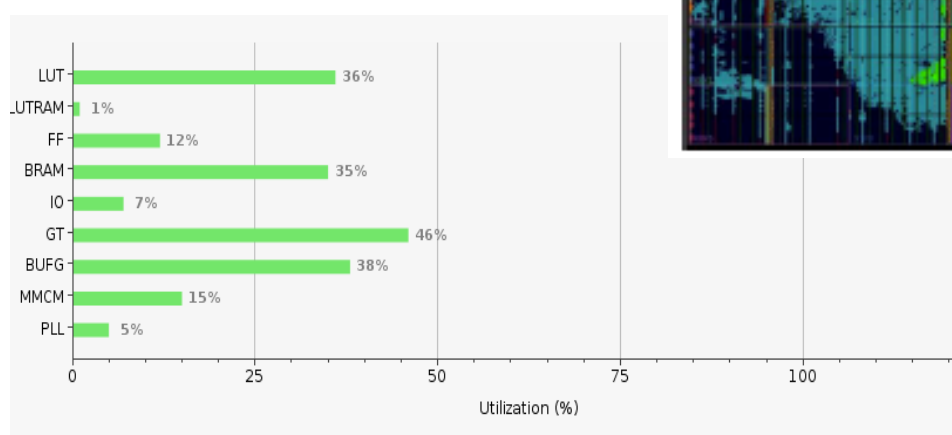


Backend electronics

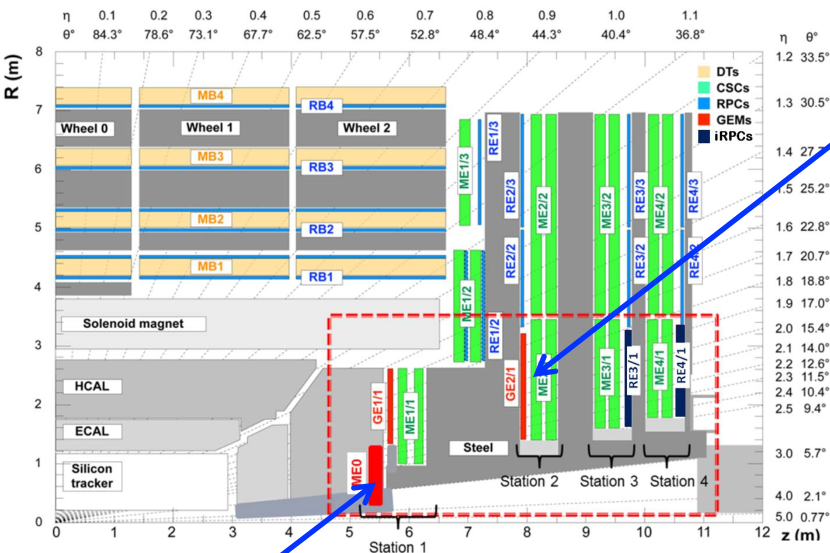
- CTP7, µTCA AMC developed for CMS Calo. Trigger
  - 1 Virtex-7 FPGA + Zynq
  - Optical links: 67 Rx + 48 Tx



- We have demonstrated that it can manage
  - 36x GBT cores (that is 12 Triple-GEM detectors)
  - + 24x 8b/10b links
  - + DAQ link to AMC13
- 1 µTCA crate to read out GE1/1

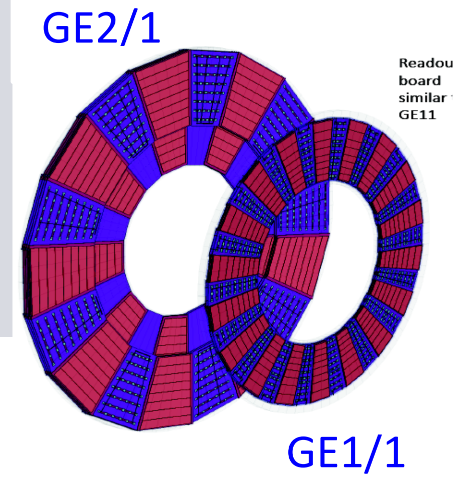


Further CMS GEM upgrades: GE2/1 & ME0



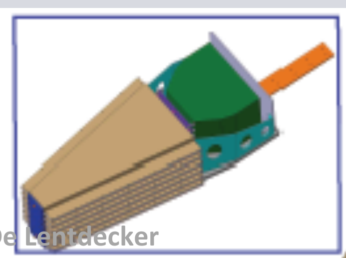
GE2/1:

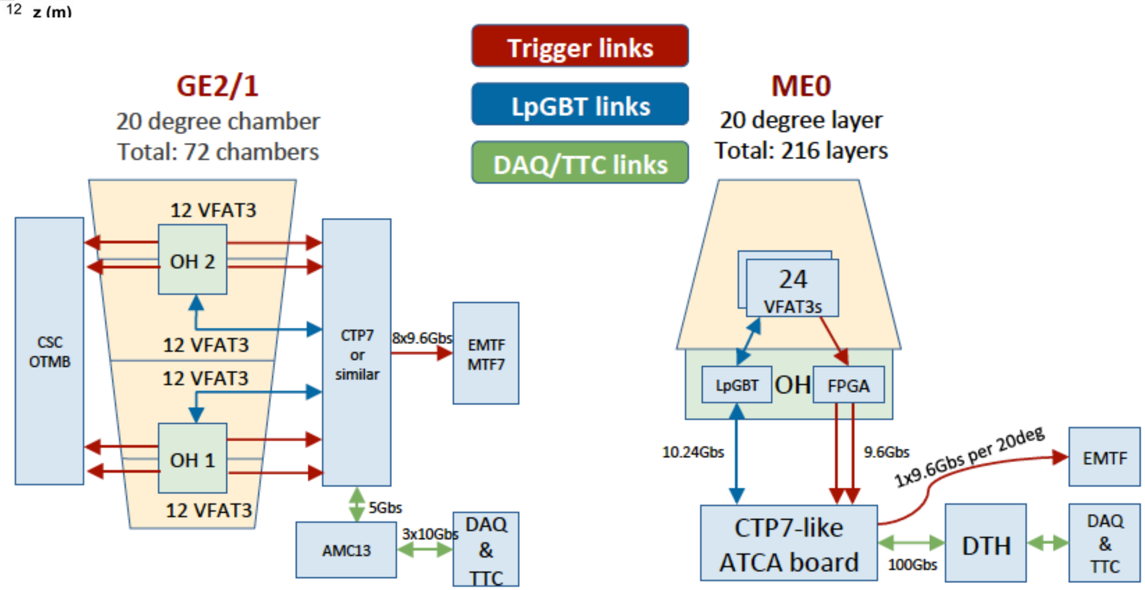
- 18 staggered super-chambers per endcap, each chamber spans 20°
- 442k channels (like GE1/1)



ME0:

- Very forward Muon tagger
- 6 layers of Triple-GEM
- each chamber spans 20°
- >650k channels





Summary

- For the first time Triple-GEM detectors are operated in CMS
  - Very nice opportunity to gain experience in installing, commissioning and operating GEM detectors inside CMS
  - Commissioning still ongoing
  - Next milestone: integration of GEM DAQ & DCS into CMS online
- Finalization of the GE11 electronics
  - VFAT3
    - Arrived end of December 2016
    - working as expected, all functionalities tested, full characterization on-going
  - Summer 2017, all electronics chain from CTP7 to VFAT3, including GEB and OH, being tested
    - Full characterization on-going

References

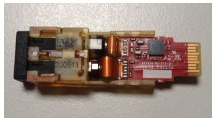
[1] ATCA® / µTCA®, https://www.picmg.org/openstandards/microtca/

AMC = Advanced Mezzanine Card

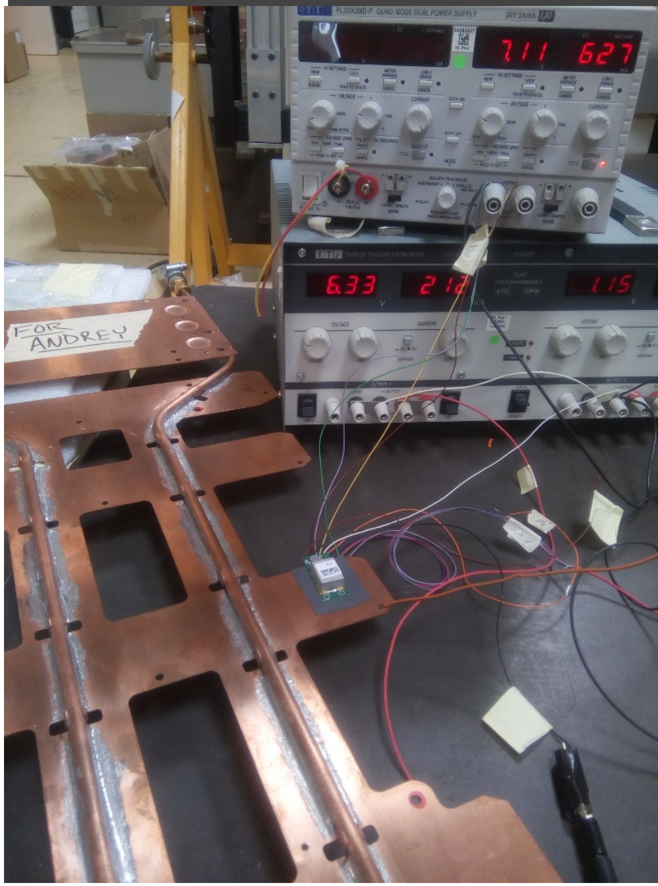
[2] The GBT-SerDes ASIC prototype, P. Moreira et al., 2010 JINST 5 C11022, https://espace.cern.ch/GBT-Project/default.aspx

[3] FEAST : ASIC DCDC converters: http://project-dcdc.web.cern.ch/project-dcdc/public/ASICDatasheet.html

[4] VTRx / VTTx: The Versatile Transceiver: towards production readiness, C. Soos, 2013 JINST 8 C03004, https://espace.cern.ch/project-versatile-link/public/default.aspx



BACKUP



	FEAST 1.0 V		FEAST 1.8 V		FEAST 2.5 V	
		Temp (C)		Temp (C)		Temp (C)
Input Voltage (V)	7.2		7.2		7.2	
Output Voltage (V)	0.995		1.8		2.499	
Output Current (A)	1	20.5	1	20.4	1	20.3
Output Current (A)	4	22.7	4	22.5	4	22.3

- To have good contact between FEAST and Cooling plate, FEASTs will be screwed to cooling plate.
- Without cooling, FEAST will shut down (max Temp.: 73 °C) !
- Note that FEAST also needs to be well connected to GEB to bring power

GEB mechanics