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IN THE CITY OF NEW YORK

The Phase-I Trigger Readout Electronics Upgrade for the ATLAS Liquid-Argon Calorimeters

TWEPP 2017

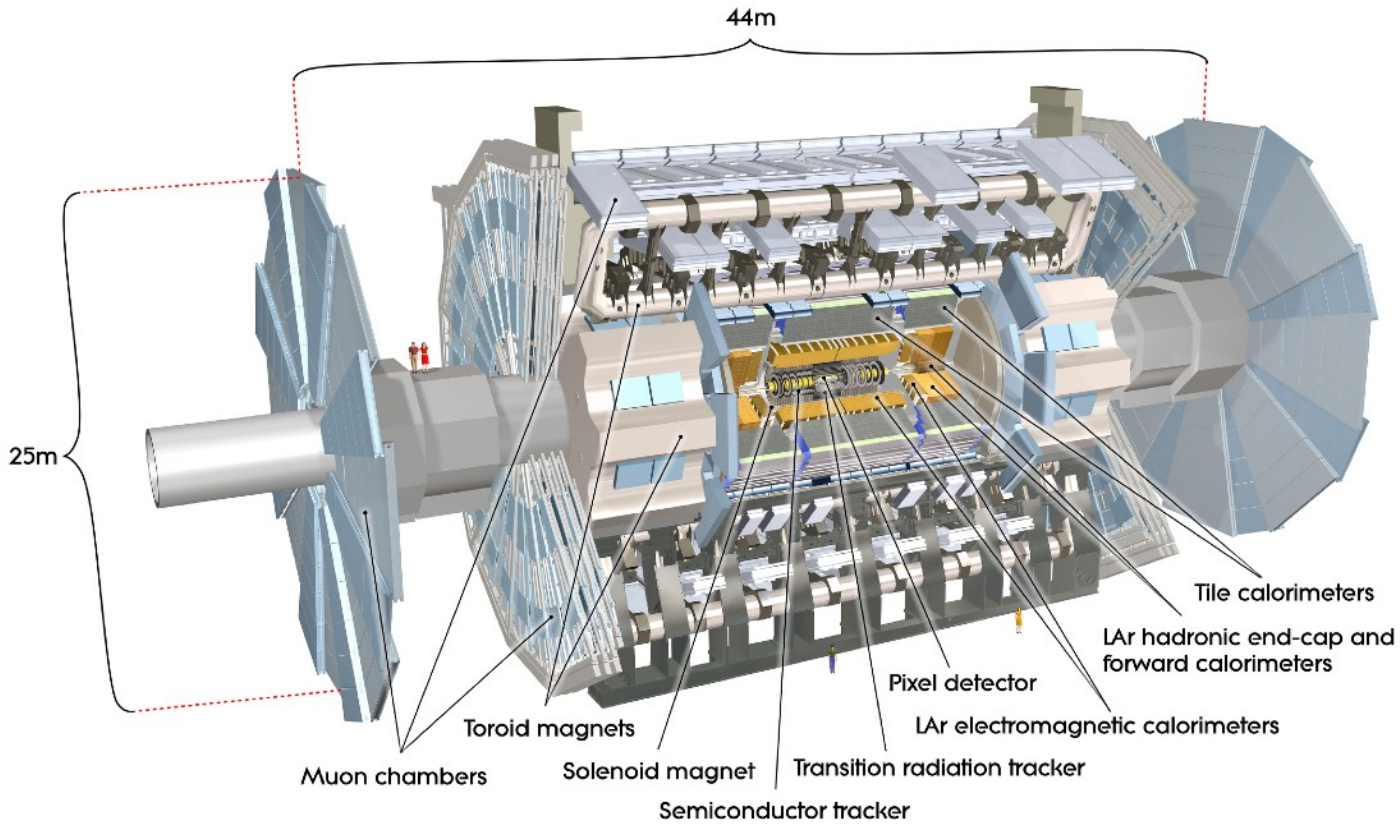
Inês Ochoa, on behalf of the ATLAS Liquid Argon Calorimeter group

Outline

- Introduction
  - The ATLAS detector
  - Liquid Argon calorimeter
  - Phase-I upgrade
- LAr Front End electronics
- LAr Back End electronics
- Demonstrator

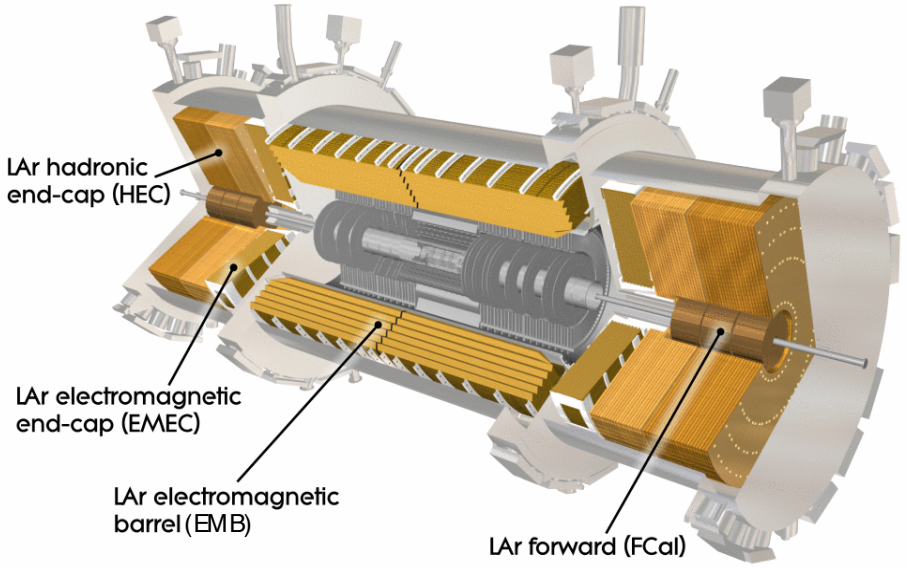
ATLAS Detector

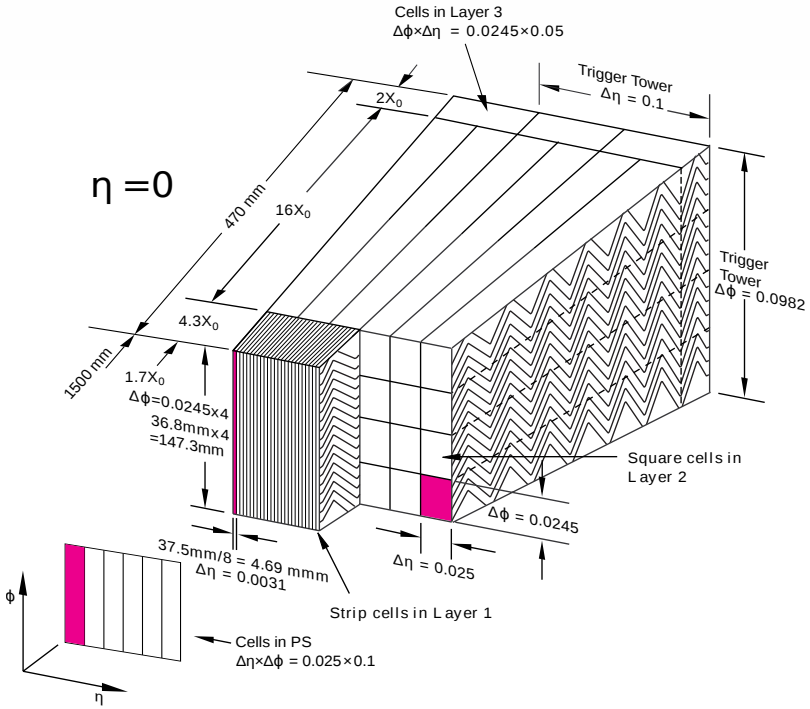
- **A Toroidal LHC ApparatuS:**
  - A multipurpose detector with cylindrical geometry and forward-backward asymmetry.
  - 44 m long, 25 m diameter and 7000 tons
- Pixel and strip detectors, electromagnetic and hadronic calorimeters, muon chambers, solenoid and toroidal magnet systems: a total of 88 M channels.



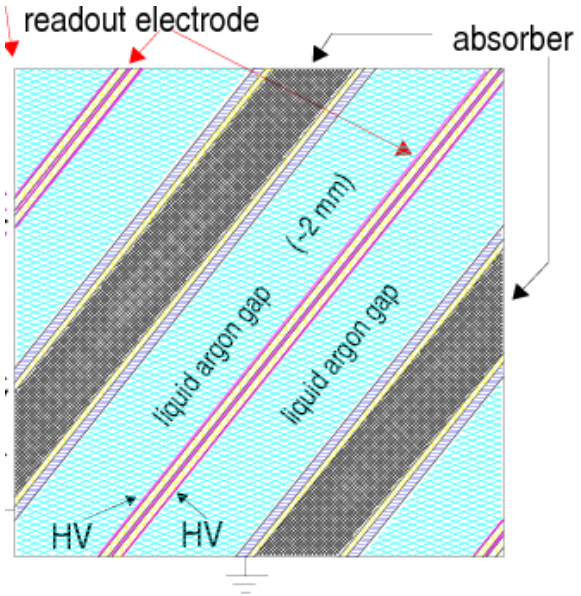
Liquid Argon Calorimeter

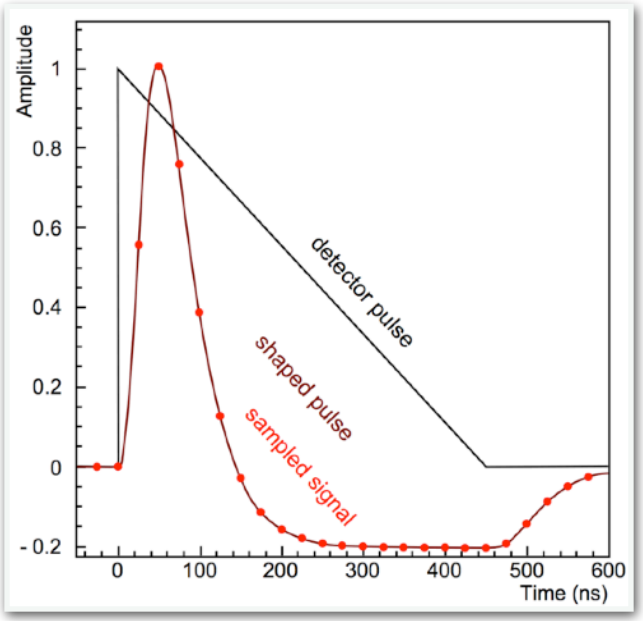
- **Main goal is to measure position and energy of photons and electrons.**
- Sampling calorimeter in accordion or rod matrix geometry:
  - Lead/copper/tungsten as absorbers
  - LAr as active medium
  - Copper-kapton electrodes
- Composed of four layers with different spatial resolutions:
  - ~180k channels for full readout
  - 3k trigger towers: groups of cells with 0.1 x 0.1 in (η,Φ)
- Total radiation length: 22 X_0





LAr ionisation pulse





- **Principle of operation:**
  - Incoming particle creates an electromagnetic shower which ionizes liquid argon.
  - Resulting current is collected by readout electrodes.
  - Amplification + CR-RC^2 shaping of the converted voltage.
  - Sampling of the shaped pulse @ 40 MHz and digitization.
  - Transverse energy deposited in a given cell is computed and sent to DAQ.

Current LAr readout electronics

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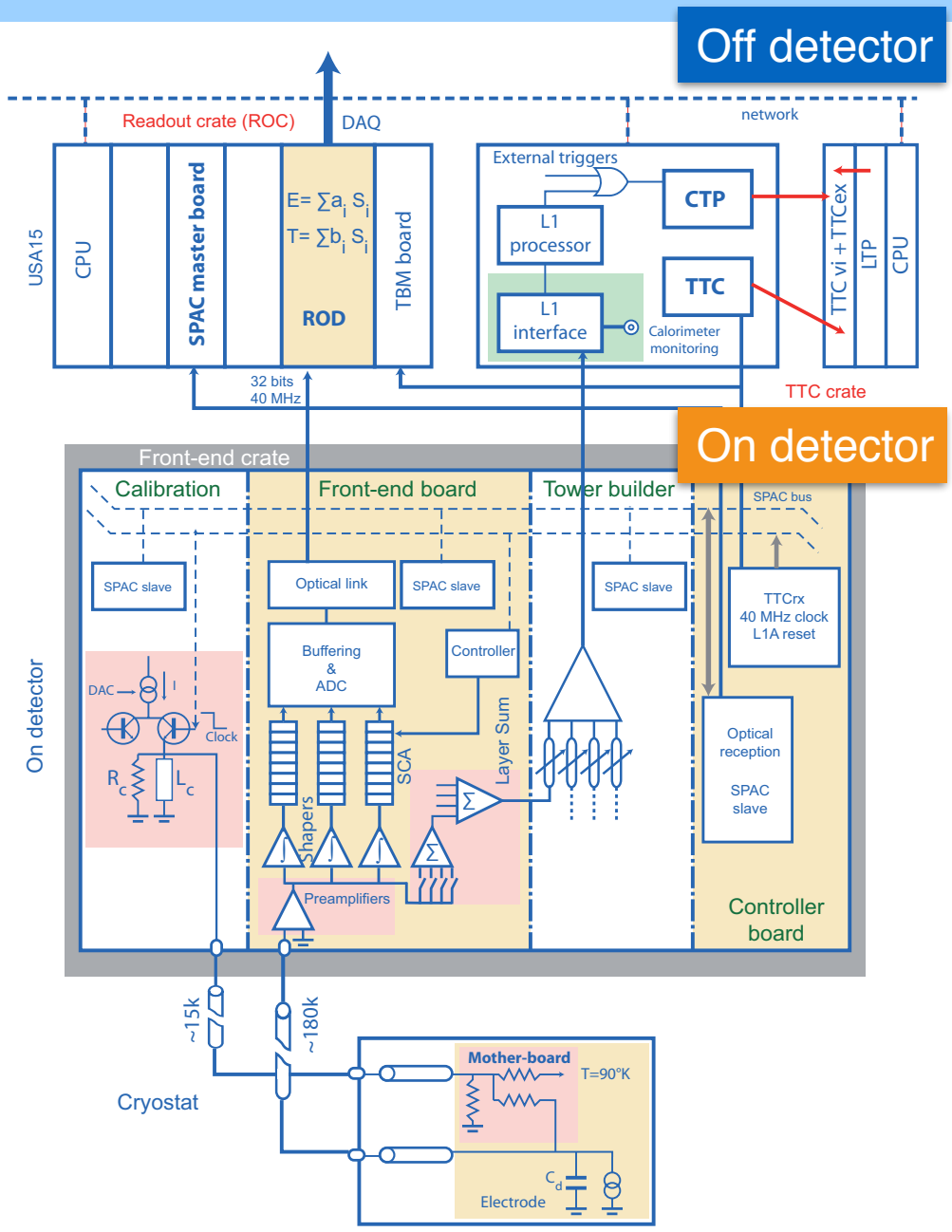
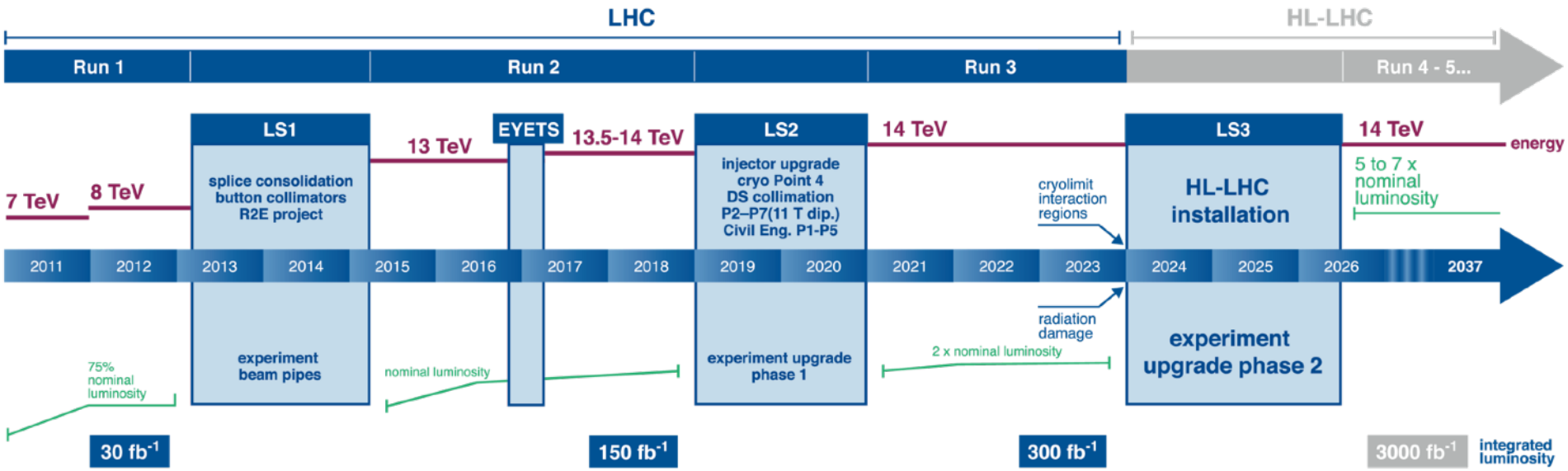
- **Regular** readout (full granularity):
  - Amplification and shaping of cell signals.
  - Buffering with analog pipeline.
  - Digitization upon L1 accept (<100 kHz)
  - Data transmission via optical link.
- **Trigger** readout:
  - Layer sum boards (LSB) sum cell energies.
  - Tower builder boards (TBB) form trigger tower analog signals, sent to L1.
- 1524 front end boards (FEB)
- 192 readout driver boards (ROD)



Upgrade Plans for LHC and ATLAS



- Run 2 (current) conditions:
  - L_{max} = 1.3 x 10^{34} cm^{-2} s^{-1}, $\langle\mu\rangle \sim 24$
- **Phase-I upgrade:** 2019-2020 (LS2)
  - L_{max} = 3 x 10^{34} cm^{-2} s^{-1}
  - $\langle\mu\rangle \sim 80$
  - Max. hardware trigger rate at 100 kHz

Upgrade trigger readout

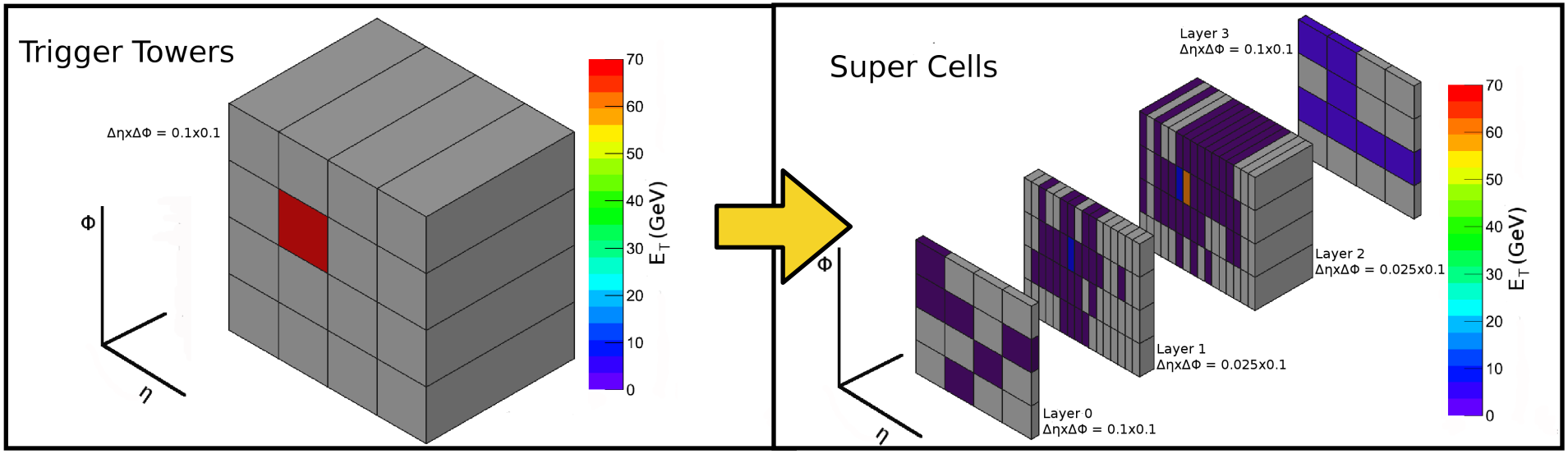
- **Phase-II upgrade:** 2024-2026 (LS3)
  - L_{max} = 7.5 x 10^{34} cm^{-2} s^{-1}
  - $\langle\mu\rangle \sim 200$
  - Max. hardware trigger rate at 1 MHz

Upgrade main readout

$\langle\mu\rangle$ = average number of interactions

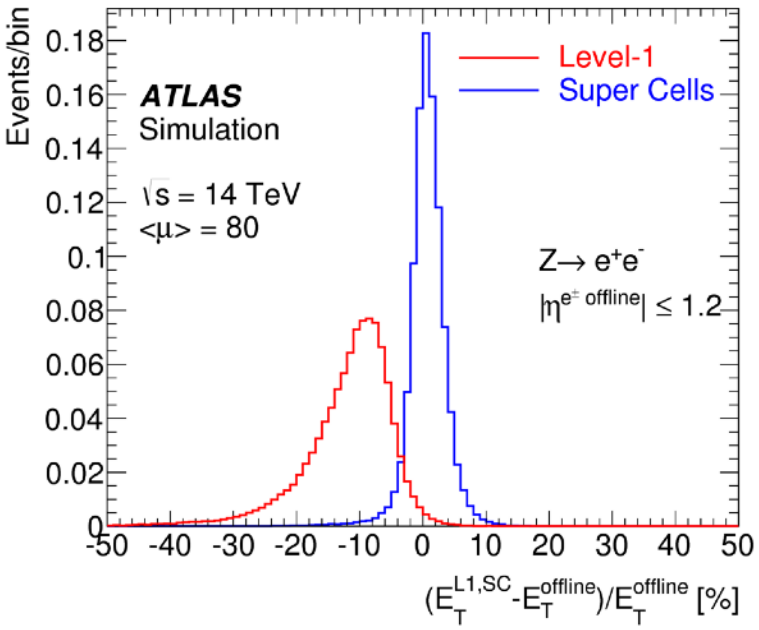
LAr Phase-I upgrade

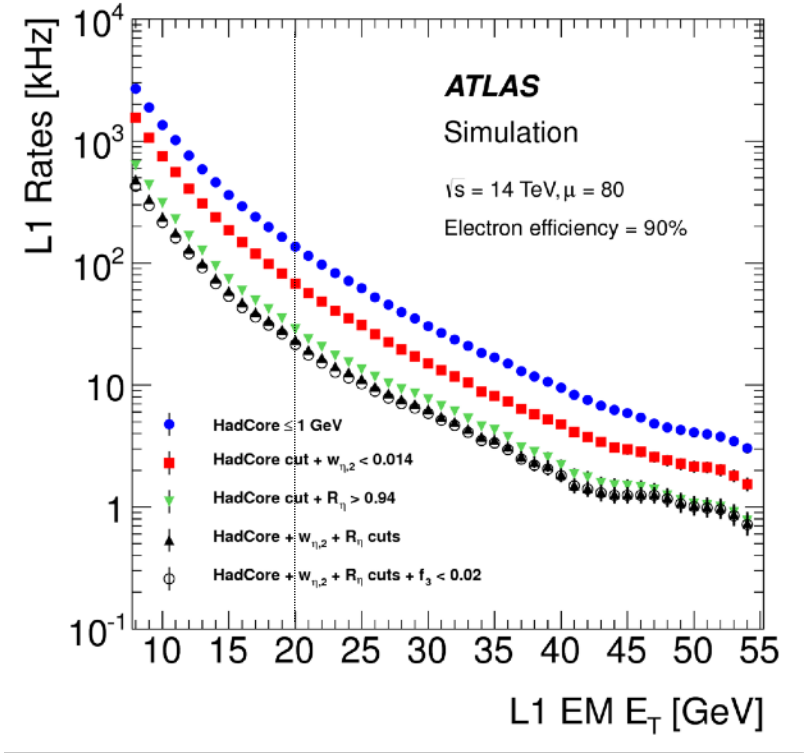
Simulation of electron with 70 GeV of transverse energy



- Taking advantage of the luminosity increase during the LHC Run 3 requires maintaining low p_T thresholds and same trigger bandwidth (100 kHz).
- **Goal:** higher granularity and higher resolution to inform L1 trigger decision.
- **Super Cells** as trigger objects:
  - Finer segmentation: 10-fold increase in granularity from longitudinal and lateral segmentation.
  - Quantization scale constant in voltage leading to slightly changing E_T-LSB vs η: ~ 180 MeV in the middle, 70 to 120 MeV in Front and Back.

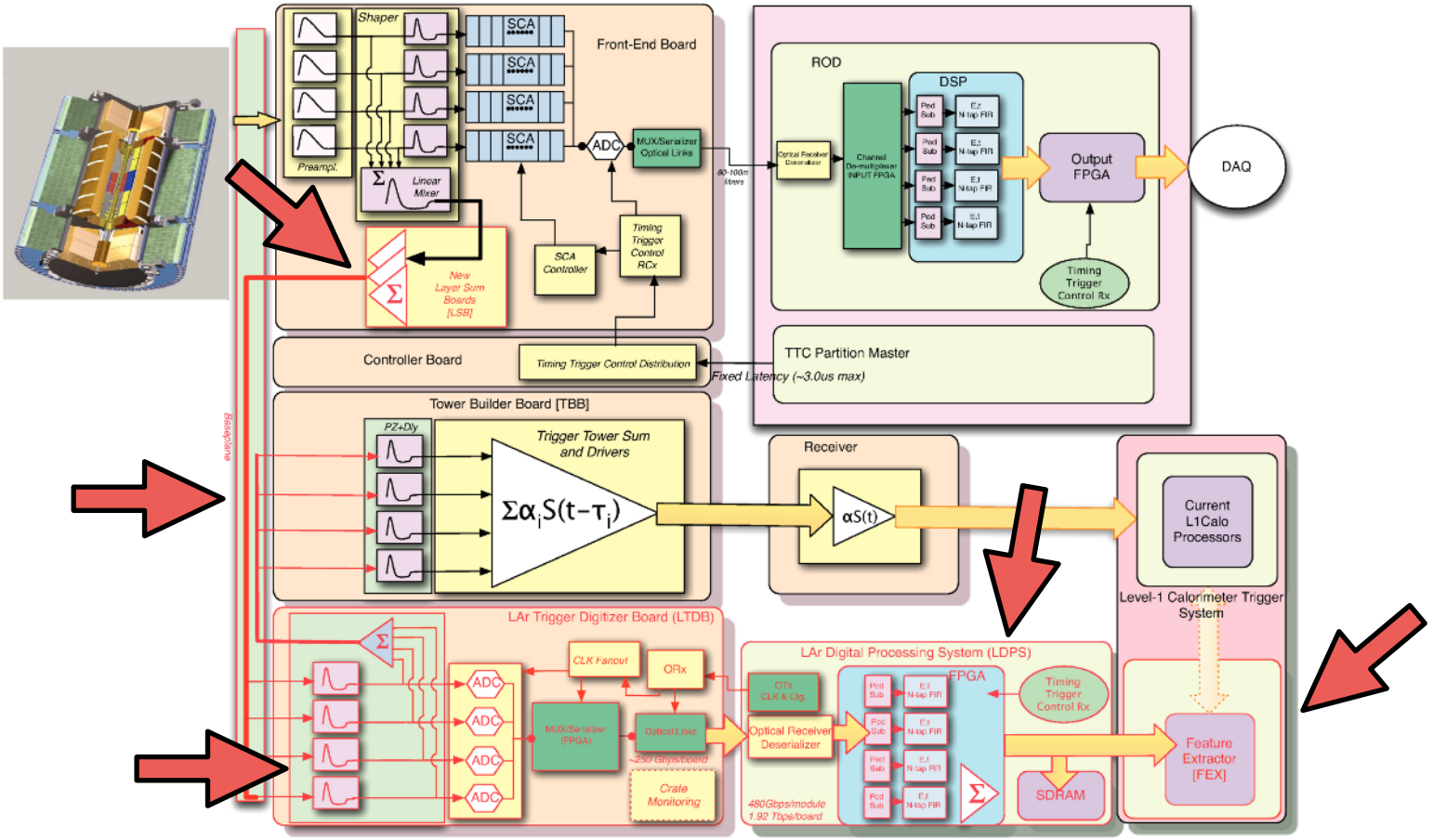
Physics case





- Information on lateral and longitudinal shower development available at L1, using higher granularity from Super Cells.
- Improved energy resolution of objects reconstructed at trigger level.
- **Reduction of L1 thresholds by 10-15 GeV compared to Run 2 (same rate).**

LAr Phase-I upgrade

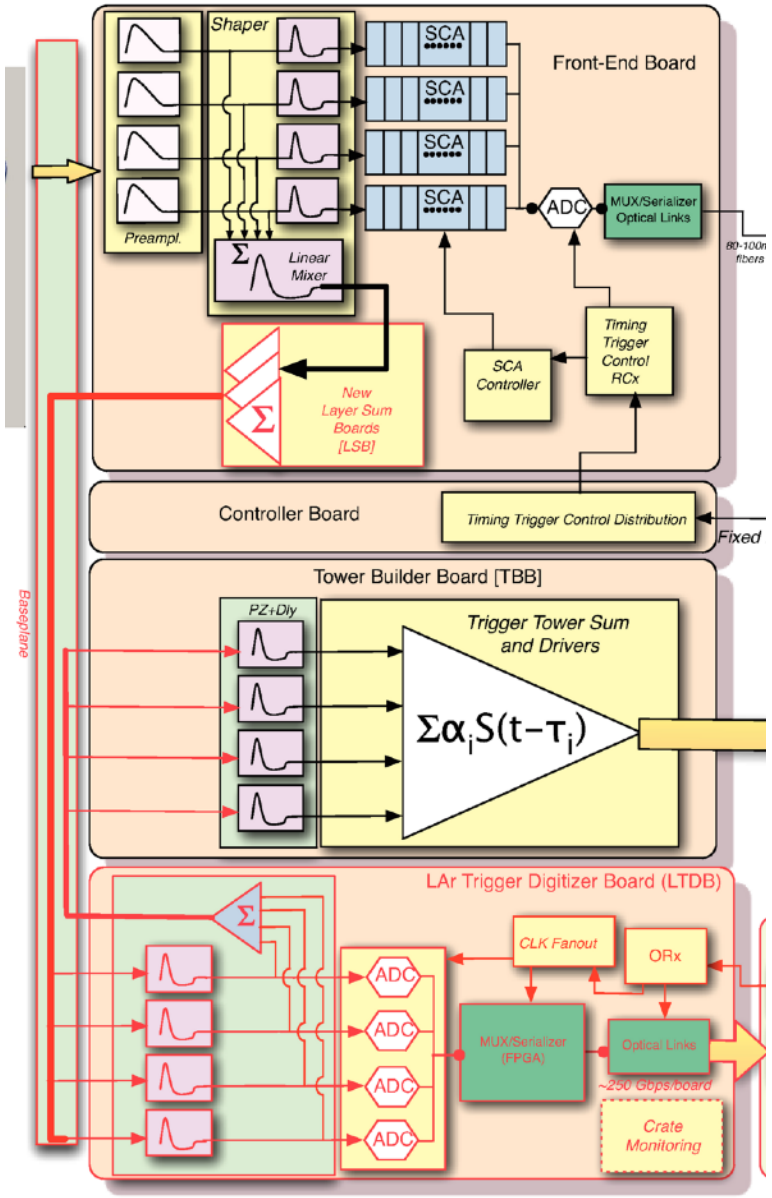


- Sample and digitize 34k Super Cell signals and convert them to E_T @ 40 MHz.
- Send ~41 Tbps to trigger system.
- Latency budget LAr + Trigger: 65 bunch crossings (BC) ≃ 1.63 μs. Estimated ≃ 58 BCs.
- Maintain compatibility with Phase-II upgrade plans.

Front End Electronics Upgrade

New FE components:

- New **Layer Sum Boards** to provide higher granularity Super Cell signals in front and middle layers.
- New **Baseplane** to route new signals (10x more connections than current one).
- **LAr Trigger Digitizer Board (LTDB)** to receive, digitize and send the SuperCell signals to the Back-End electronics using radiation tolerant custom ASICs:
  - ADC
  - Serializer (LOCx2)
  - Laser driver (LOCId)
- Analog sums also built for legacy TBB.

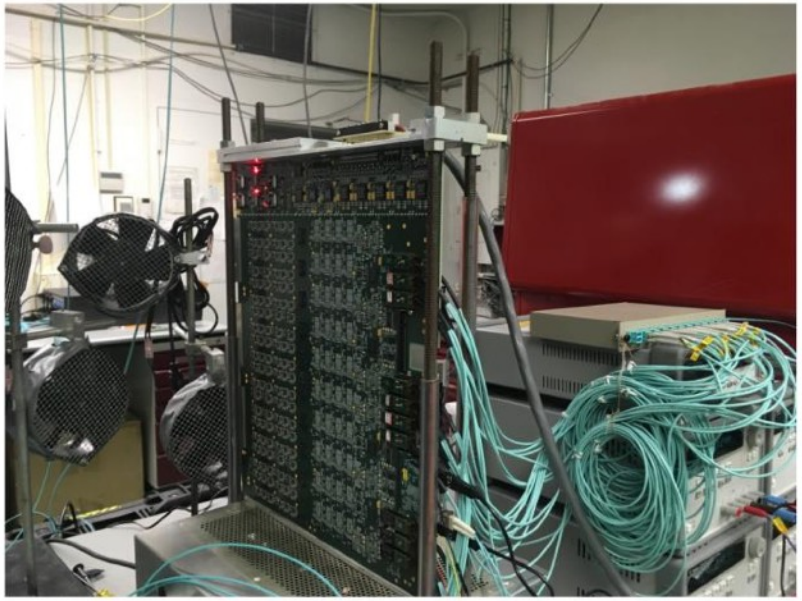


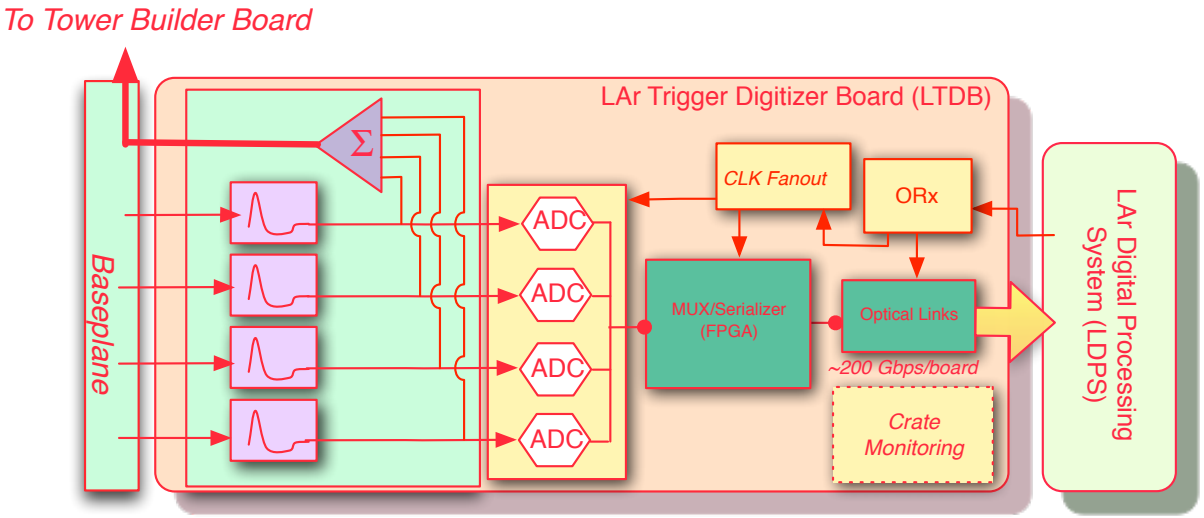
Radiation tolerance: TID 100 kRad and tested for SEE up to 3.8×10^{12} h/cm^2.

LTDB - overview

- Total of 124 LTDBs, each reading 320 Super Cells:
  - Digitization of analog signals with 12 bits @ 40 MHz, with 80 custom ADCs.
  - Digital signals are transmitted using 40 optical links @ 5.12 Gbps with custom ASICs (LOCx2 + LOCId).
  - 5 GBTx (serializer-de-serializer) links for Trigger, Timing and Control (TTC) signals.
  - Power distribution board (total consumption ~125 W).

LTDB prototype

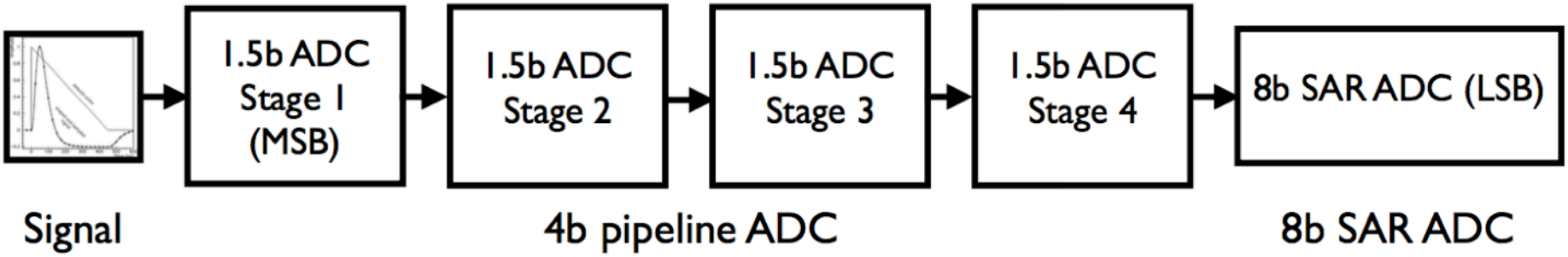




Status:

- Pre-prototype with FPGA instead of LOCx2. ✓
- Prototype with close-to-final ASICs under test. ✓

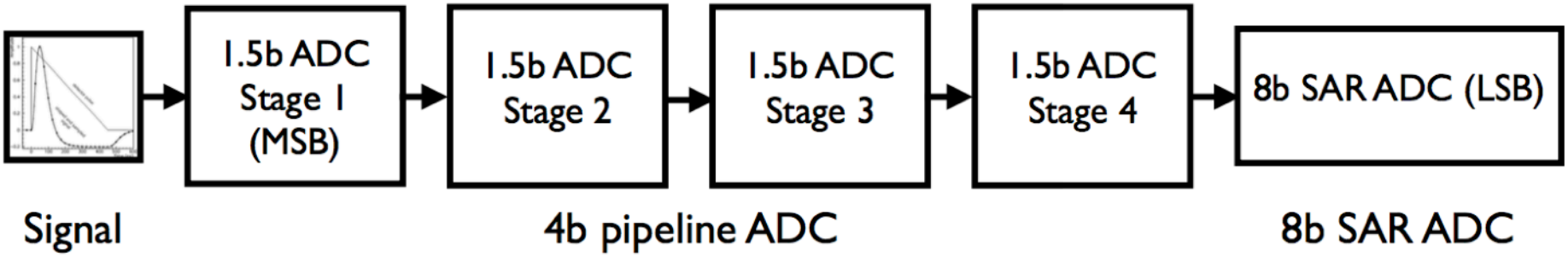
LTDB - Custom ADC



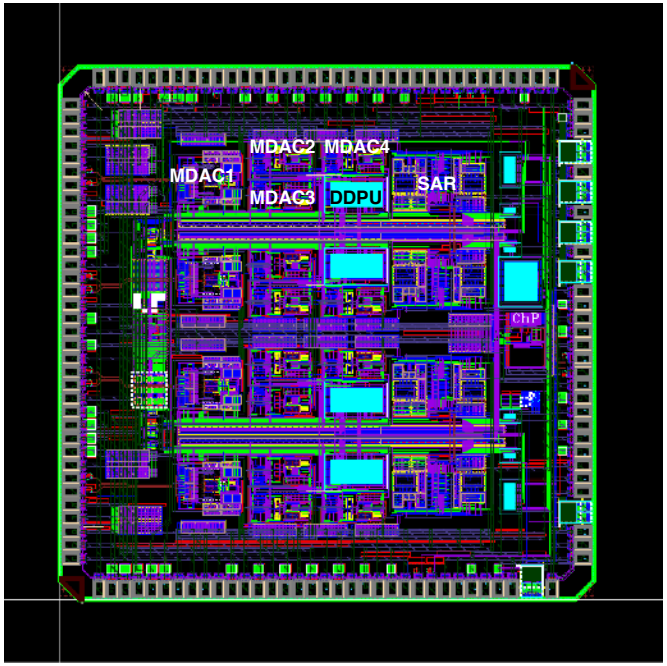
- **Requirements:**
  - Calorimeter signals continuously sampled and digitized at 40 MHz.
  - Four channels per chip.
  - ADC power must be less than 145 mW per channel.
  - Latency must be less than 200 ns.
  - Radiation-tolerant.
  - Dynamic range required of approximately 12 bits.

- **4-channel 12-bit radiation-hard ADC: NevisADC**
  - 130 nm CMOS.
  - Pipeline MDAC stages determine 4 MSB.
  - SAR ADC for lower 8 bits.
  - Sampling information from the rising edge of differential input SLVS 40MHz clock.
  - Data sent out serially using 320MHz DDR SLVS clock signaling.
  - I2C interface (1.2V signaling).

LTDB - Custom ADC



- **4-channel 12-bit radiation-hard ADC: NevisADC**
  - ENOB 11 bits
  - Dynamic range ~11.8b
  - Power dissipation < 50 mW/channel
  - ~ 100 ns latency



IBM8RF 130nm CMOS
3.6 x 3.6 mm
72 pins QFN

Status:

- 180 recently produced “Nevis15" chips to develop and validate the QA/QC procedures.

LTDB - Custom ADC - Radiation Tolerance

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- HL-LHC requirement is 100 kRad of total dose and SEE tests with a total fluency of 3.8×10^{12} h/cm^2.

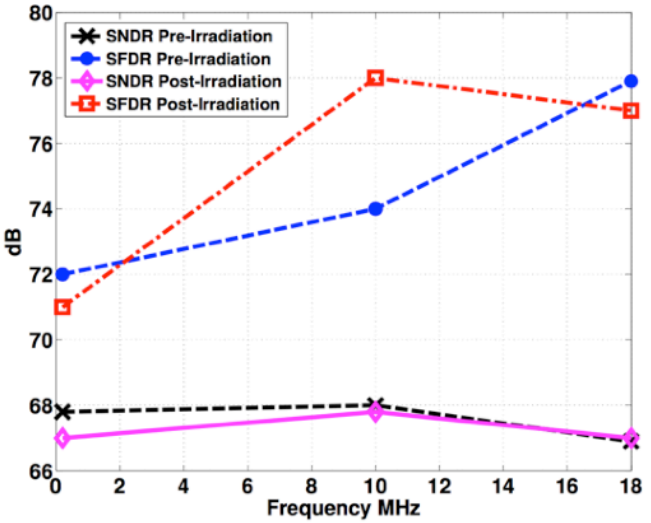
- ADC performance measured before and after irradiation in ~200 MeV proton beam.
  - **Radiation tolerance established up to 10 MRad.**

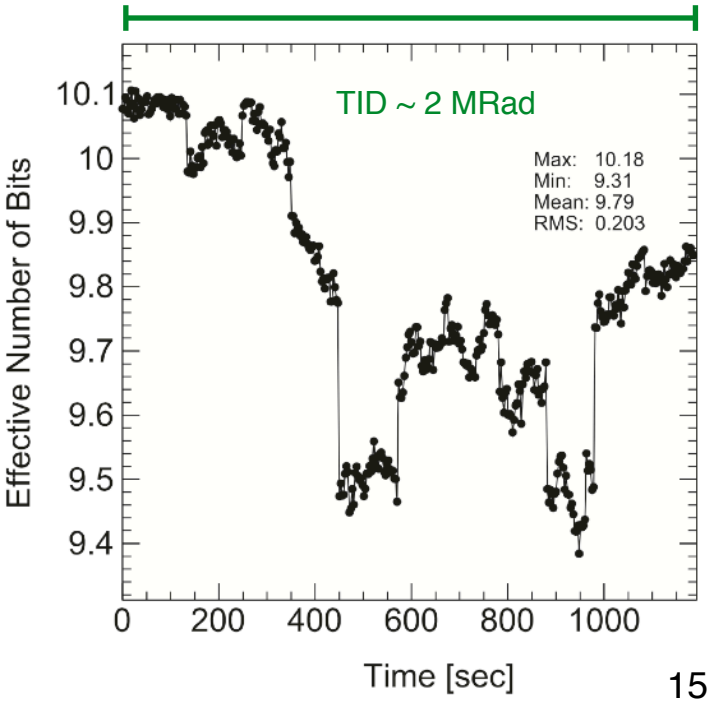
- SEE cross-sections measured as < 10^{-12} cm^2 (per channel).
  - Over 30k channels and 10 h fills (2 fb^{-1} each), expect 10 SEE events/fill and 1 SEFI/fill requiring reset.

Chip No.	Rate [10^8proton/cm^2/s]	Dose [kRad]	SEFI	SEU (analog)	SEU (digital)	SEE	Cross section (w/analog errors) [10^{-12} cm^2]
3	19.0	101	0	8	1	12	0.6 (5.1 ± 1.8)
3	76.0	283	0	41	2	43	0.6 (9.8 ± 1.5)
4	18.6	203	1	10	0	11	0.3 (3.5 ± 1.1)

SEE

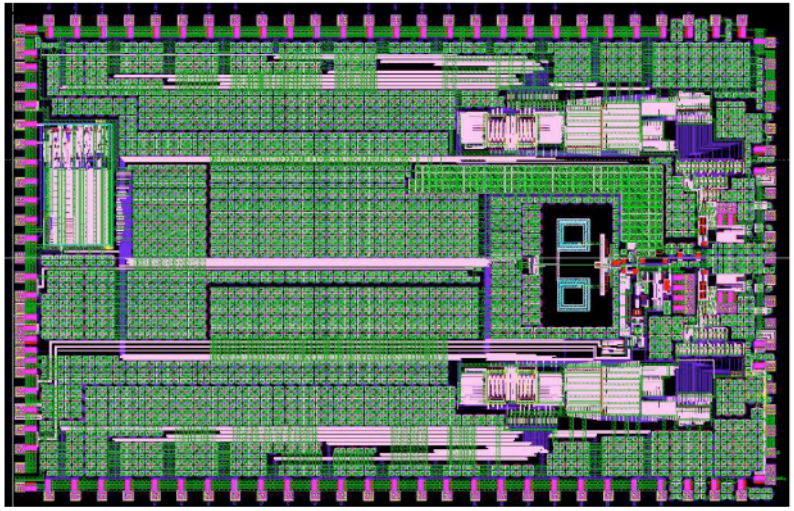
TOTAL DOSE





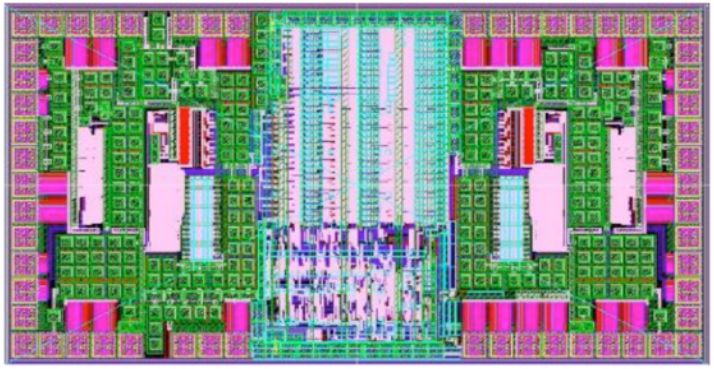
LTDB - Optical Links

- **Serializer: LOCx2**
  - 250 nm Silicon-on-Sapphire
  - Dual-channel 8 x 14 bits
  - Output at 5.12 Gbps
  - Power consumption: 1 W
  - Latency < 75 ns



6.036 x 3.68 mm
100 pins QFN

- **Driver: LOCId**
  - Dual channel VCSEL driver
  - Same technology as LOCx2



2.114 x 1.090 mm
40 pins QFN

Status:

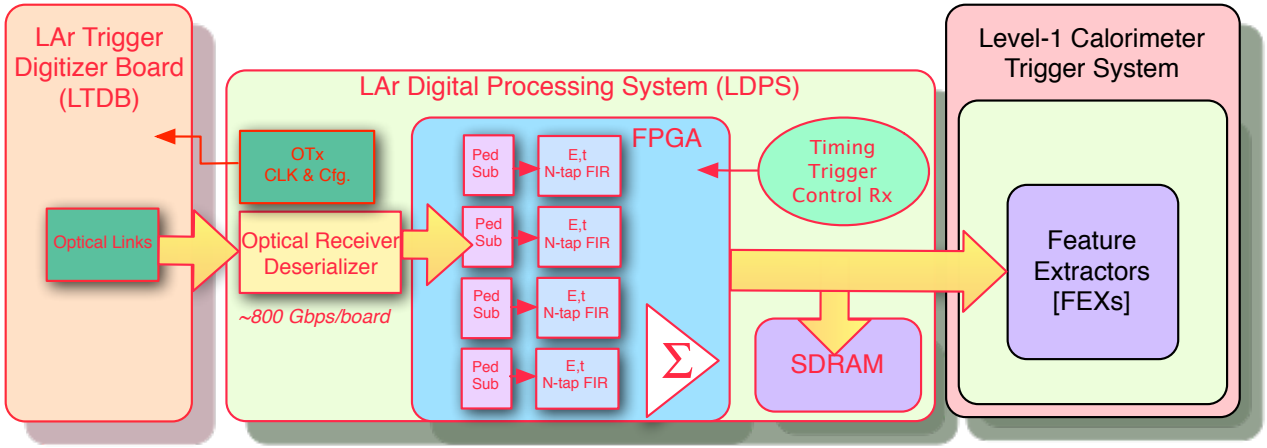
- Wafers of LOCx2 and LOCId produced and under test on LTDB prototype. ✓
- Both ASICs radiation tolerant: no change in the output eye diagram has been observed after ~200 kRad TID. ✓

Back End Electronics Upgrade

- The LAr Digital Processing System (LDPS) receives the 12-bit data from the LTDBs, calculates the transverse energy of each Super Cell and sends the result every 25 ns to the L1 trigger system.
- Configures and monitors LTDBs, providing TTC signals.

Main component: LAr Digital Processing Blade (LDPB)

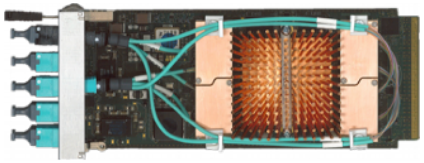
- 31 LDPBs to read 124 LTDBs:
  - 192 input fibres @ 5.12 Gbps and 192 output fibres @ 11.2 Gbps.
  - ~ 25 Tbps input from Super Cells and ~ 41 Tbps output to L1.

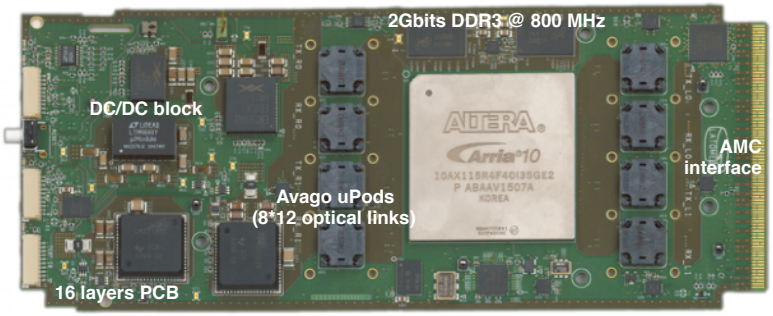


- One carrier board with four Advanced Mezzanine Cards (AMC) and a Rear Transition Module (RTM).

LATOME: LAr Trigger prOcessing MEzzanine

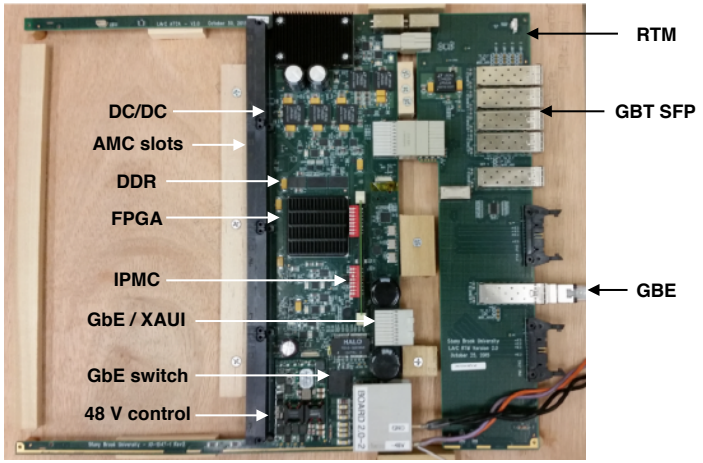
- Main data flow: E_T computed using optimal filtering for Super Cells and trigger towers. BCID assignment and transmission to L1 trigger.
- Monitors data and sends report to TDAQ system upon request.
- ARRIA-10 (Altera) FPGA.





LArC: LAr Carrier

- Monitors data through RTM and ATCA, with 10/40 GbE, GBT and TTC. Transmission to DAQ for events accepted by the L1 trigger.
- Virtex7 (Xilinx) FPGA.

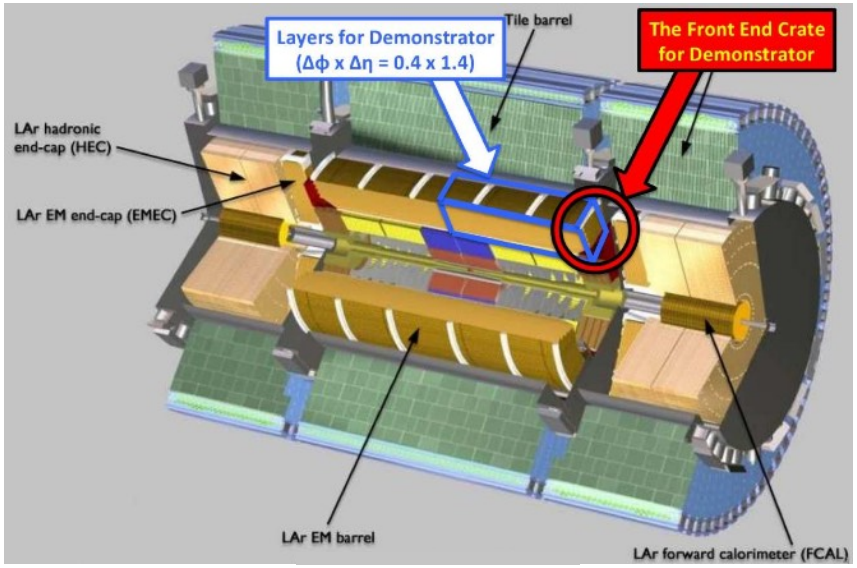


- **Status:** prototypes have been tested and integrated. Validated features include optical links up to 11.2 Gbps, 1 GbE and GBT interfaces.

Demonstrator System

- A demonstrator system for proof of principle and experience gain for the Phase-I upgrade:
  - Installed in one crate (1/32 barrel region) in the summer of 2014.
  - Reads Super Cells data for optimization and validation of energy reconstruction and BCID.

- **Front-end:** 2 LTDBs
  - Commercial 12-bit ADC (TI ADS5272), not radiation-hard.
  - Multiplexing 8 Super Cells on one 4.8 Gbps optical link.
- **Back-end:** 3 ATCA test boards for baseline acquisition (ABBA) at BE.
  - ATCA boards with 3 Altera FPGAs (Stratix IV).
  - Data readout using IPbus protocol over UDP on 10 GbE network.

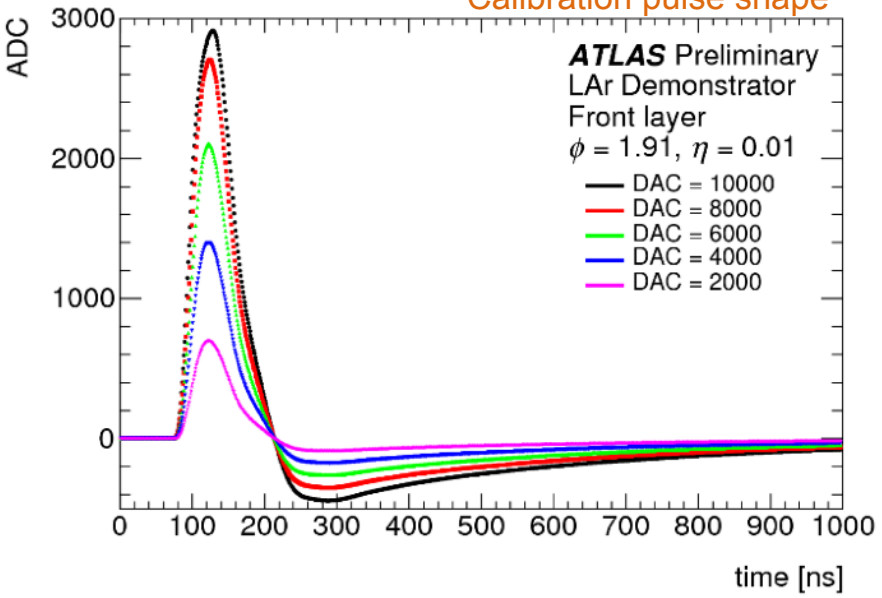


- **Status:** taking LHC collision data since the start of Run 2.

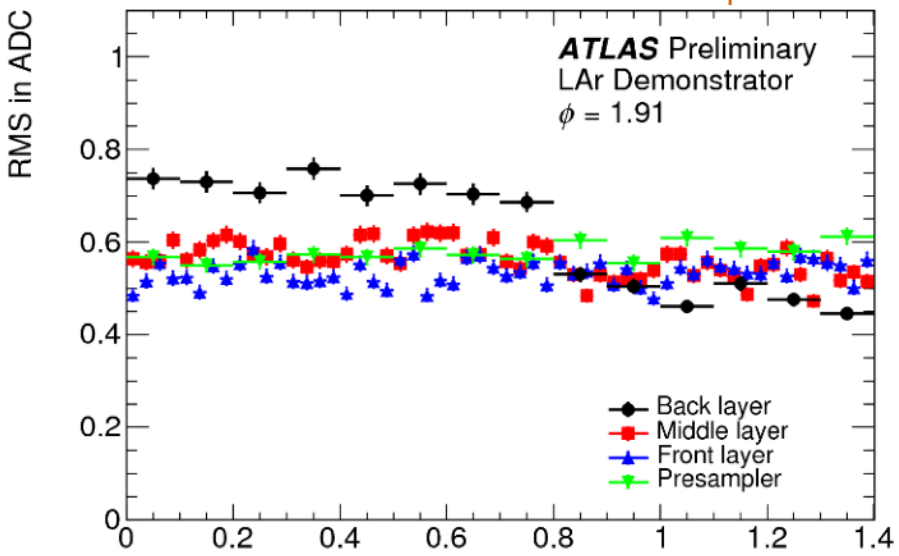
Demonstrator System

- **Calibration:**
  - Pulses injected at different amplitudes by calibration board.
  - Good linearity observed.
- **Collisions:**
  - Successful data taking in 2015, 2016 and 2017, for data triggered in demonstrator acceptance region.
- Comparison to main ATLAS Readout data:
  - Noise levels below 1 ADC count.
  - Consistent with neighboring crates.
  - Good agreement between readouts.
- **Plan:** replace with LTDB and LDPB final prototypes in early 2018.

Calibration pulse shape



Noise levels of Super Cells



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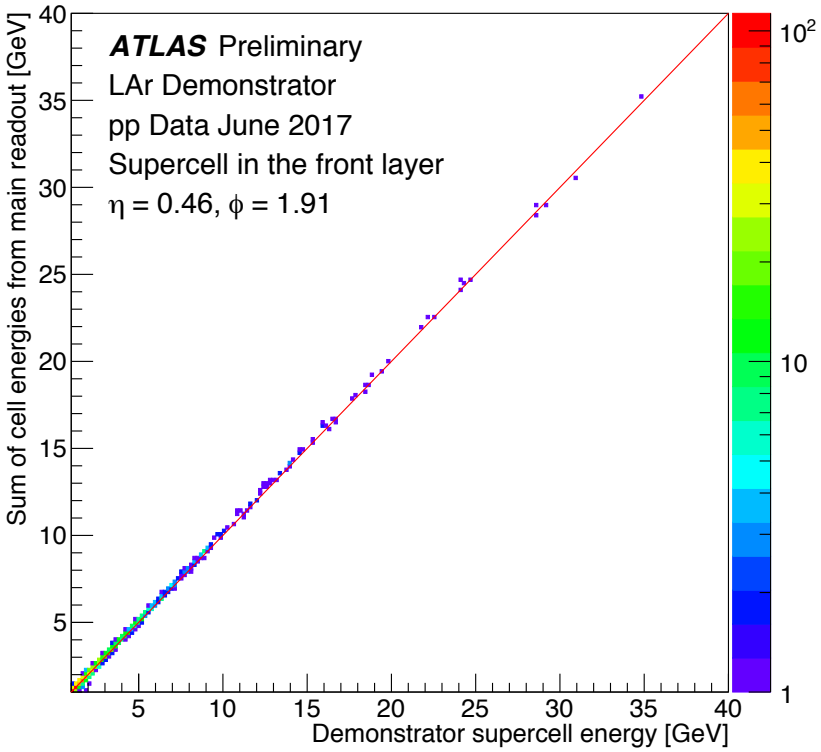
Correlation of energy measurements for each layer

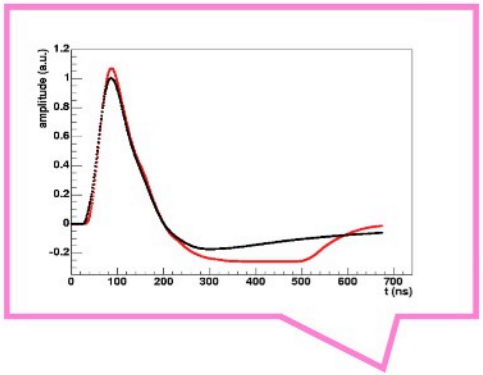


Summary

- The **ATLAS Liquid Argon calorimeter electronics** will be upgraded during the Long Shutdown 2 (2019-2020).
- The **trigger path** will be digitized at the front end level with increased granularity.
- New **LTDB** (front end) and **LPDS** (back end) systems have been developed:
  - Digitization and readout at 40 MHz.
  - Radiation tolerant ADC and optical links have been specifically designed.
  - Total data output rate to trigger system ~ 40 Tbps.
  - Production will start in 2018.
- A **demonstrator system** has been installed and successfully run in 2015, 2016 and is currently taking 2017 data.
- The Phase-I upgrade is a stepping stone towards the full readout upgrade during the Long Shutdown 3 (Phase-II).

Backup

Energy reconstruction



$$E_{\text{cell}} = F_{\mu\text{A}\to\text{MeV}} \cdot F_{DAC\to\mu\text{A}} \cdot \frac{1}{\frac{M_{\text{phys}}}{M_{\text{cali}}}} \sum_{i=1}^{M_{\text{ramps}}} R_i \left[\sum_{j=1}^{N_{\text{samples}}} a_j \left(s_j - p \right) \right]^i$$

Cell energy

Sampling fraction

Calibration board

ADC to DAC (Ramps)

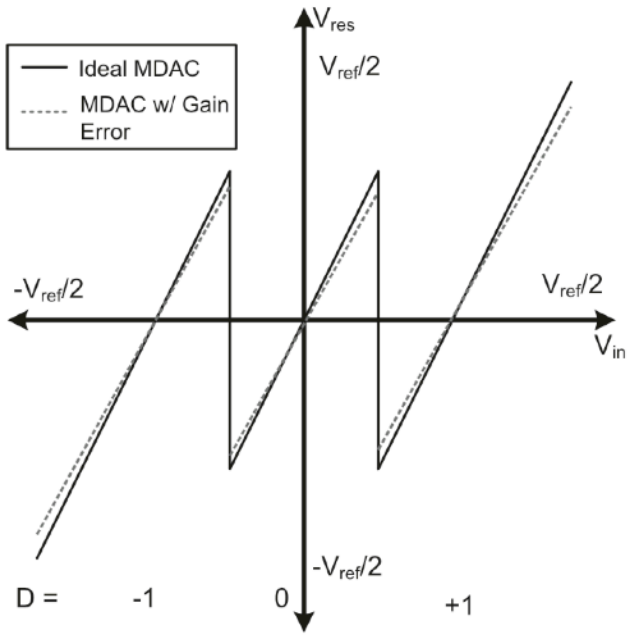
Pulse Samples

Optimal Filtering Coefficients

Pedestals

Nevis ADC: calibration

$$V_{\text{out}} = 2V_{\text{in}} - DV_{\text{ref}}$$



- The gain of each pipeline ADC stage is nominally 2.
- Gain errors due to capacitor mismatch give rise to code jumps in the output.
  - If the gain is greater than 2, the output voltage of a given stage would be greater than input voltage to following stage, resulting in missing codes.
- The calibration procedure measures the actual gain and corrects for it.
- Calibration constants are computed outside the chip and then stored in a triple-redundant buffer.
- Results in reduced dynamic range: 11.85b (~3700 counts) instead of 12b (4096 counts).

Nucl.Instrum.Meth. A855 (2017) 38-46

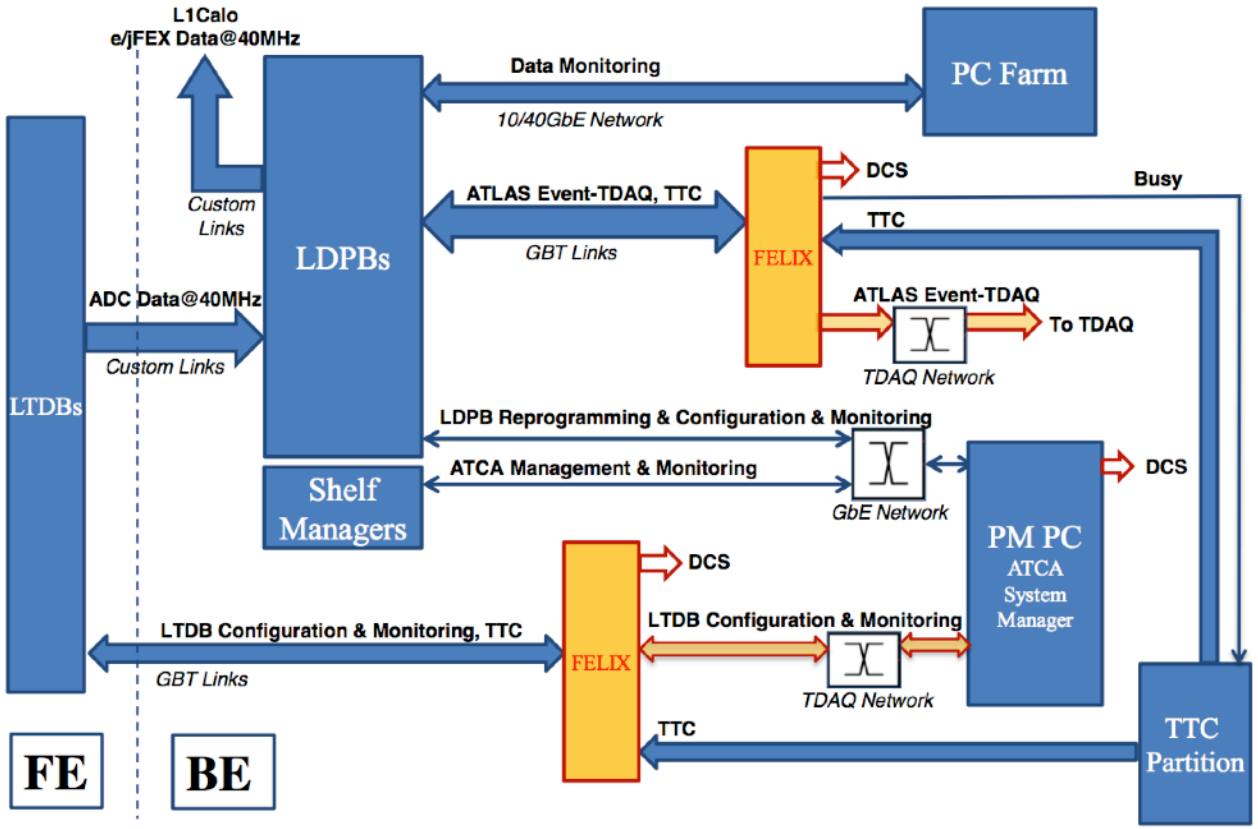


Figure 49. Schematic overview of the LDPS system. The physical elements are represented in boxes: LDPB, Shelf manager, Partition Master (PM), TTC partition, PC farm in blue and FELIX [31, 32], which is under TDAQ responsibility [4], in yellow. The links and networks are represented as arrows. The description of the data is written above the arrow and the type of link in italic below the arrows. See text for details.

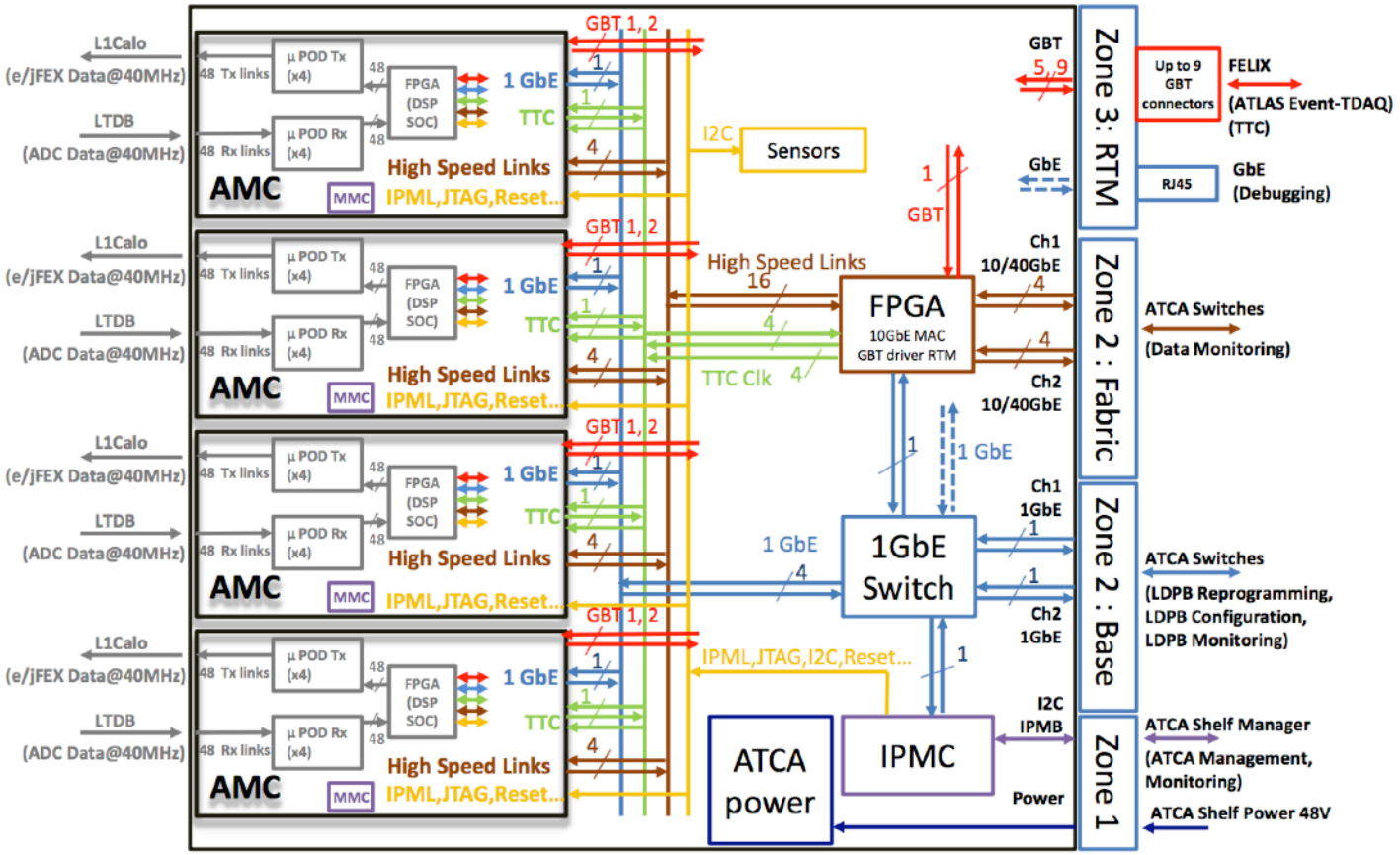


Figure 53. Schematic diagram of the implementation of the LDPB in which four Advanced Mezzanine Cards (AMCs) are mounted on a carrier board. The various line colors represent different communication functionalities: FPGA programming through GbE (light blue), monitoring data through high speed links and 10/40 GbE (brown), distribution of trigger, timing, and control (TTC) information (green), ATCA management and JTAG (orange) and data to ATLAS Events with GBT based links (red).

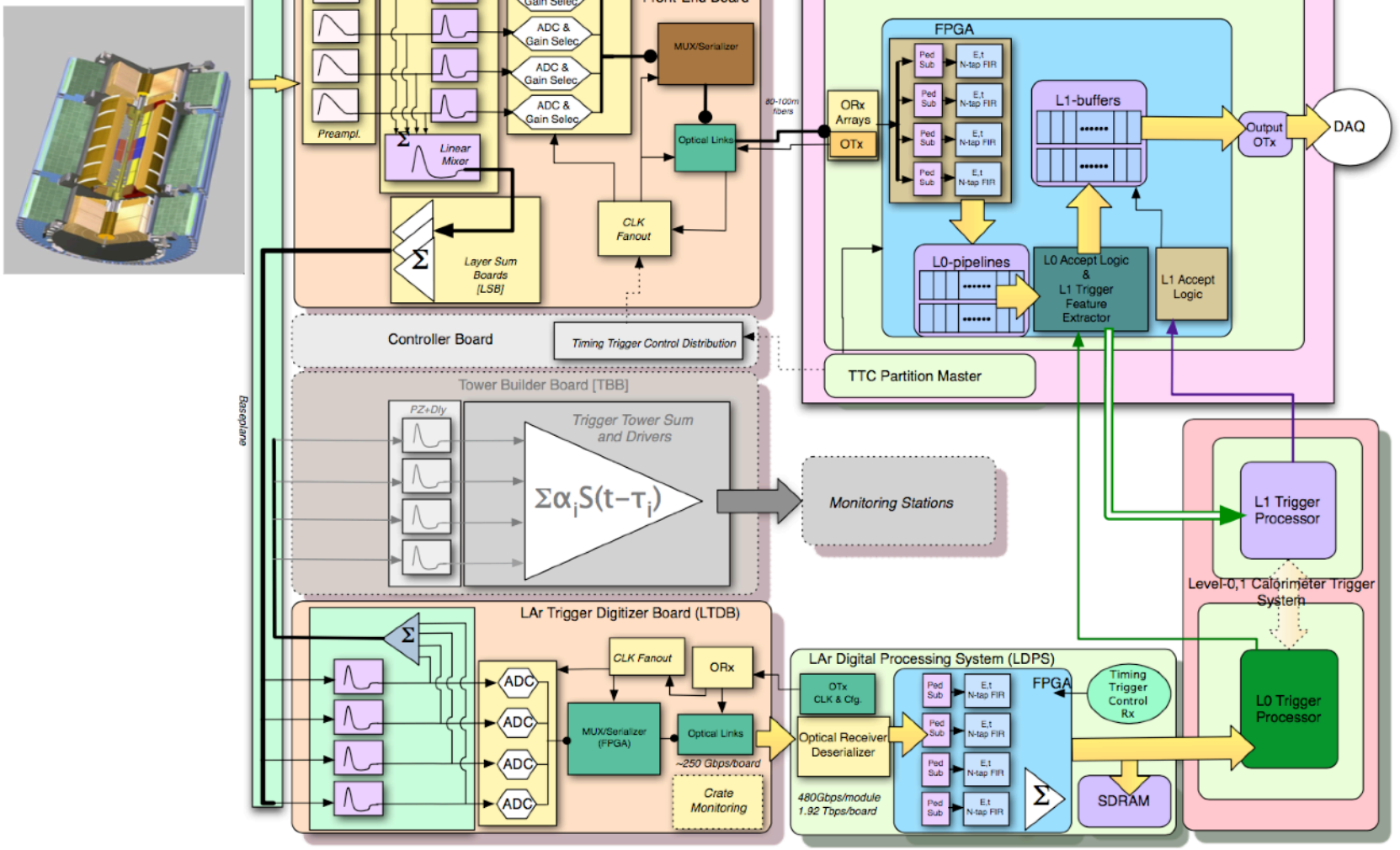


Figure 5. Schematic block diagram of the Phase-II upgrade LAr readout architecture. The "legacy" trigger electronics (grayed out in the figure) will be decommissioned during LS3.