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The Phase-I Trigger Readout Electronics Upgrade for the ATLAS Liquid-Argon Calorimeters

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Electronics developments are pursued for the trigger readout of the ATLAS Liquid-Argon Calorimeter towards the Phase-I upgrade scheduled in the LHC shut-down period of 2019-2020. The LAr Trigger Digitizer system will digitize 34000 channels at a 40 MHz sampling with 12 bit precision after the bipolar shaper at the front-end system, and transmit to the LAr Digital Processing system in the back-end to extract the transverse energies. Results of ASIC developments including QA and radiation hardness evaluations, and performances on prototypes will presented with the overall system design.

Summary

The upgrade of the Large Hadron Collider (LHC) scheduled for a shut-down period of 2019-2020, referred to as the Phase-I upgrade, will increase the instantaneous luminosity to about three times the design value. Since the current ATLAS trigger system does not allow sufficient increase of the trigger rate, an improvement of the trigger system is required. The Liquid Argon (LAr) Calorimeter read-out will therefore be modified to use digital trigger signals with a higher spatial granularity in order to improve the identification efficiencies of electrons, photons, tau, jets and missing energy, at high background rejection rates at the Level-1 trigger. The new trigger signals will be arranged in 34000 so-called Super Cells which achieves 5-10 times better granularity than the trigger towers currently used and allows an improved background rejection.

The readout of the trigger signals will process the signal of the Super Cells at every LHC bunch-crossing at 12-bit precision and a frequency of 40 MHz. The data will be transmitted to the back-end at 5.12 Gb/s using a custom serializer and optical converter. ASICs have been developed for ADC, serializer and transmitter for this project and PCB boards are being developed now. In the new back-end system, the received digital data will be processed with a FIR filter, optimal filtering, on a FPGA (Intel-FPGA Arria-X) to identify the bunch crossing and extract the transverse energy with a fixed latency. The results of the digital processing are transferred to the level-1 trigger system for trigger object reconstruction. The backend system is developed using the ATCA architecture. ATCA carrier blade with RTM will carries four Advanced Mezzanine Cards with the FPGA. In total, the backend system will consist from 31 carrier boards in three ATCA shelfs.

In order to verify the full functionality of the new Liquid Argon trigger readout system, a demonstrator set-up has been installed on the ATLAS detector and has been operated in parallel to the regular ATLAS data taking during the LHC Run-2. Noise level and linearity on the energy measurement have been verified to be within our requirements. We have collected data with 13 TeV proton-proton collisions during the LHC Run-2, and have observed real pulse from the detector through the demonstrator system.

The talk will give an overview of the Phase-I Upgrade of the ATLAS Liquid Argon Calorimeter readout and present the custom developed hardware including their role in real-time data processing and fast data transfer. This contribution will includes the performance of the newly developed ASICs including their radiation tolerance and quality assuarance, the performance of the prototype boards in the demonstrator system. Results of the system integration test with the final prototypes will be reported.

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