TWEPP 2017 – Topical Workshop on Electronics for Particle Physics

Integration of Intelligence and Redundancy Elements into the FPGA-Based DAQ of the COMPASS Experiment

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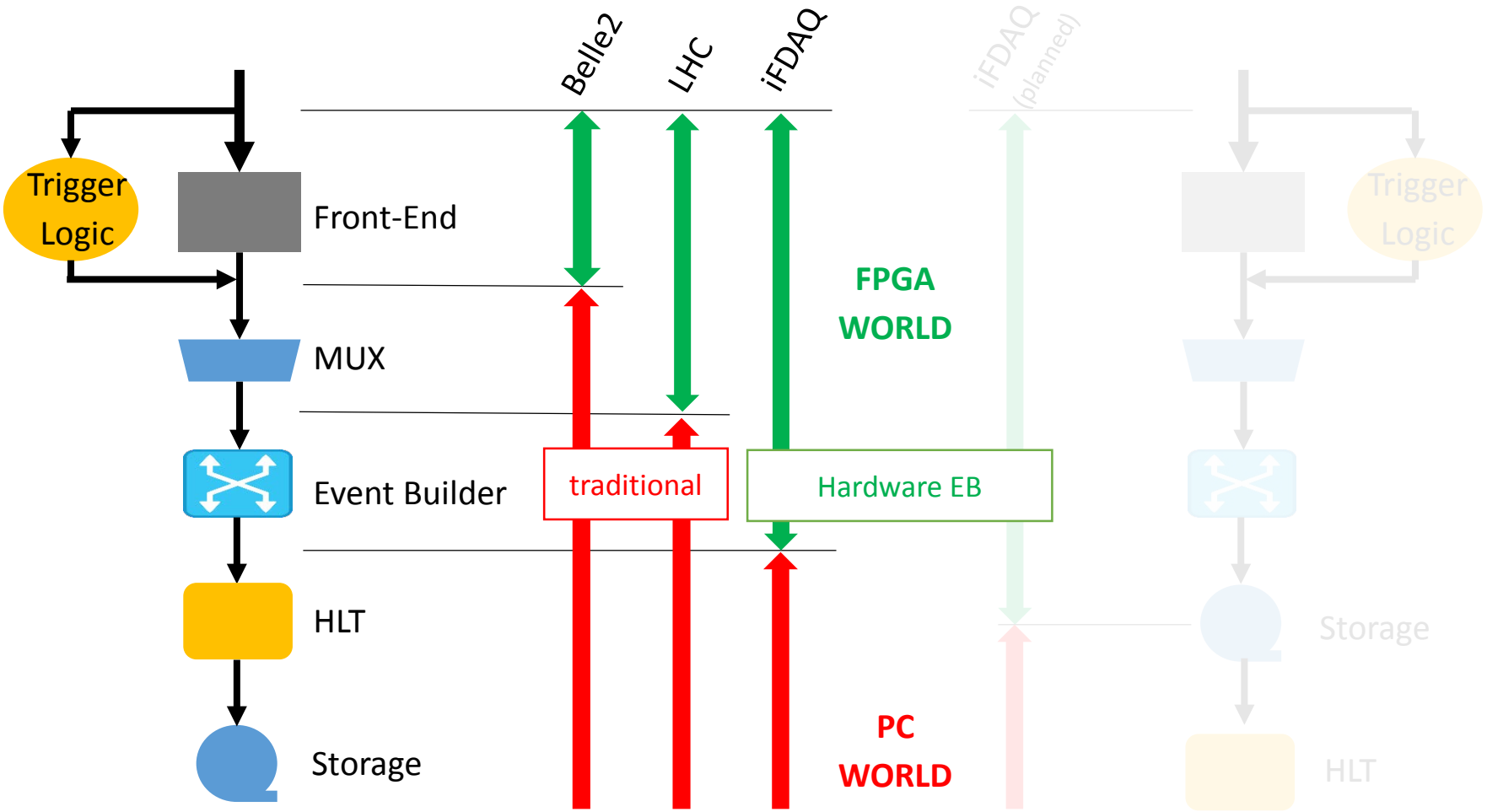
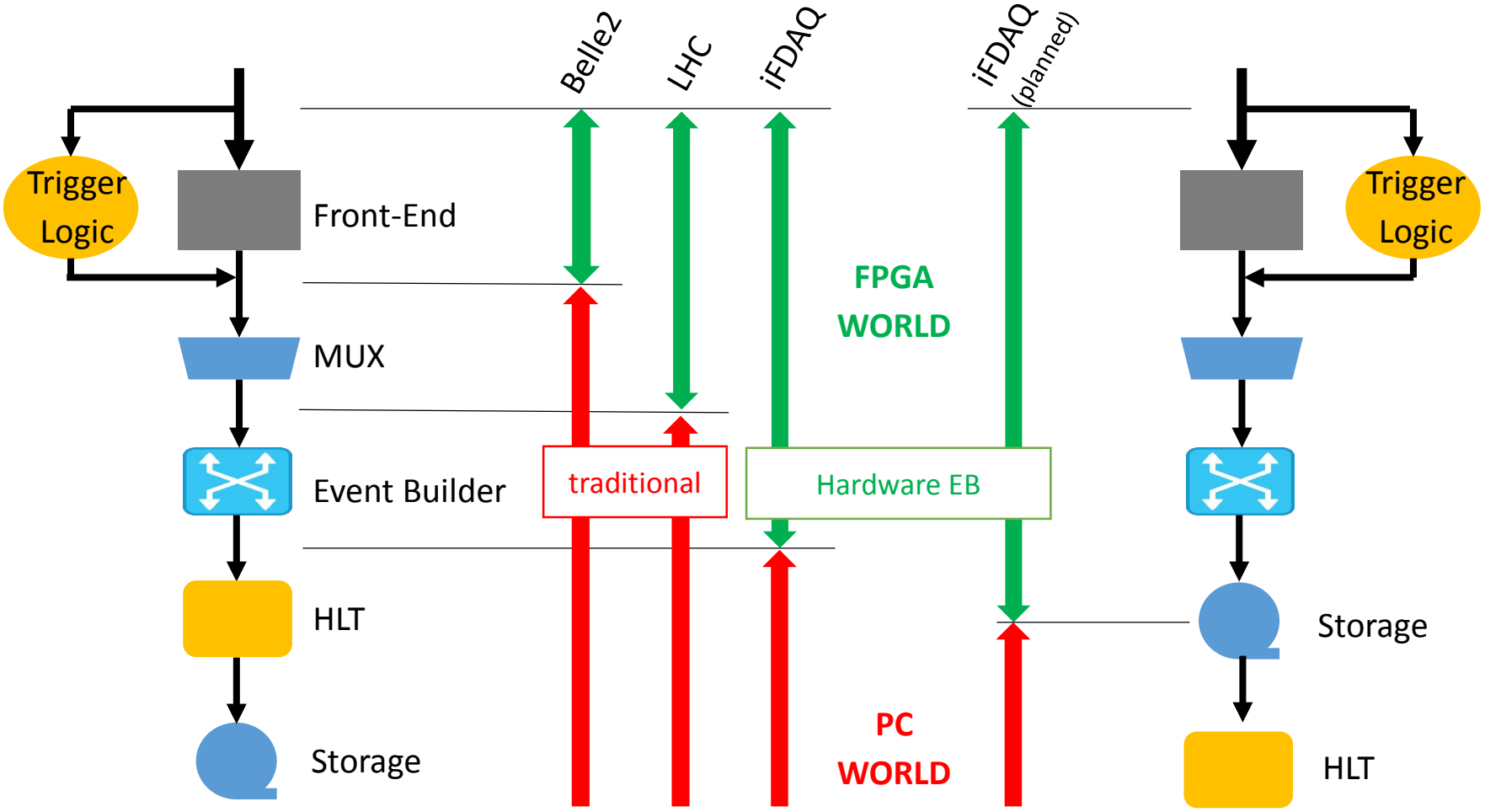
Possible DAQ Systems



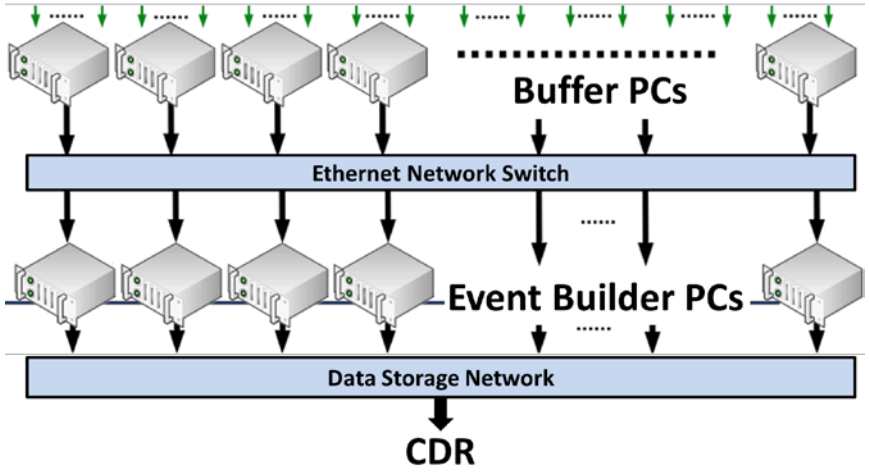
Possible DAQ Systems



Event Builder – CPU vs. FPGA

Event Building: combination of logically connected, but physically split data fragments

CPU



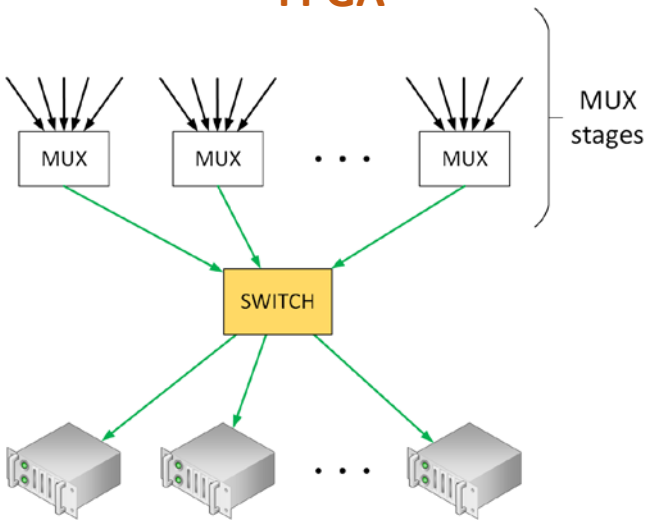
Buffer PCs:

- Buffers data until receiving control msg to forward to specific builder unit
- Replicated over number of computers to fit performance needs and application scenario

Event Builder PCs:

- Collects event fragments and combines them into complete event
- Replicated over number of computers to fit throughput requirements

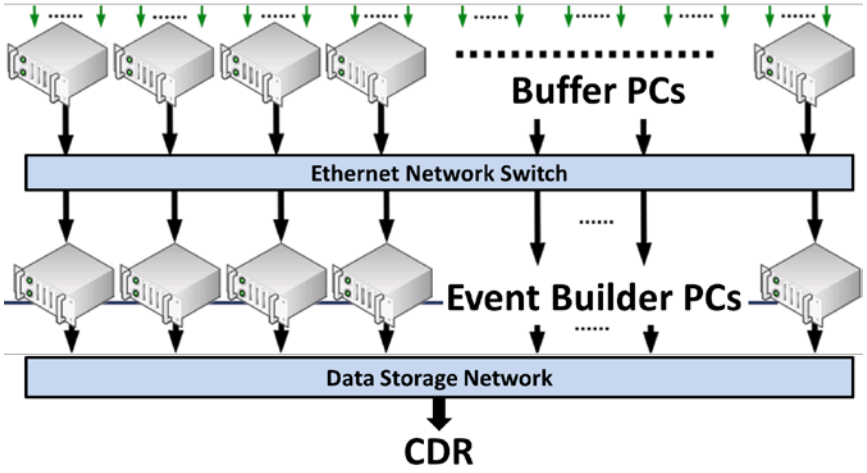
FPGA



- Usage of FPGAs and exploiting its properties:
  - Parallel processing
  - Pipeline architectures
- Collecting of all data in one FPGA-module
- Optional multiplexing stages to reduce number of incoming links
- Distribution of data flow to different computer nodes

Event Builder – CPU vs. FPGA

CPU (sequential)



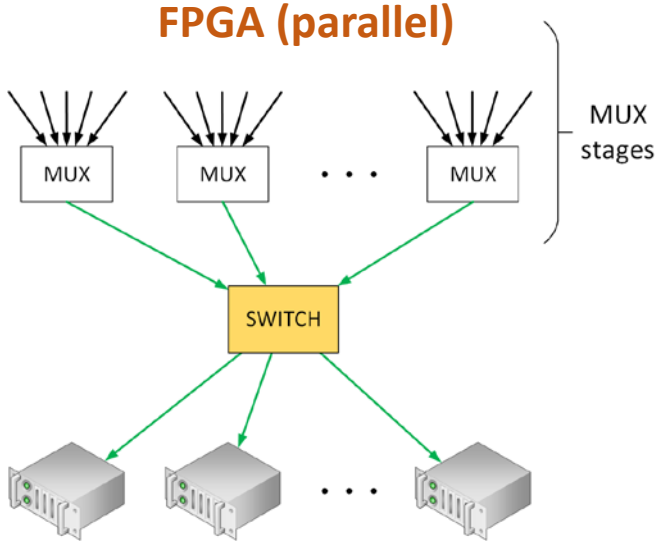
Disadvantages:

- Throughput limited by EB-network
- Performance of sequential execution strongly depends on algorithm complexity
- Recovery of hanging processes takes significant time

Advantages

- Easy integration of redundancy elements
- Uses mass-produced components
- Knowledge and templates available

FPGA (parallel)



Advantages:

- Continuation of the pipeline architecture in FEE
- Only FPGA allows to build real real-time systems
- High scalability
- High reliability

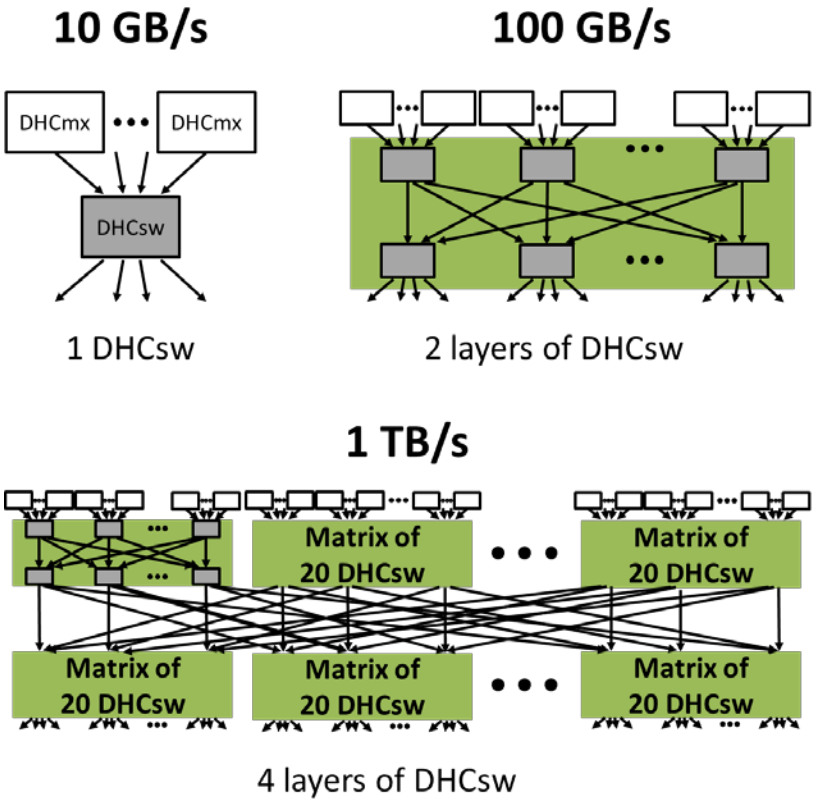
Disadvantages:

- Longer development time

⇒ **Motivation for**

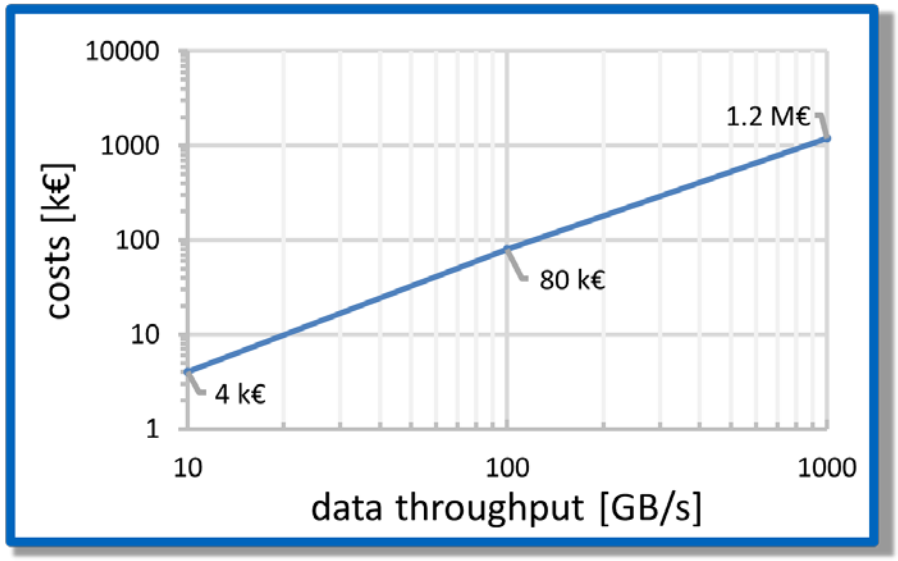
- Minimizing or elimination of real-time processes
- Development of highly automatized and reliable DAQ

Scaling Possibility of Hardware EB



Scenario for:

- Xilinx **7-series FPGA**
- SLINK interfaces replaced by **Aurora**



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   - **Hardware**
   - **Firmware**
   - **Software**
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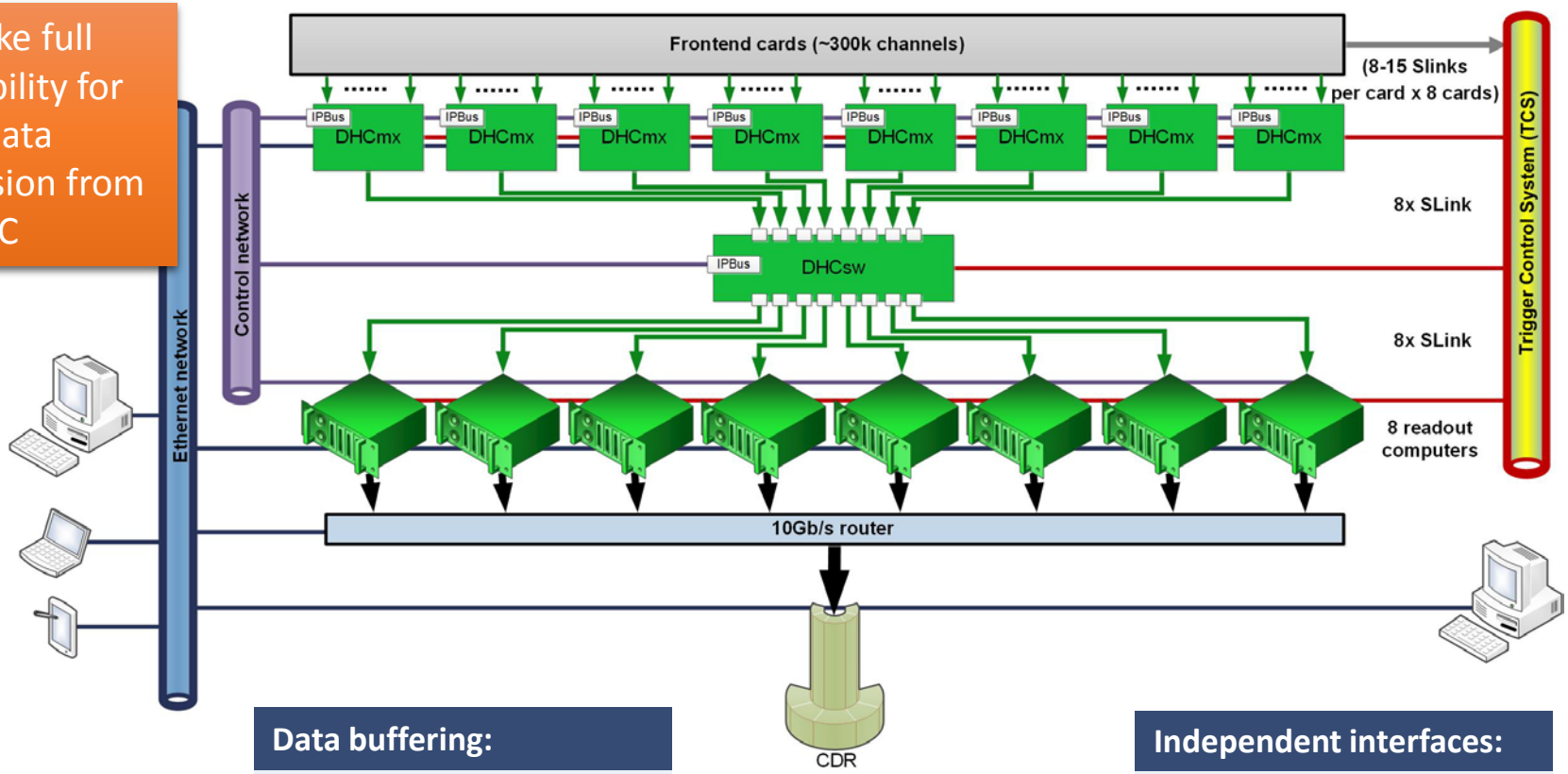
iFDAQ – System Design

FPGAs take full responsibility for reliable data transmission from FEEs to PC



Data buffering:

- 4GB RAM on each module => possibility to average data rate over spill cycle
- 1 GB/s sustained rate

Independent interfaces:

- synchronization → **TCS (Trigger Control System)**
- data flow (event building) → **SLINK**
- configuration and data flow control -> **Ipbus**

iFDAQ – System Design

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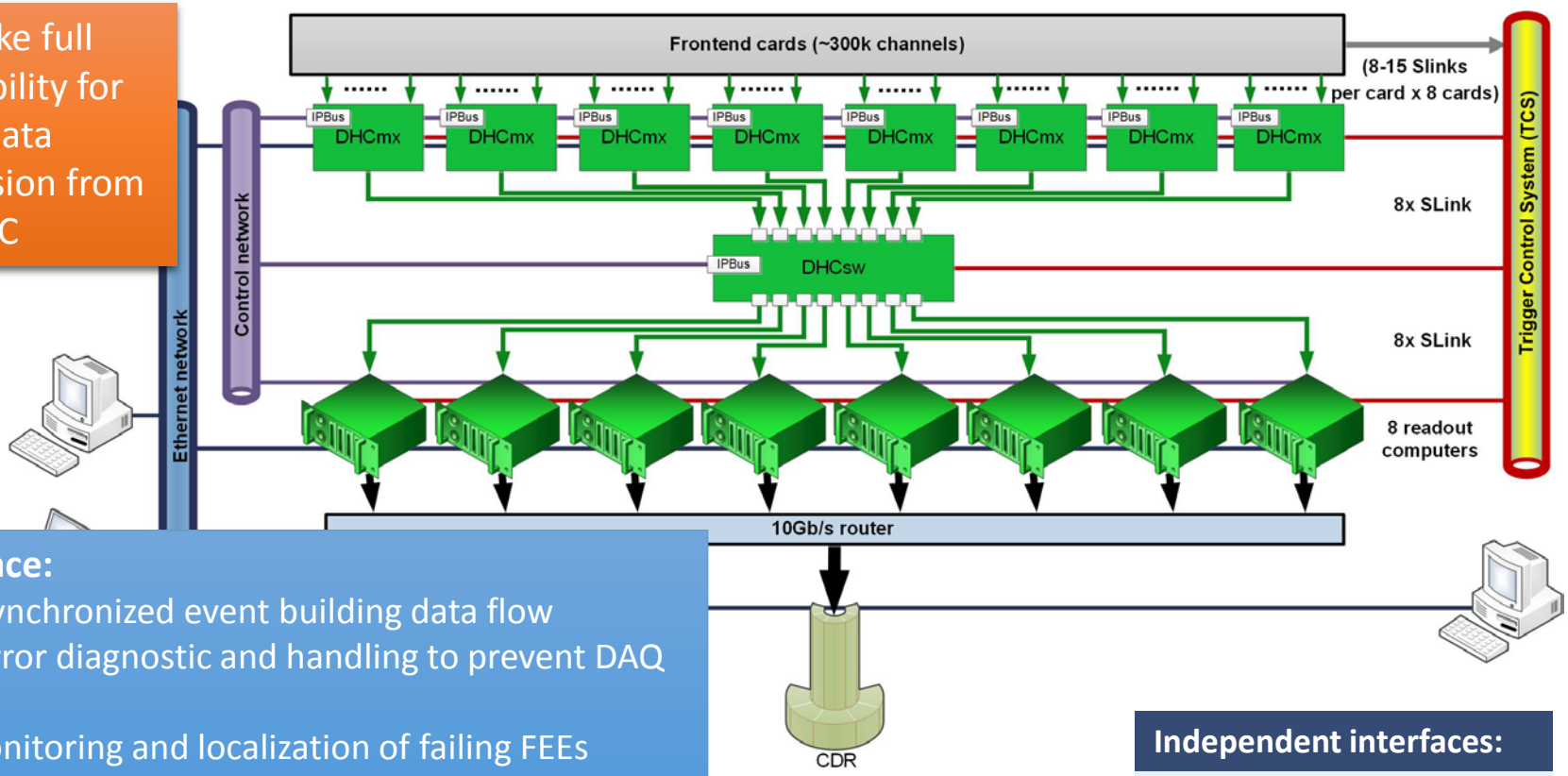

Intelligence:

- Self-synchronized event building data flow
- FEE error diagnostic and handling to prevent DAQ crash
  => monitoring and localization of failing FEEs
- Automatic resynchronization of FEEs
  => FEEs can be attached at any time
  => continuous data taking
  => continuous monitoring of data stream and FFE status

Independent interfaces:

- synchronization → **TCS (Trigger Control System)**
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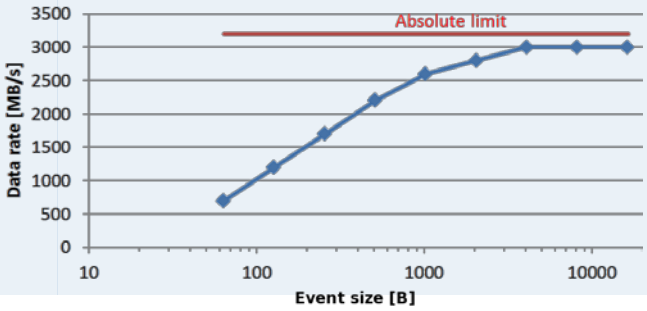
Data Handling Card (DHC)

AMC module

- **form factor:** AMC standard
- **FPGA:** Virtex6 XC6VLX130T
- **memory:** 4 GB DDR3 SDRAM
- **firmware:**
  - **DHCmx** 12:1 multiplexer [1]
  - **DHCsw** 8x8-switch
- **data rate:**



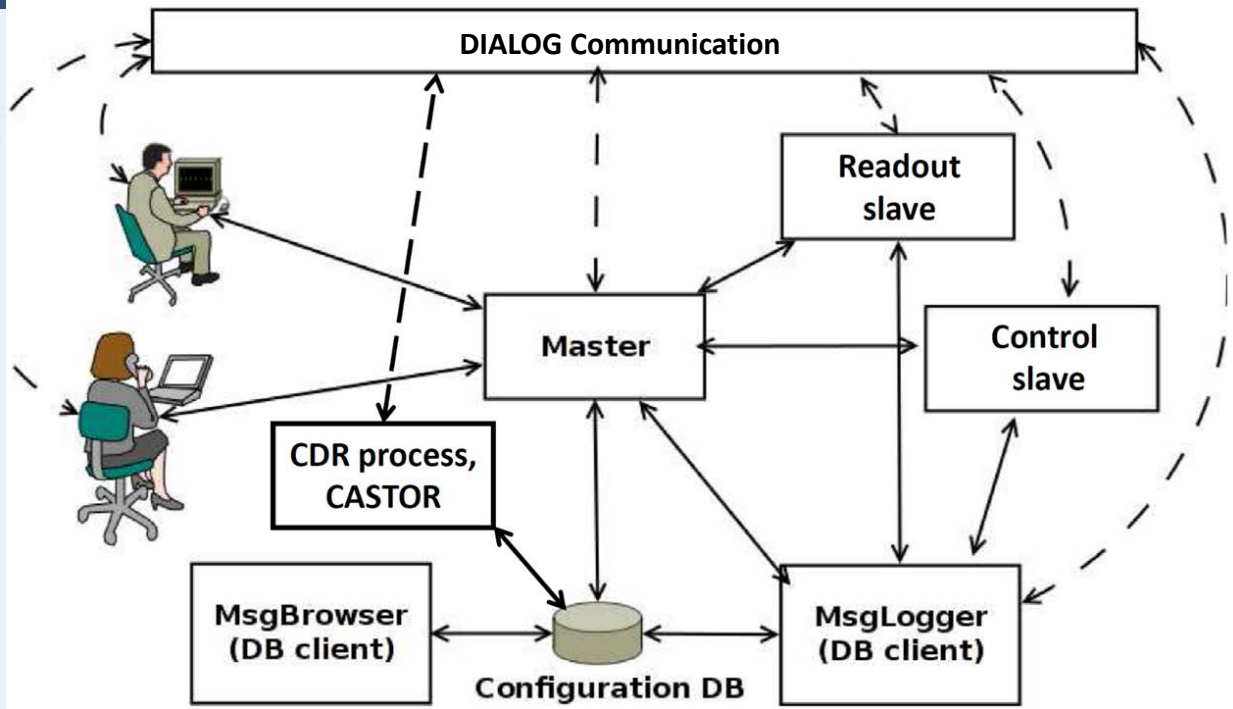
VME carrier card

- **form factor:** 6 U VME
- **interfaces:**
  - TCS (Trigger Control System) receiver
  - 1 Gb Ethernet for control network (IPbus)
  - 16 serial data links (SLINK)
  - JTAG for backup programming of FLASH

RCCAR software

Run Control, Configuration, And Readout Software (RCCARS):

- **Multilayer system** around master process
  - **master:**
    Middleman between GUI, DB, all other processes
  - **GUIs**
    display overall status of iFDAQ, control behavior of iFDAQ (when in Control mode)
  - **readout slaves (only real-time processes)**
    readout of data, analysis of events, error check, transformation into DATE-format, distribution to monitoring tools, writing to HDD
  - **control slaves**
    monitoring and control of hardware nodes
  - **message logger**
    collection of msgs from processes, storing msgs in DB
  - **message browser**
    display of msgs and support for advanced filtering
  - **Central Data Recording (CDR)**
    transfer of raw data to CASTOR, disk cleaning for new data
- Inter-process communication via **DIALOG library** (Custom-developed server/client communication)



ICHEP 2017 Paris

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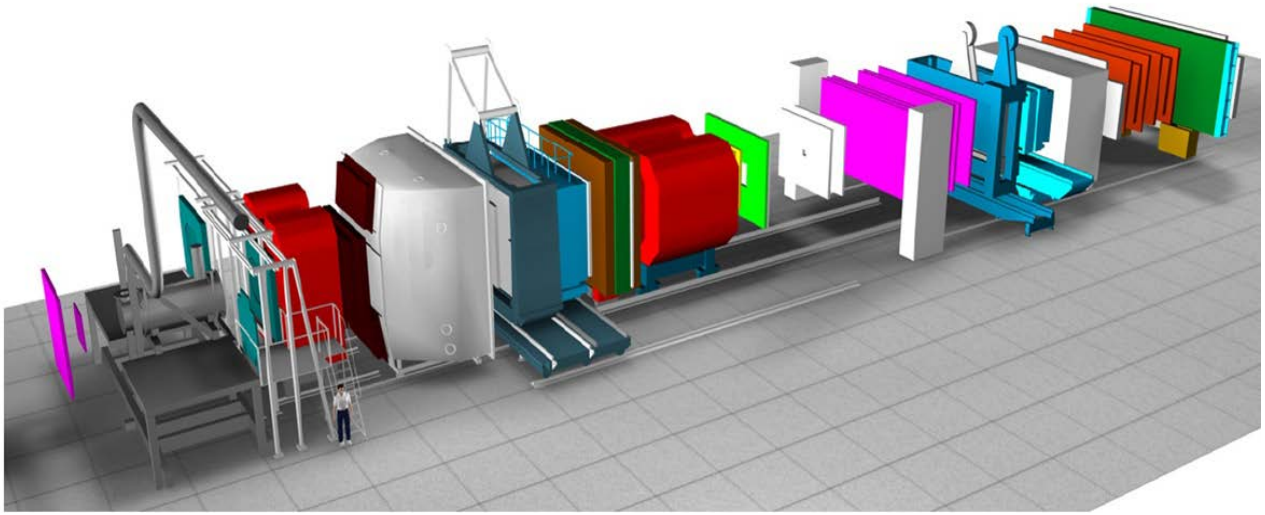
COMPASS – Overview

COmmon
Muon
Proton
Apparatus for
Structure and
Spectroscopy

- Fixed target experiment at SPS accelerator at CERN (M2 beamline)
- High intensity beams: $4 \cdot 10^7 \frac{\mu}{s}$; $2 \cdot 10^7 \frac{\text{hadrons}}{s}$
- Multi-purpose experiment
- Start of data-taking: 2001
- Since 2014: New DAQ with hardware event builder (iFDAQ)



COMPASS – Spectrometer Setup

spectrometer facts	
• Length:	60m
• Amount of channels:	300.000
• Trigger rate:	30 kHz
• On-spill data rate:	1.5 GB/s
• Event size:	20-50 kB

- Fixed target experiment at SPS accelerator at CERN (M2 beamline)
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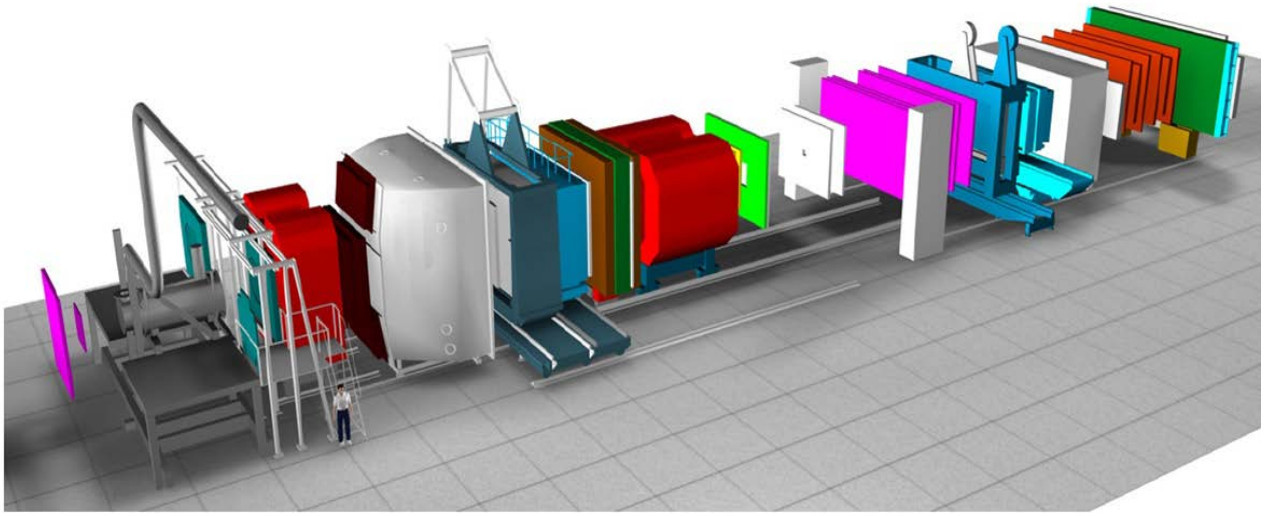
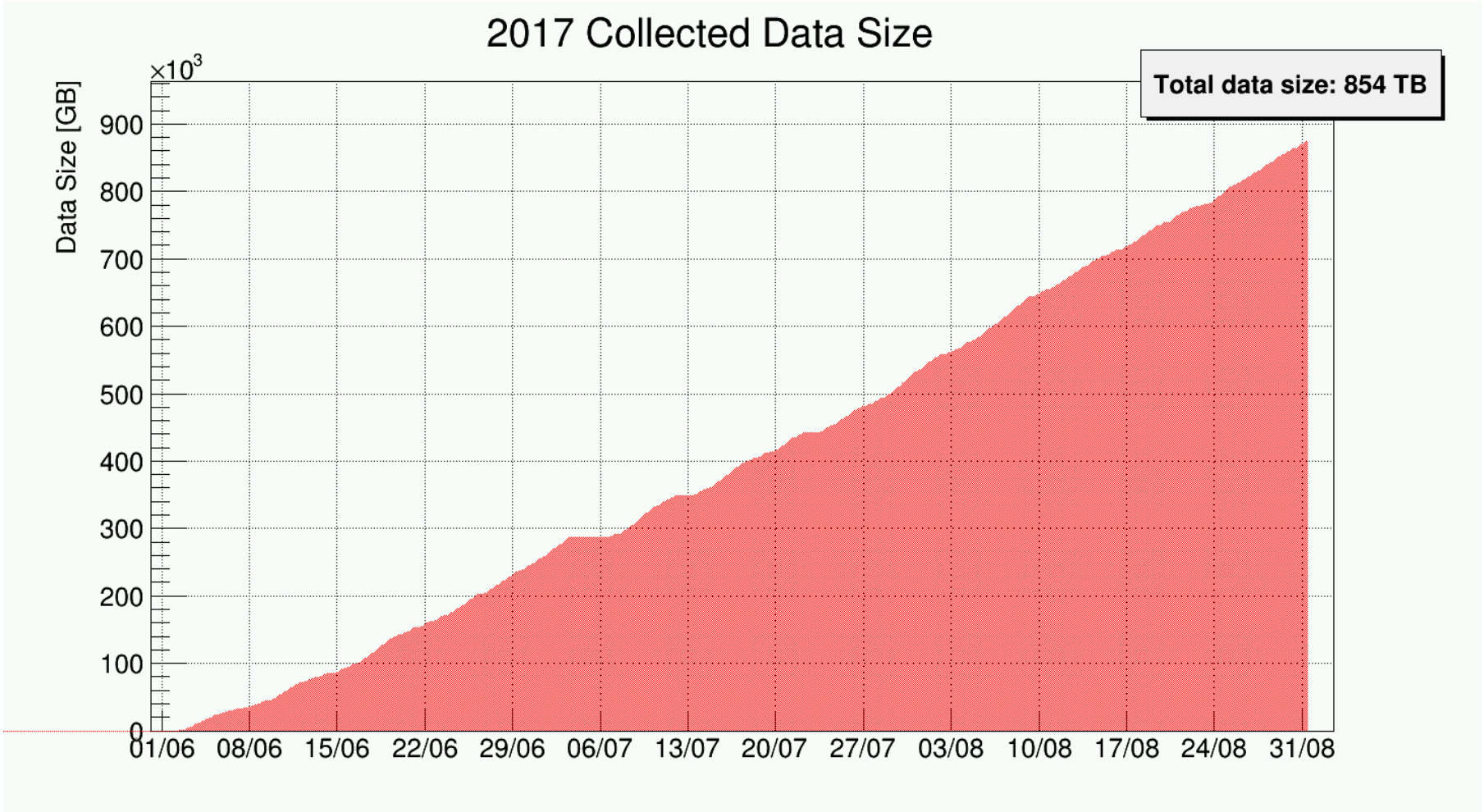
Source [2]



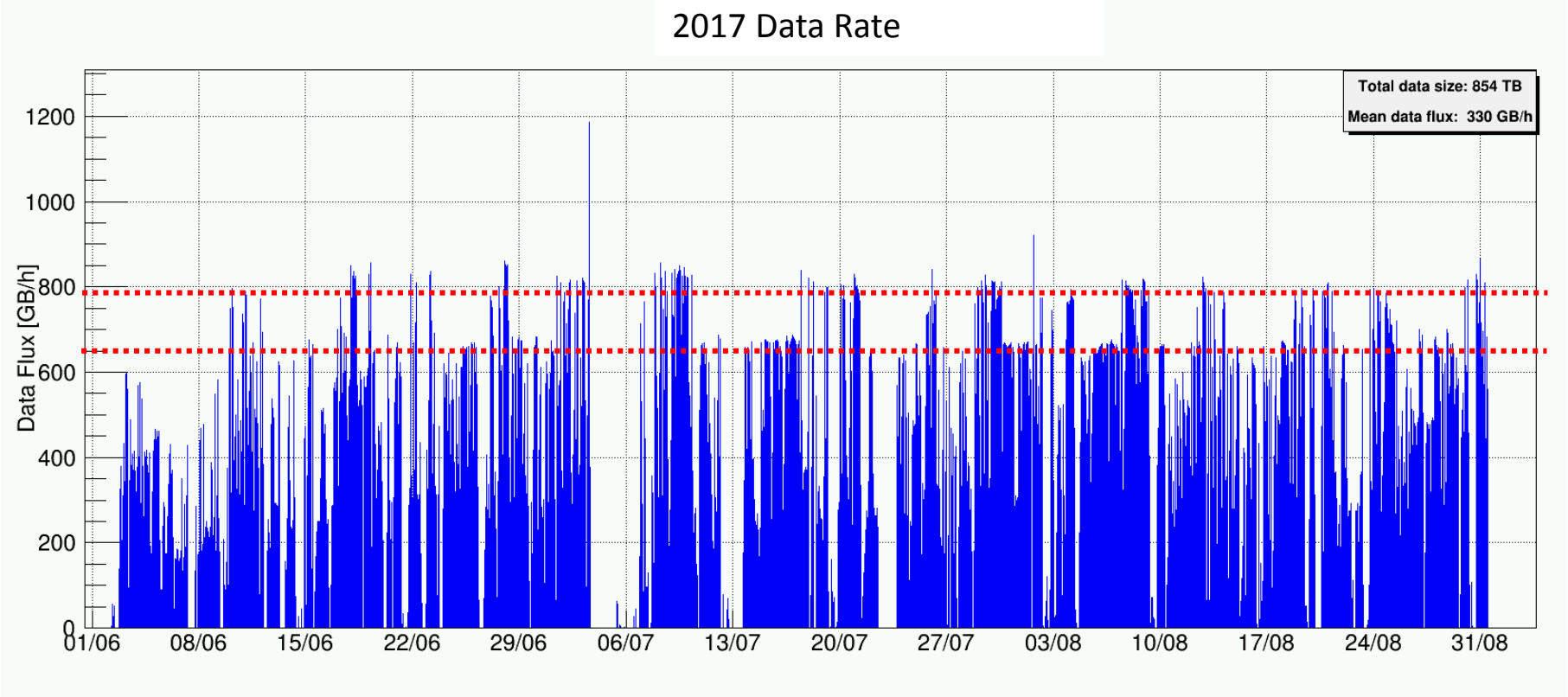
iFDAQ in COMPASS – Hardware Parts

- Very compact: 30 online PC in **former** DAQ
  Now: 1 VME crate (6-U) + one rack (8 computers)
- Highly flexible: Easily adaptable to different spectrometer setups (e.g. Drell-Yan 2016 vs. DVCS 2017)

Performance – Accumulated Data 2017



Performance – Data Rate 2017

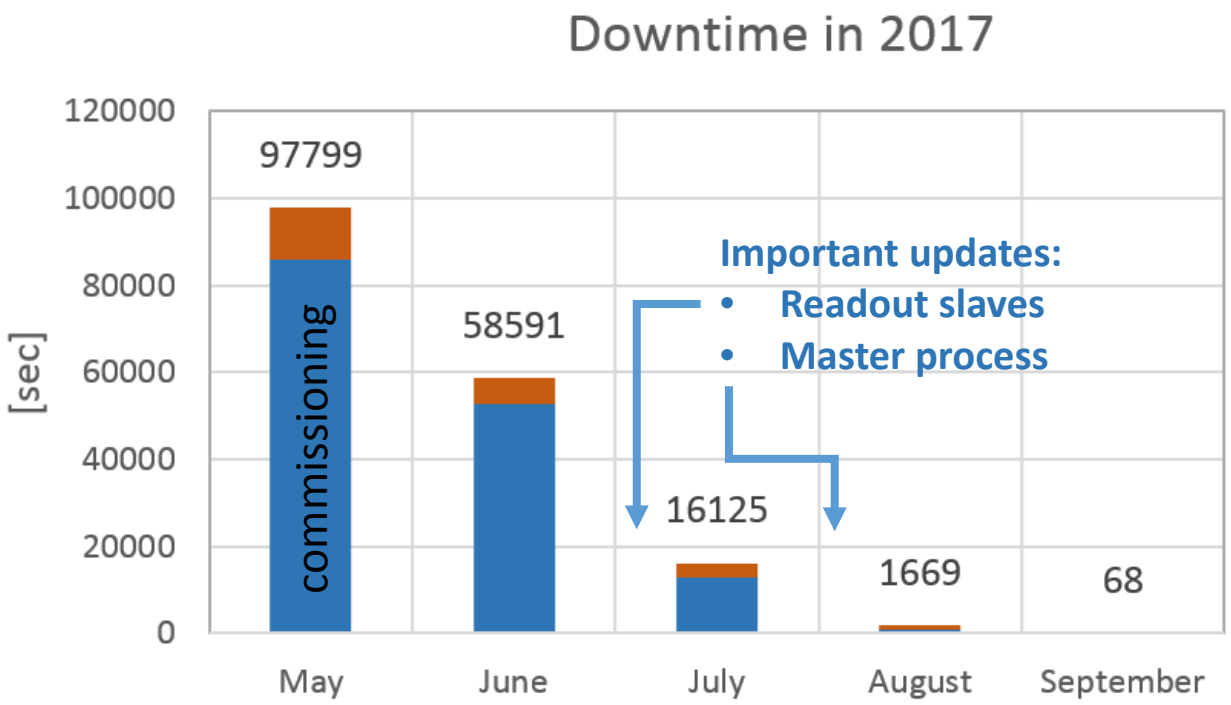


Spiky structure reflects beam intensity

Average data rate: 91.7 MB/s

Average over stable beam periods: 250 MB/s

Perfomance – Uptime in 2017



PCI/DMA error

Error occurrence usually after scrambled data

Automatic safe stop

Automatic safe stop of data run

- When desynchronization of data flow in event builder
- Data error on switch level in 3 consecutive spills

UPTIME (%)	96.35%	97.74%	99.40%	99.94%	99.99%

Highly reliable

Two effects:

1. More stable detectors
2. Upgrades of RCCAR software

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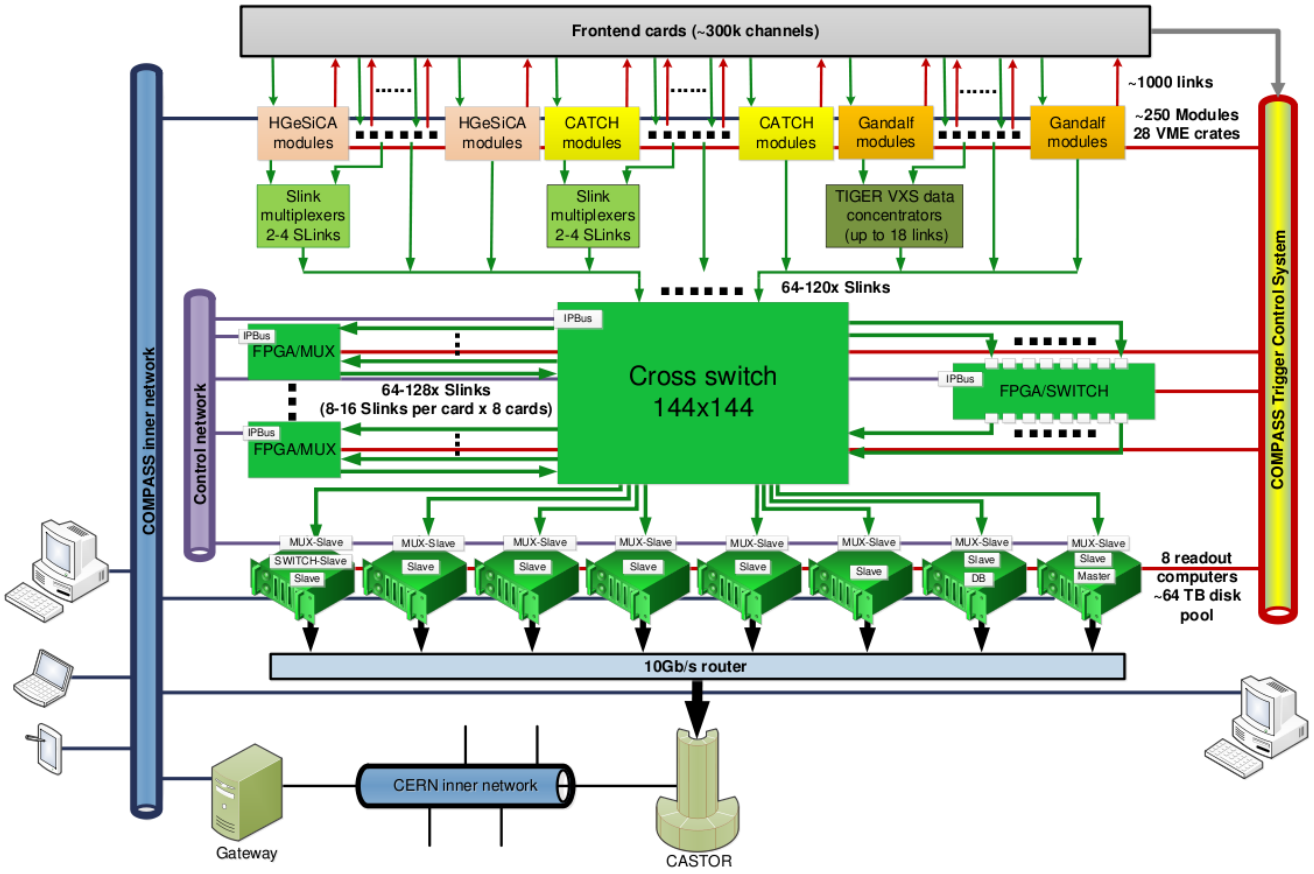
Crosspoint Switch - Integration

Crosspoint Switch

- connects:
  - FE electronics
  - DHCmx modules
  - DHCsw module
  - Spillbuffers
- purpose:
  - Ease of load balancing
  - System redundancy to compensate hardware failures

⇒ **provides fully customizable network topology**



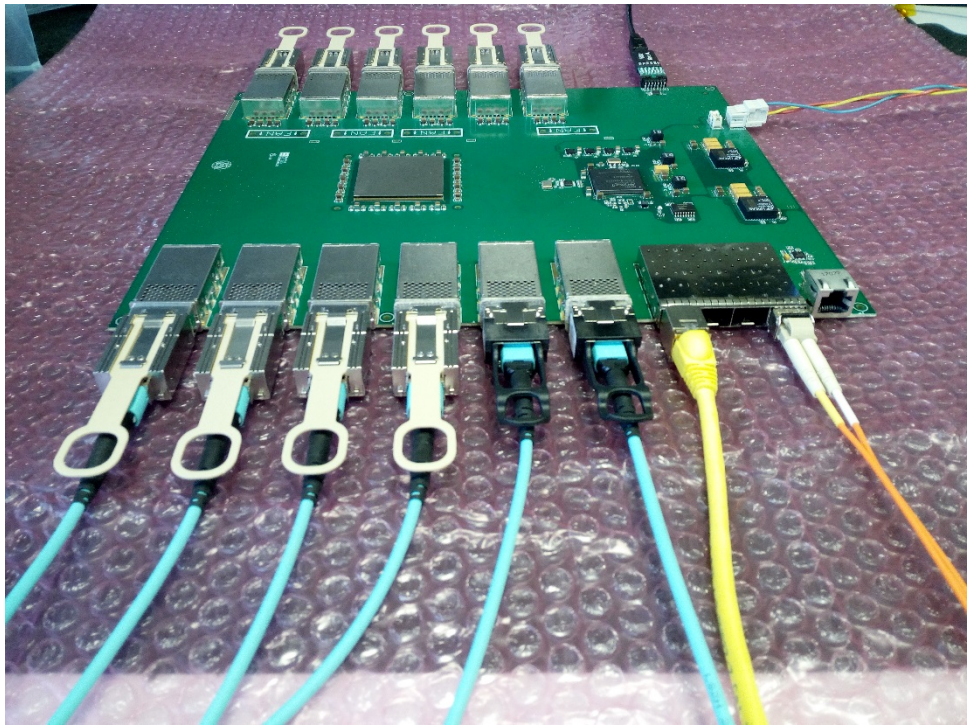
Crosspoint Switch – Hardware Design

Crosspoint Switch Components

- **interfaces:**
  - 12 x 12 channel CXP transceiver (MPO fiber connectors)
  - Ethernet for IPbus
  - JTAG
  - TCS (Trigger Control System) receiver

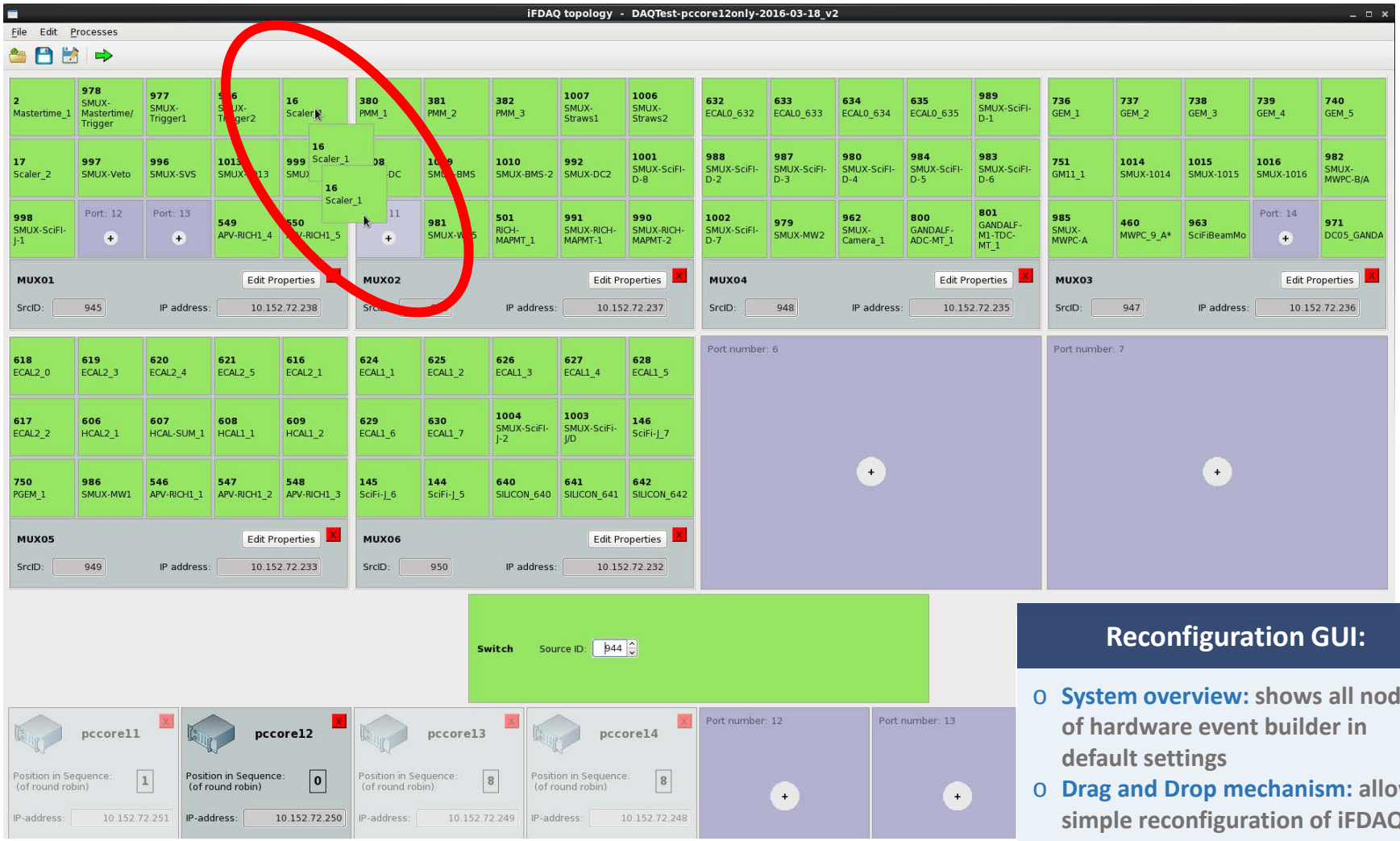
- **Switching and Control:**
  - **Vitesse VSC3144-02** – fully configurable 144x144, asynchronous, 6.5 Gbps crosspoint switch
  - **Xilinx Artix-7 FPGA** for switch control and monitoring

Status: module produced
testing to be started



- **Interface FPGA – Crosswitch:**
  - 90 MHz, 11-bit parallel data bus
  - Multiple program assignments can be queued and issued simultaneously ⇒ fast programming

Crosspoint Switch – Software



Reconfiguration GUI:

- **System overview:** shows all nodes of hardware event builder in default settings
- **Drag and Drop mechanism:** allows simple reconfiguration of iFDAQ topology

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Outlook

Ongoing development:

- Integration of Redundancy Logic

  -> integration of the hardware for the crosspoint switch

  -> upgrade of Software for automatic identification of malfunctioning hardware parts

- Debugging of Software to increase reliability with the help of the DAQ Debugger

Ideas for the Future:

- upgrade of TCS to bidirectional PON (**p**assive **o**ptical **n**etwork) with use of **U**niversal **C**ommunication **F**ramework (UCF) developed at TUM for on-the-fly reconfiguration of interconnections
- Minimizing of real-time processes

  -> direct writing of data onto SSD

Conclusion

- Improvements since commissioning of iFDAQ in 2014:
  - Increased reliability (Uptime around 99.99%)
  - Extended intelligence

    -> Automatic safe stop of the run for self-recovery

    -> Continuously running
  - No event size limit due to upgrades in firmwares
- Performance in 2017:
  - Data rate: 91.7 MB/s (average)

    250 MB/s (in stable beam conditions)

    380 MB/s (peak sustained rate)
  - On-spill data rate: 1.5 GB/s
- iFDAQ transferred to other HEP experiment (NA64)

THANK YOU for your Attention

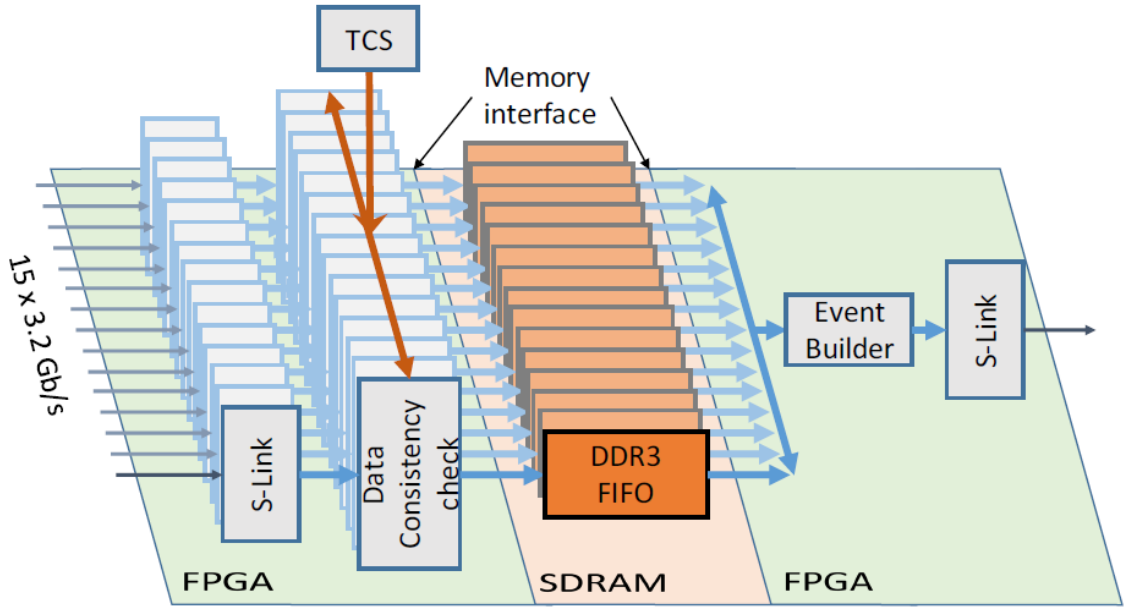
References

[1] Y. Bai et al., *New data acquisition system for the COMPASS experiment*, in proceedings of *Topical Workshop on Electronics for Particle Physics (TWEPP)*, Lisbon Portugal September 2015

[2] COMPASS collaboration, P. Abbon et al., *The COMPASS experiment at CERN, Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip., 577(3):455-518, 2007.*

Backup slides

Firmware – DHCmx



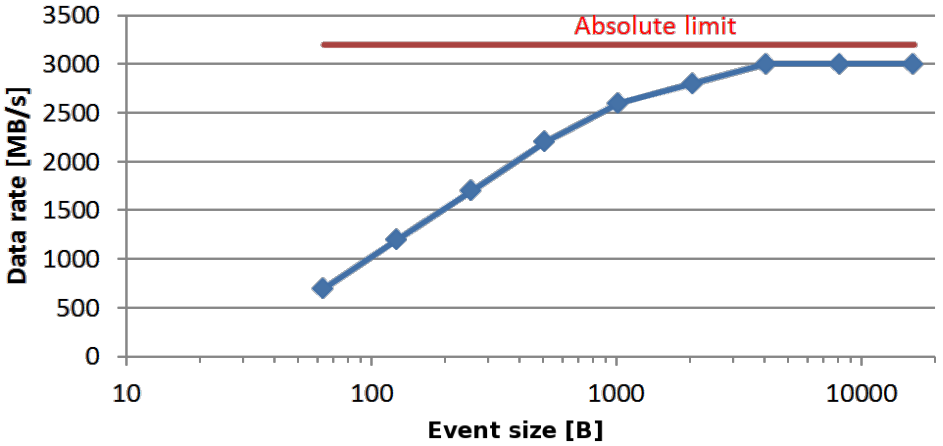
Data Consistency Check:

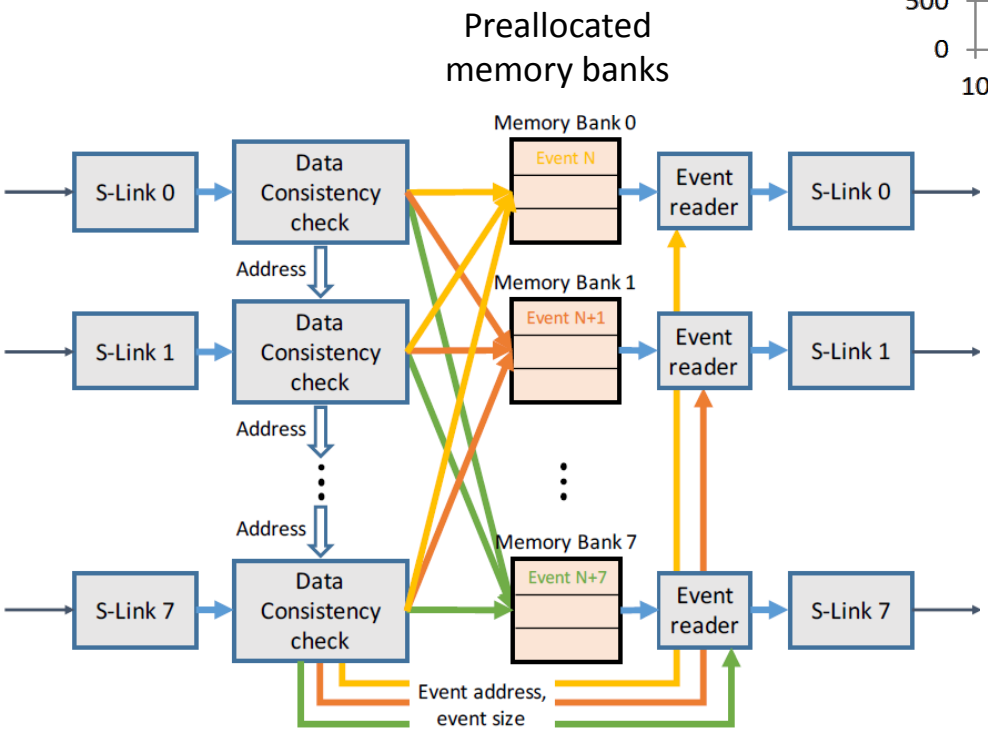
- Transmission errors detected by S-Link
- Truncation, i.e. mismatch between real and declared data block size
- Inconsistency of event label
- Missing data -> timeout

Error detected

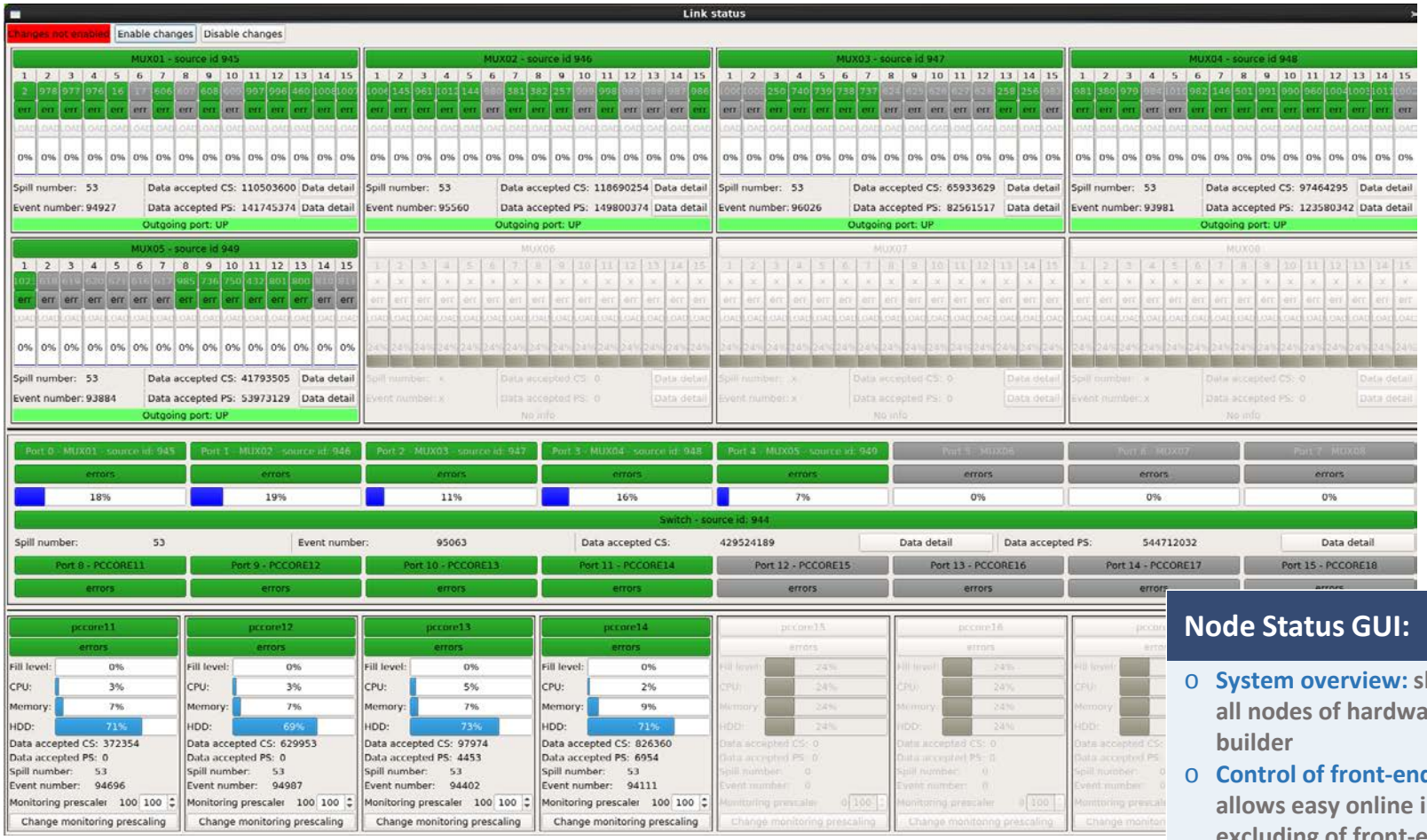
- Discarding/throttling of wrong data
- Adding of specific header
- Setting error flag in local register

Firmware – DHCsw





Run Control & Node Status GUI



Node Status GUI:

- **System overview:** shows status of all nodes of hardware event builder
- **Control of front-end modules:** allows easy online including, excluding of front-end modules into DAQ and reloading of front-end modules