TWEPP 2017 – Topical Workshop on Electronics for Particle Physics

Integration of Intelligence and Redundancy Elements into the FPGA-Based DAQ of the COMPASS Experiment

Bodlák Martin, Frolov Vladimir, Huber Stefan, Jarý Vladimír, Konorov Igor, Květoň Antonín, Nový Josef, <u>Steffen Dominik</u>, Šubrt Ondřej, Tomsa Jan, Virius Miroslav

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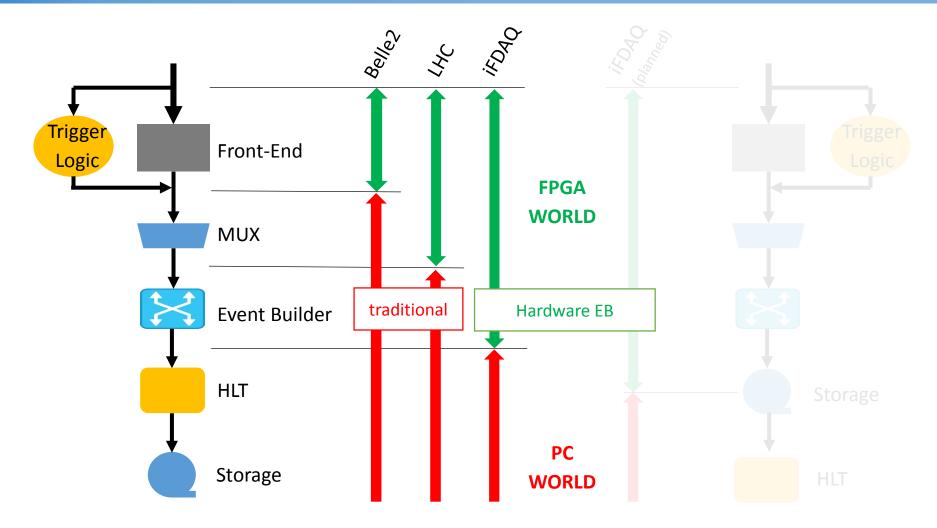
- 1. Motivation and Concept of Hardware Event Building
- 2. Design of the intelligent FPGA-based DAQ
  - System
  - Hardware
  - Firmware
  - Software
- 3. iFDAQ integration and performance in COMPASS
  - Setup of COMPASS spectrometer
  - iFDAQ Performance and Status in 2017
- 4. Integration of Redundancy Logic
  - Software
  - Hardware
- 5. Outlook and Conclusion

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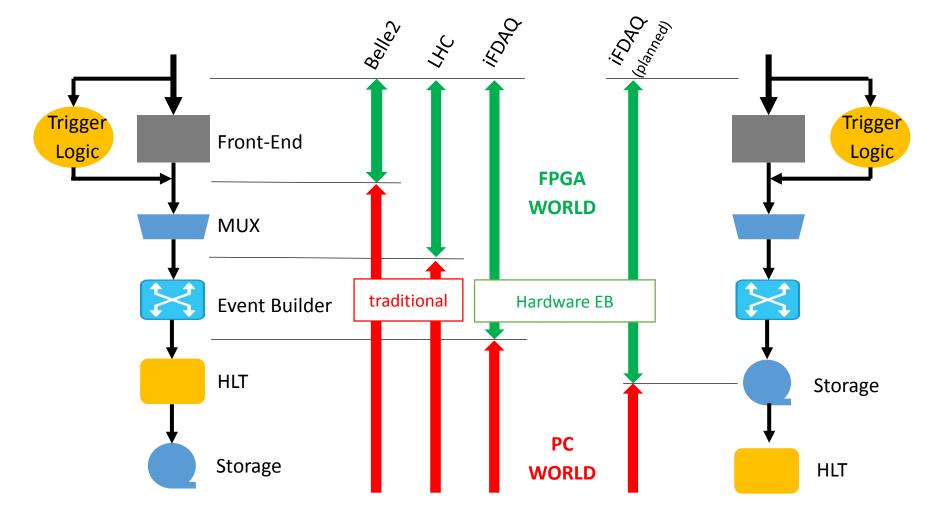
Conclusion

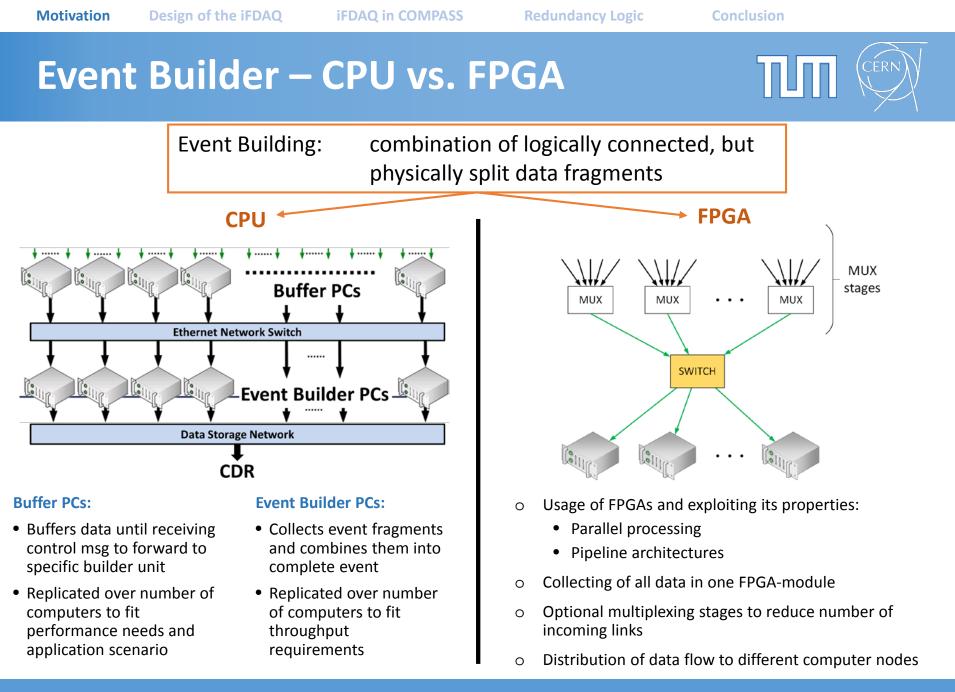


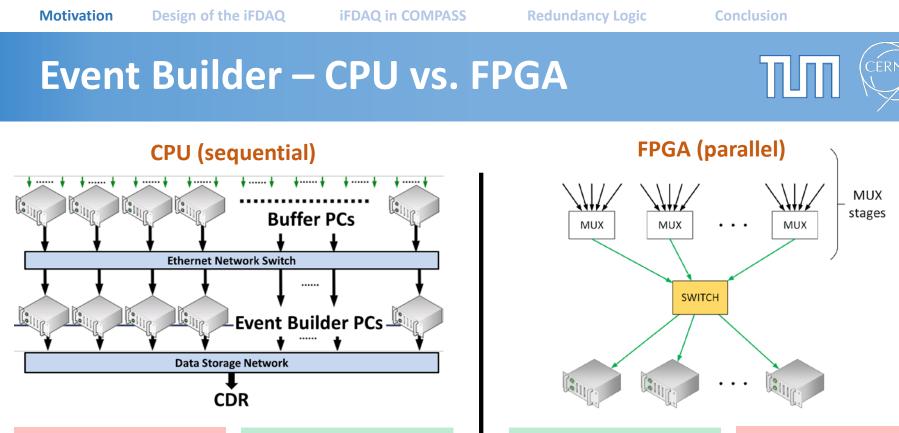


Conclusion









#### **Disadvantages:**

- Throughput limited by EB-network
- Performance of sequential execution strongly depends on algorithm complexity
- Recovery of hanging processes takes significant time

#### **Advantages**

- Easy integration of redundancy elements
- Uses mass-produced components
- Knowledge and templates available

#### **Advantages:**

- Continuation of the pipeline architecture in FEE
- Only FPGA allows to build real real-time systems
- High scalability
- High reliability

#### **Disadvantages:**

• Longer development time

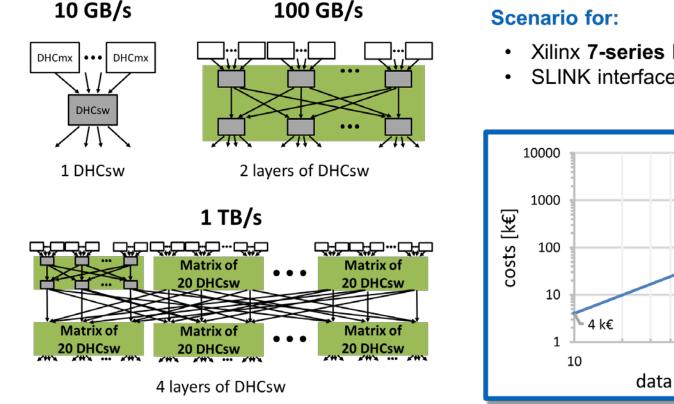
#### $\Rightarrow$ Motivation for

- Minimizing or elimination of realtime processes
- Development of highly automatized and reliable DAQ

Conclusion

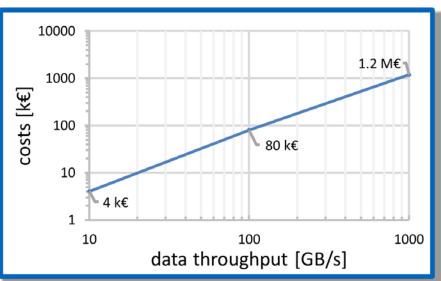


## **Scaling Possibility of Hardware EB**



### Scenario for:

- Xilinx 7-series FPGA
- SLINK interfaces replaced by Aurora



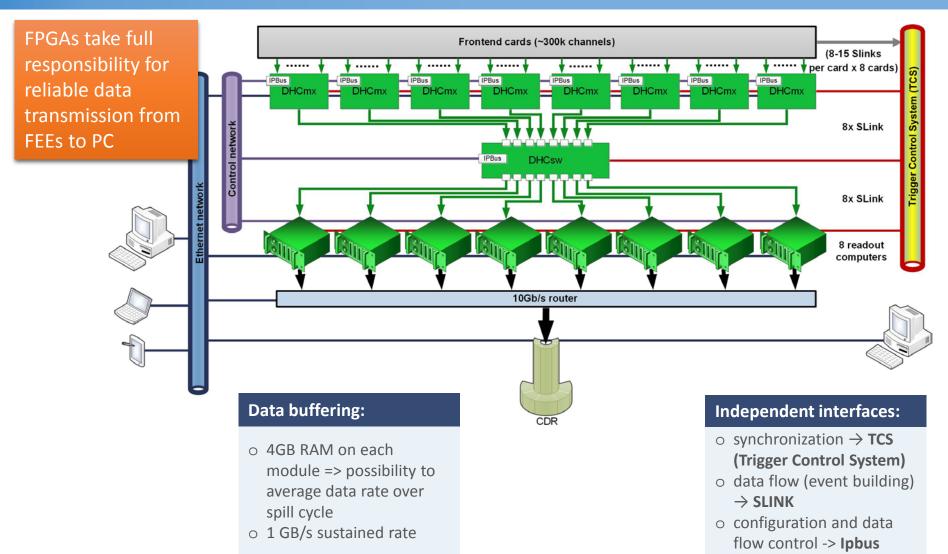
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**iFDAQ in COMPASS** 

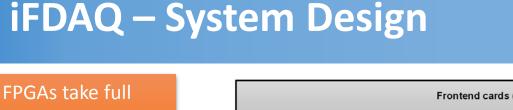
**Redundancy Logic** 

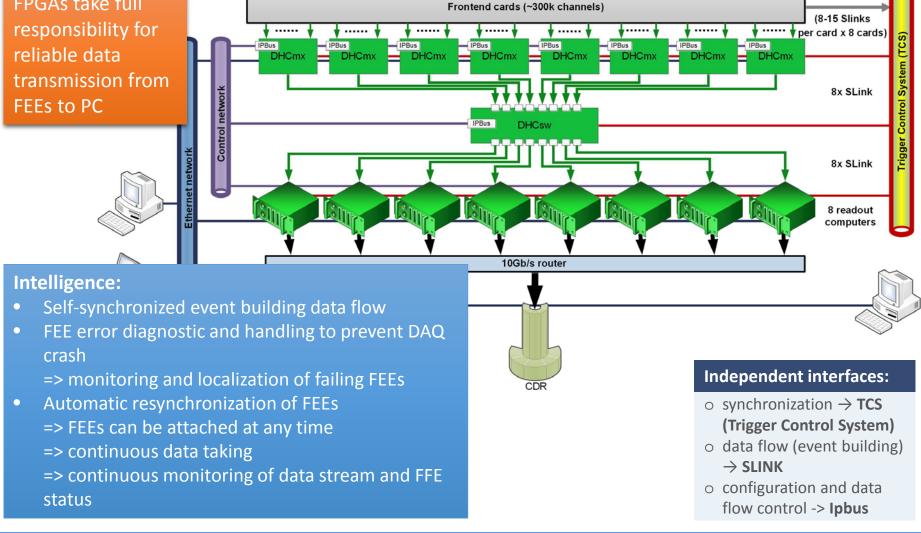
Conclusion

### iFDAQ – System Design



Conclusion





Conclusion

## Data Handling Card (DHC)

### AMC module

$\circ$ form factor:	AMC standard					
○ FPGA:	Virtex6 XC6VLX130T					
o memory:	4 GB DDR3 SDRAM					
o firmware:	<ul> <li>DHCmx 12:1 multiplexer [1]</li> <li>DHCsw 8x8-switch</li> </ul>					
o data rate: 300 300 300 300 300 300 300 300						
	10 100 1000 10000 Event size [B]					

### VME carrier card

 $\circ\,$  form factor:

6 U VME

- o interfaces:
- TCS (Trigger Control System) receiver
- 1 Gb Ethernet for control network (IPbus)
- 16 serial data links (SLINK)
- JTAG for backup programming of FLASH



Conclusion

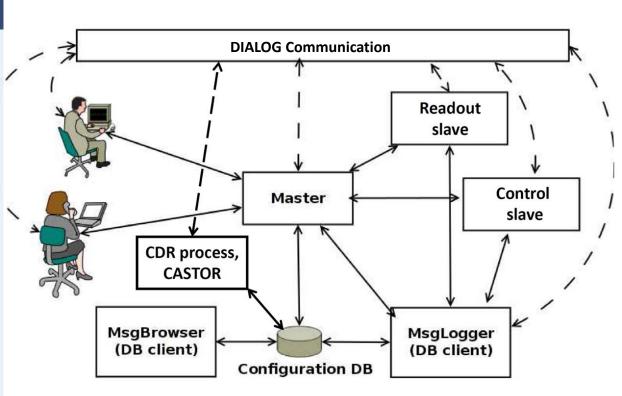
### **RCCAR** software

### Run Control, Configuration, And Readout Software (RCCARS):

- o Multilayer system around master process
  - master: Middleman between GUI, DB, all other processes
  - GUIs

display overall status of iFDAQ, control behavior of iFDAQ (when in Control mode)

- readout slaves (only real-time processes) readout of data, analysis of events, error check, transformation into DATE-format, distribution to monitoring tools, writing to HDD
- control slaves monitoring and control of hardware nodes
- message logger collection of msgs from processes, storing msgs in DB
- message browser display of msgs and support for advanced filtering
- Central Data Recording (CDR) transfer of raw data to CASTOR, disk cleaning for new data
- Inter-process communication via DIALOG library (Custom-developed server/client communication)



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Motivation

**COMPASS – Overview** 

**iFDAQ in COMPASS** 

**Redundancy Logic** 

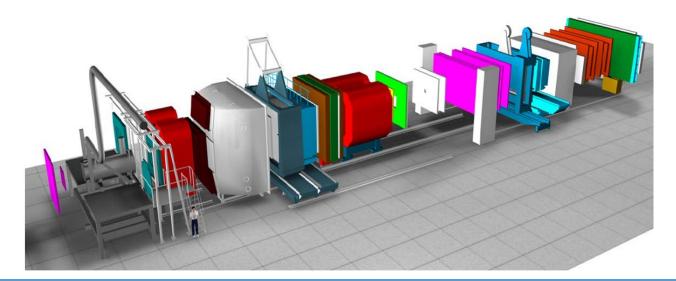
Conclusion

# 



COmmon Muon Proton Apparatus for Structure and Spectroscopy

- Fixed target experiment at SPS accelerator at CERN (M2 beamline)
- High intensity beams:  $4 \cdot 10^7 \frac{\mu}{s}$ ;  $2 \cdot 10^7 \frac{\text{hadrons}}{s}$
- o Multi-purpose experiment
- Start of data-taking: 2001
- Since 2014: New DAQ with hardware event builder (iFDAQ)

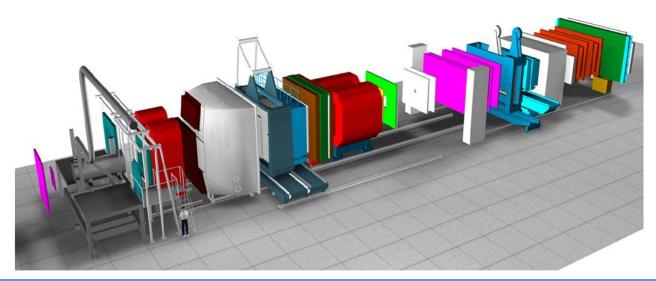


### **COMPASS – Spectrometer Setup**

	spectrometer fa	icts
•	Length:	60m
•	Amount of channels:	300.000
•	Trigger rate:	30 kHz
•	On-spill data rate:	1.5 GB/s
•	Event size:	20-50 kB

Source [2]

- Fixed target experiment at SPS accelerator at CERN (M2 beamline)
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Dominik Steffen | TWEPP – Santa Cruz | 13/09/2017



- Very compact: 30 online PC in former DAQ
   Now: 1 VME crate (6-U) + one rack (8 computers)
- Highly flexible: Easily adaptable to different spectrometer setups (e.g. Drell-Yan 2016 vs. DVCS 2017)





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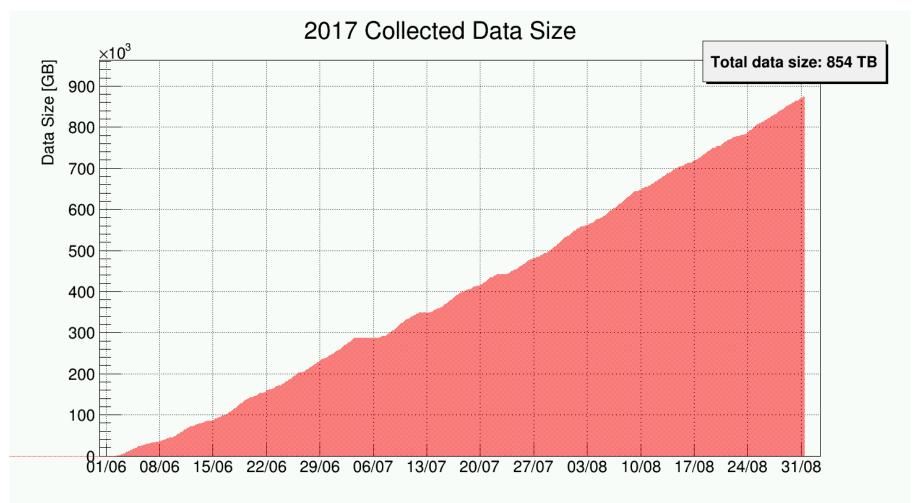


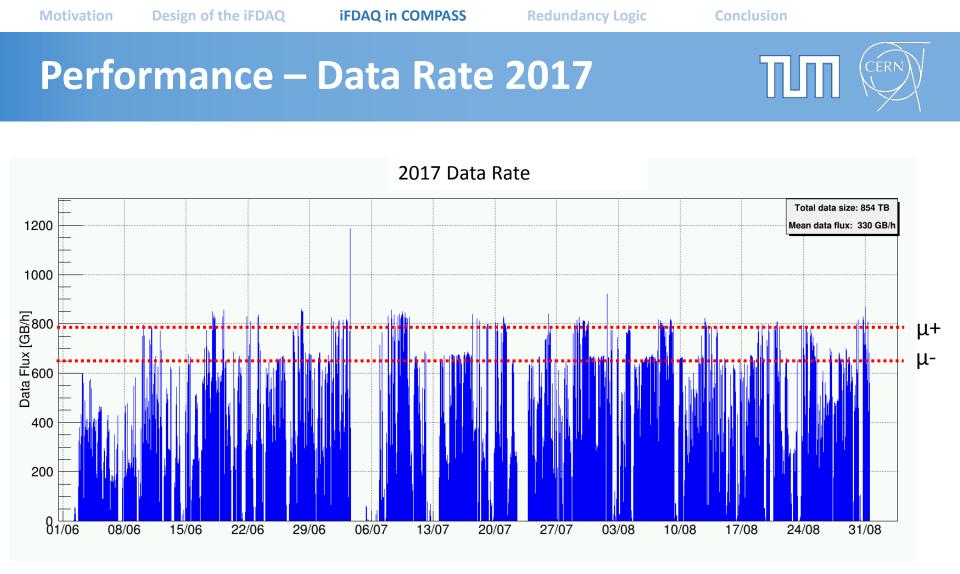
**iFDAQ in COMPASS** 

**Redundancy Logic** 

Motivation

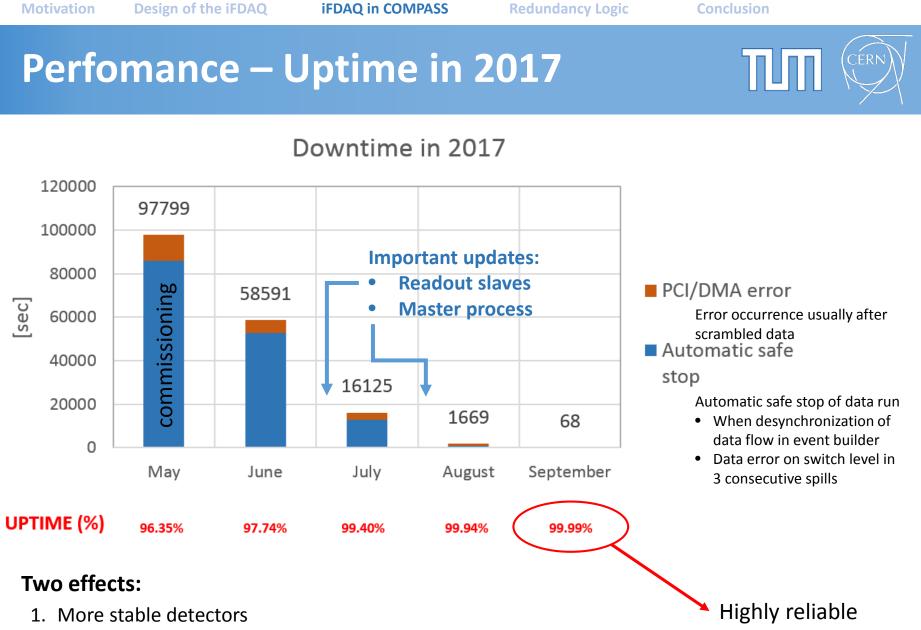






Spiky structure reflects beam intensity

Average data rate: 91.7 MB/s Average over stable beam periods: 250 MB/s



2. Upgrades of RCCAR software

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## **Crosspoint Switch - Integration**

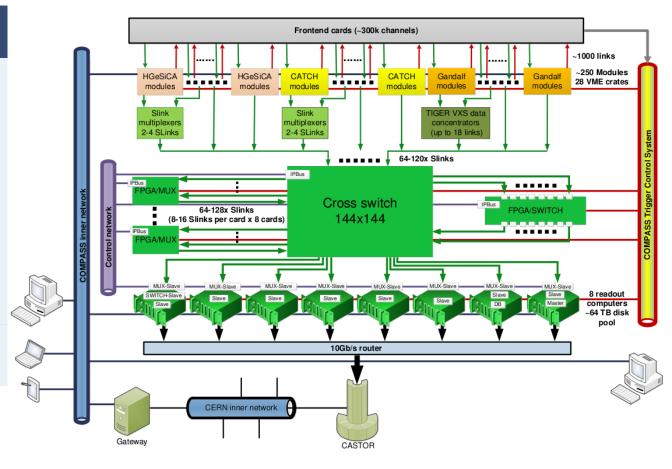
### **Crosspoint Switch**

#### $\circ$ connects:

- FE electronics
- DHCmx modules
- DHCsw module
- Spillbuffers

### o purpose:

- Ease of load balancing
- System redundancy to compensate hardware failures
- ⇒ provides fully customizable network topology



Conclusion



## **Crosspoint Switch – Hardware Design**

### **Crosspoint Switch Components**

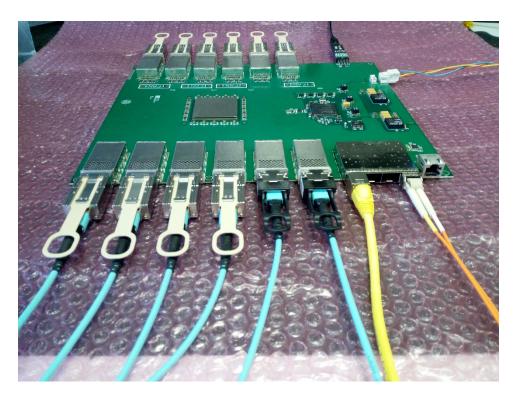
### $\circ$ interfaces:

- 12 x 12 channel CXP transceiver (MPO fiber connectors)
- Ethernet for IPbus
- JTAG
- TCS (Trigger Control System) receiver

### $\odot$ Switching and Control:

- Vitesse VSC3144-02 fully configurable 144x144, asynchronous, 6.5 Gbps crosspoint switch
- Xilinx Artix-7 FPGA for switch control and monitoring

# Status: module produced testing to be started



### • Interface FPGA – Crosswitch:

- 90 MHz, 11-bit parallel data bus
- Multiple program assignments can be queued and issued simultaneously ⇒ fast programming

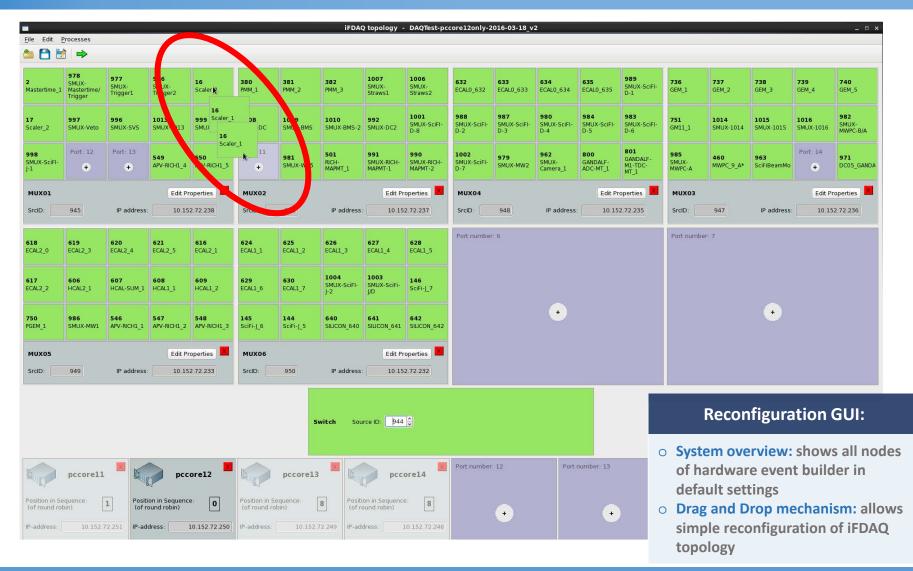
Motivation

**iFDAQ in COMPASS** 

**Redundancy Logic** 

Conclusion

## **Crosspoint Switch – Software**



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### • Ongoing development:

- Integration of Redundancy Logic
  - -> integration of the hardware for the crosspoint switch
  - -> upgrade of Software for automatic identification of malfunctioning hardware parts
- Debugging of Software to increase reliability with the help of the DAQ Debugger

### Ideas for the Future:

- upgrade of TCS to bidirectional PON (passive optical network) with use of Universal Communication Framework (UCF) developed at TUM for on-the-fly reconfiguration of interconnections
- Minimizing of real-time processes
  - -> direct writing of data onto SSD



- Improvements since commissioning of iFDAQ in 2014:
  - Increased reliability (Uptime around 99.99%)
  - Extended intelligence
    - -> Automatic safe stop of the run for self-recovery
    - -> Continuously running
  - No event size limit due to upgrades in firmwares
- Performance in 2017:
  - Data rate: 91.7 MB/s (average)
     250 MB/s (in stable beam conditions)
     380 MB/s (peak sustained rate)
  - On-spill data rate: 1.5 GB/s
- o iFDAQ transferred to other HEP experiment (NA64)

### **THANK YOU for your Attention**





- [1] Y. Bai et al., *New data acquisition system for the COMPASS experiment*, in proceedings of *Topical Workshop on Electronics for Particle Physics (TWEPP)*, Lisbon Portugal September 2015
- [2] COMPASS collaboration, P. Abbon et al., *The COMPASS experiment at CERN, Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip., 577(3):455-518, 2007.*

### **Backup slides**

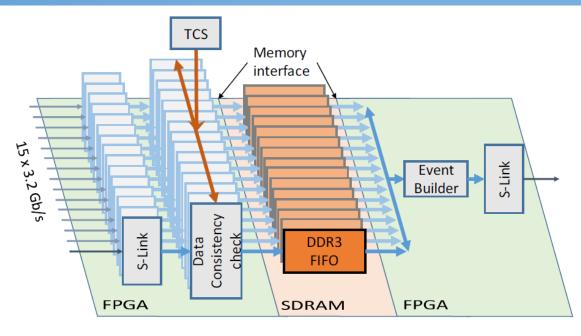
**iFDAQ in COMPASS** 

**Redundancy Logic** 

Conclusion



### **Firmware – DHCmx**

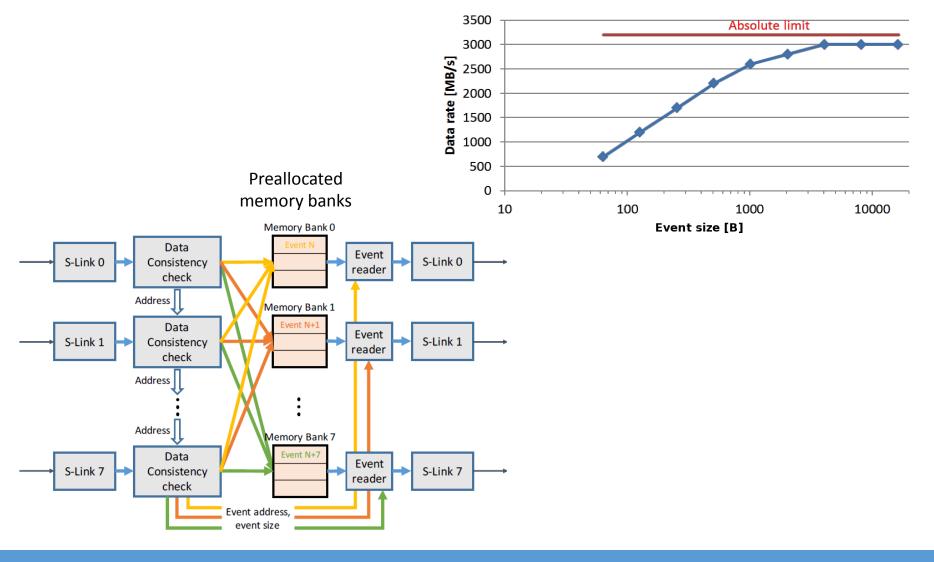


### **Data Consistency Check:**

- o Transmission errors detected by S-Link
- Truncation, i.e. mismatch between real and declared data block size
- Inconsistency of event label
- Missing data -> timeout

Error detected

- Discarding/throttling of wrong data
- Adding of specific header
- Setting error flag in local register



Motivation

**Redundancy Logic** 

Conclusion



### **Run Control & Node Status GUI**

			Link	status			
hanges not enabled Enable c	hanges Disable changes						
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Spill number:         S           Port 8 - PCCORE11         errors           errors         errors           ill level:         0%           5PU:         3%           demory:         7%           DD:         25%           Data accepted FS:         0.53           Spill number:         5.3           Vent number:         94696	3 Event numb Port.9 - PCCORE12 errors Fill level: 0% CPU: 3% Memory: 7% HDD: 65% Data accepted PS: 0 Spill number: 53 Event number: 94907	er: 95063 Port 10 - PCCORE13 errors	Switch - so Data accepted CS: Port 11 - PCCORE14 errors Fill level: 0% CPU: 2% Memory: 9% HDD: 21% Data accepted CS: 826360 Data accepted CS: 826360 Data accepted CS: 826360 Data accepted SS: 8054 Spill number: 53	unce id: 944           429524189           Port 12 - PCCORE15           errors           gencom15.           errors           Hill level           24%           PDI           24%           PDI           24%           PDD           24%           PDData accepted C5: 0           Odata accepted C5: 0           PdB amber           Event mumber	Data detail Data accept Port 13 - PCCORE16 errors Decement in errors Difference Data accept errors Data accept errors errors Data accept errors Data accept errors errors errors Data accept errors errors errors Data accept errors error	ed PS: 544712032 Port 14 - PCCORE17 errorr errorr Hill layer CPU: 0 Memory 0 Hill layer CPU: 0 Outs accepted CS: Data accepted CS: Data accepted CS: Control CS: 0 Control CS: 0 CS: 0	Data detail Port 15 - PCCORE 18 Ode Status GUI: System overview: all nodes of hardw builder Control of front-er
Spill number: 5 Port 8 - PCCOREL1 errors errors ill level: 0%. POI: 3%. ICD: 7%. IDD: 7%.	Event numb     Port 9 - PCCORE12     errors     errors     fill level: 0%     CPU: 3%     Memory: 7%     HDD: 65%     Data accepted C5: 629953     Data accepted P5: 0     Spill number: 53     Event number: 94907     Monitoring prescaler 100 100 \$	er: 95063 Port 10 - PCCORE13 errors	Switch - so Data accepted CS: Port 11 - PCCORE14 errors Fill level: 0% CPU: 2% Memory: 9% HDD: 21% Data accepted CS: 026360 Data accepted CS: 026360 Data accepted CS: 026360 Data accepted PS: 0954 Spill number: 53	unce id: 944           429524189           Port 12 - PCCORE15           errors           gecore13           errors           Hill level           24%           CPUI           24%           Hill level           24%           Data accupted C5: 0	Data detail Data accept Port 13 - PCCORE16 errors Decement in errors Difference Data accept errors Data accept errors errors Data accept errors Data accept errors errors errors Data accept errors errors errors Data accept errors error	ed PS: 544712032 Port 14 - PCCORE17 errorr Protection Participation errorr PH Insynt CPU - O Memory - O Holds: accepted CS: Sala accepted	Data detail Port 15 - PCCORE18 Ode Status GUI: System overview: all nodes of hardw builder

excluding of front-end modules into DAQ and reloading of frontend modules