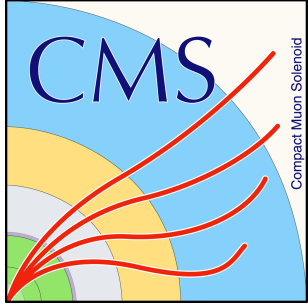
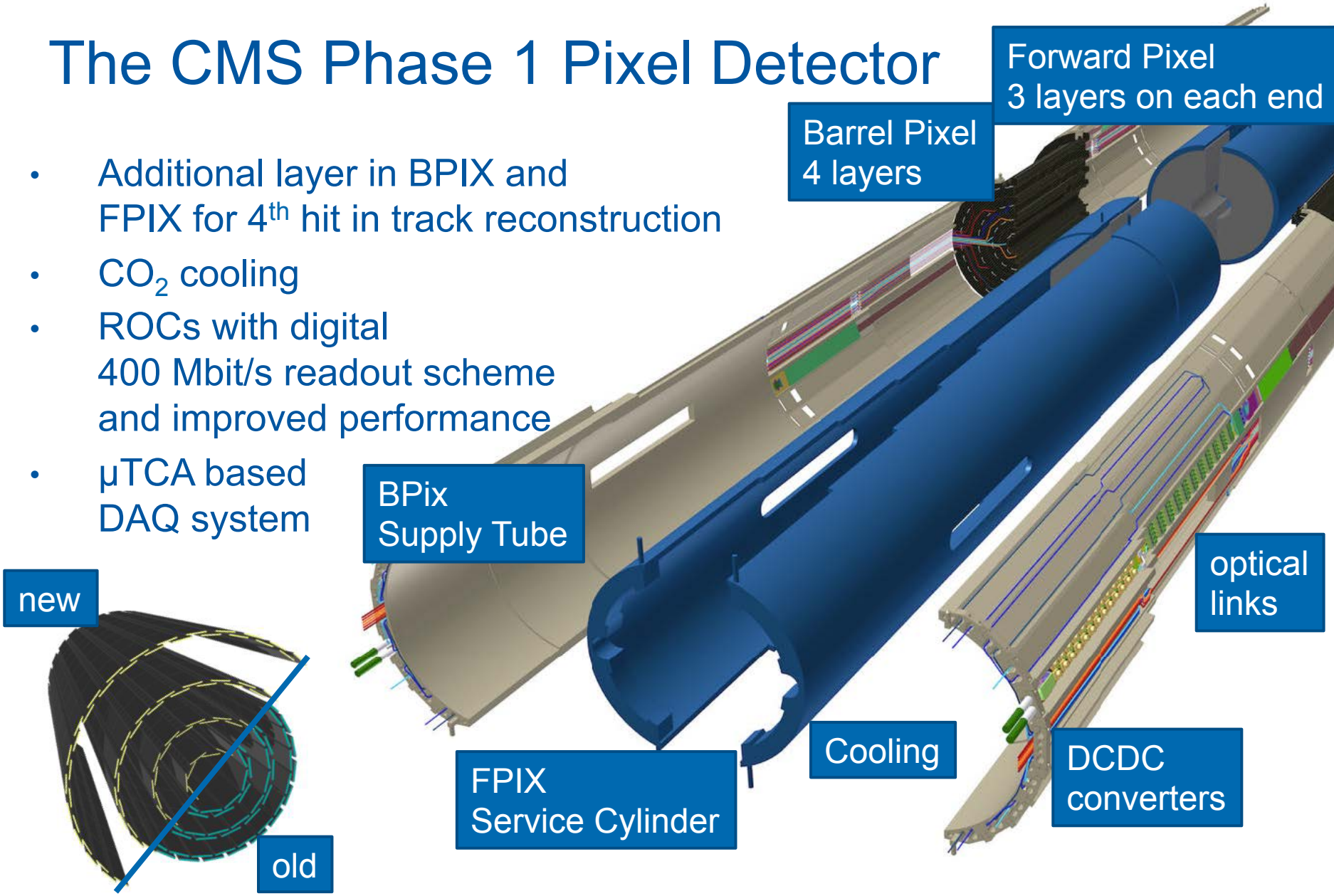


Integration of the CMS Phase 1 Pixel Detector

Andreas Kornmayer for the CMS Tracker Collaboration

The CMS Phase 1 Pixel Detector

- Additional layer in BPIX and FPIX for 4th hit in track reconstruction
- CO_2 cooling
- ROCs with digital 400 Mbit/s readout scheme and improved performance
- µTCA based DAQ system



Strategies in the CMS Pixel Phase 1 Upgrade

Evolutionary Upgrade
(when possible)

- As little changes as possible
- Keep existing working systems

→ Introduce less points of failure for the entire project

→ Already have an existing group of experts

Examples:

- PSI46dig front-end readout chip
- Modules
- Software
- Cooling

Full Overhaul
(if needed)

- New approaches to problems
- New technologies

→ More freedom in system implementation

→ Larger chance for complete failures, backup not always a possibility

Examples:

- PROC600 front-end readout chip
- µTCA DAQ backend
- Powering scheme

Strategies in the CMS Pixel Phase 1 Upgrade - Example

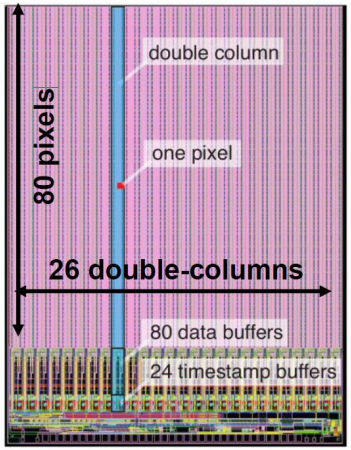
Evolutionary upgrade: PSI46digV2.1respin

Keep form factor…

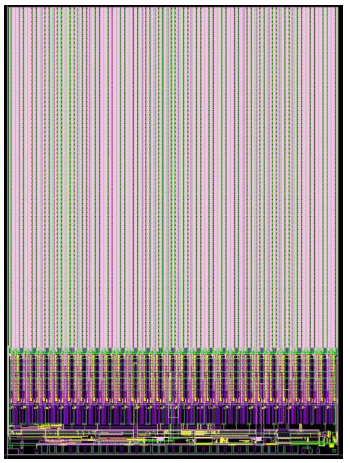
- pixel size 100µm x 150µm
- 4160 pixels/ROC
- pin-out unchanged
- same 285µm n^+-in-n sensors as Phase 1

…but still make improvements

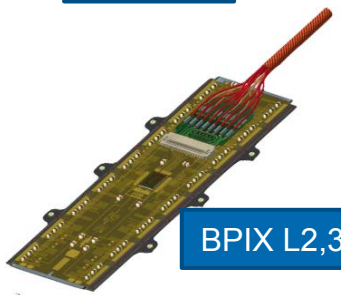
- All modules in detector have the same size→2x8 readout chips
- Faster 400 Mbit/s **digital readout** scheme
- **Deeper buffers** → Higher hit rate capability up to 120MHz/cm^2
- Lower thresholds



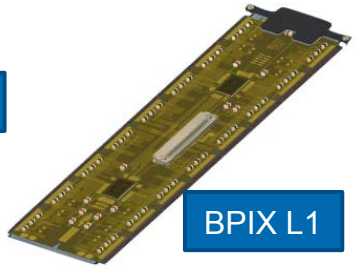
PSI46dig



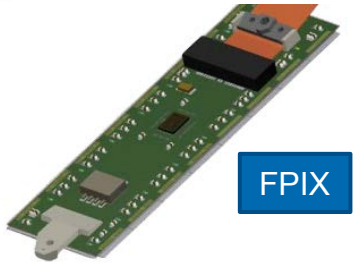
PROC600



BPIX L2,3&4



BPIX L1



FPIX

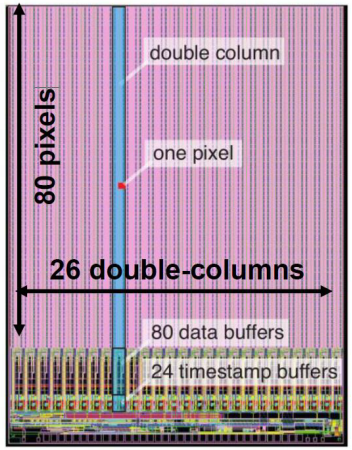
Strategies in the CMS Pixel Phase 1 Upgrade - Example

Overhaul: PROC600

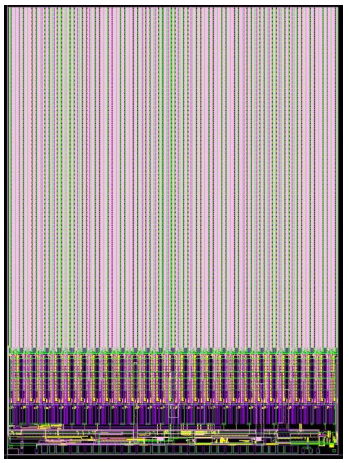
Keep form factor…

- pixel size 100µm x 150µm
- 4160 pixels/ROC
- pin-out unchanged
- same 285µm n^+-in-n sensors as Phase 1

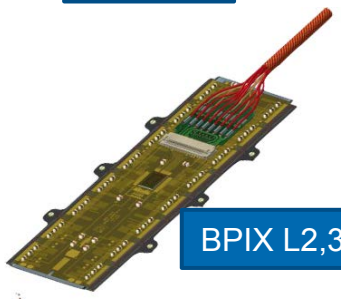
  …but make significant improvements
- Faster 400 Mbit/s **digital readout** scheme
- Completely reworked readout architecture:
  Dynamic Cluster Column Drain Architecture
  → Transfer cluster of 2x2 pixel hits instead of single pixel hits
- Increased radiation hardness for Layer 1



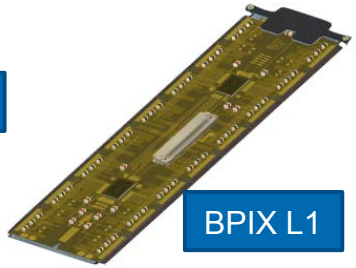
PSI46dig



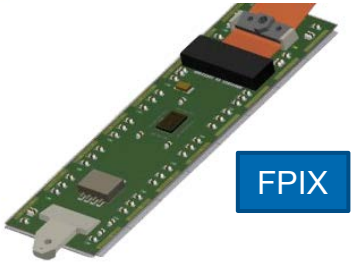
PROC600



BPIX L2,3&4

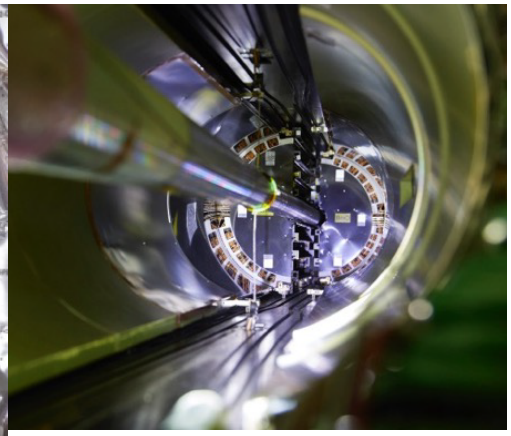


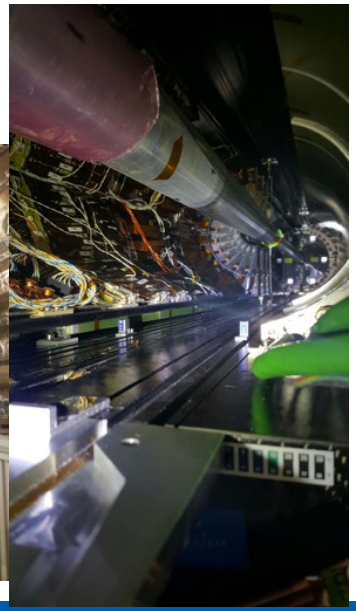
BPIX L1



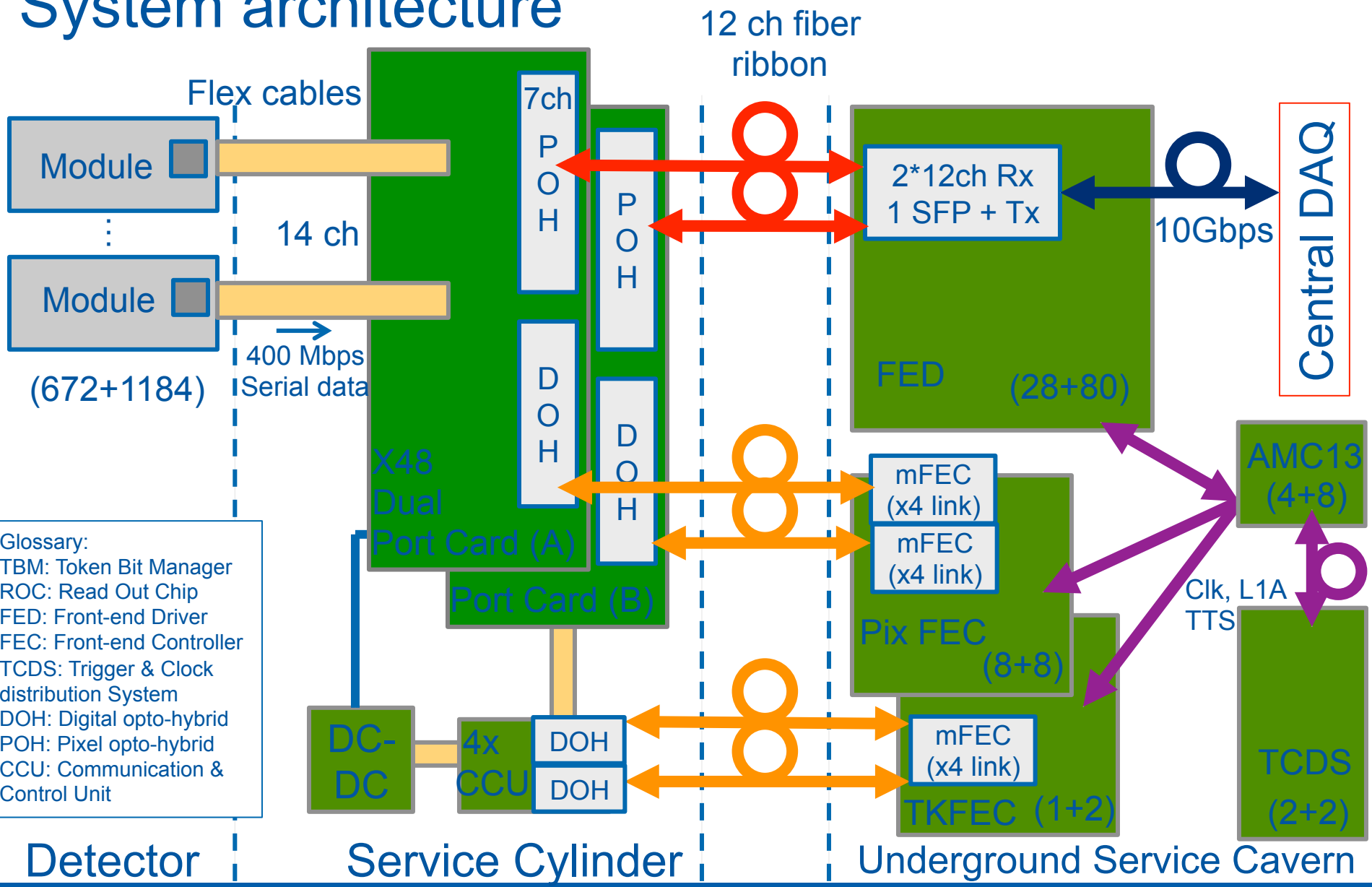
FPIX

The CMS Phase 1 Pixel Detector Installation





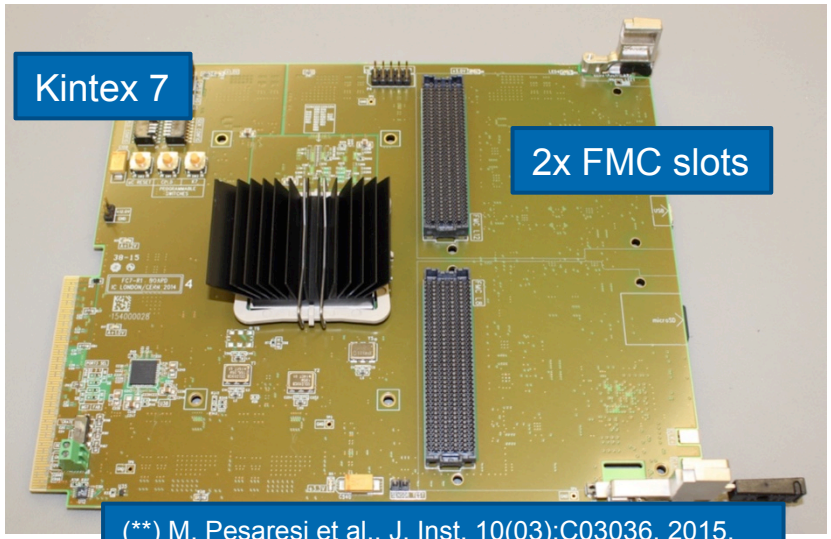
System architecture



DAQ Back-End Upgrade

Idea: Build a new DAQ system, using **standard (commercial) parts** and already **existing hardware**, build **custom electronics** only when necessary

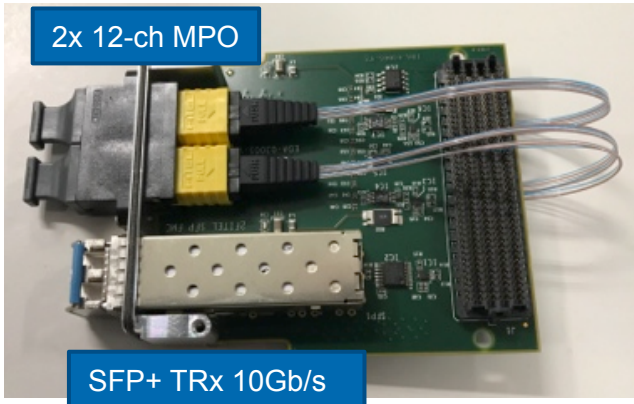
- µTCA standard crates with modified backplane
- Front-end drivers (FEDs) and front-end controllers (FECs) based on **FC7 board**
  - full size, double width µTCA AMC
  - common standard in CMS (TCDS, HCAL, CT-PPS)
  - Kintex 7 FPGA
  - FMC and firmware decides purpose of card
- Connection to TCDS system via **AMC13** card

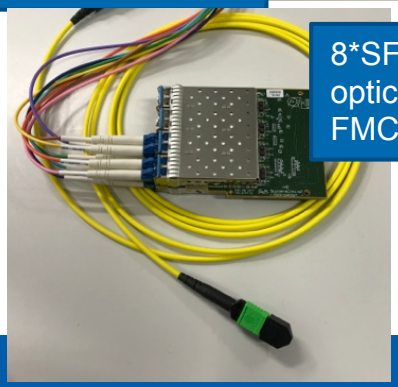


FED

FEC

2x





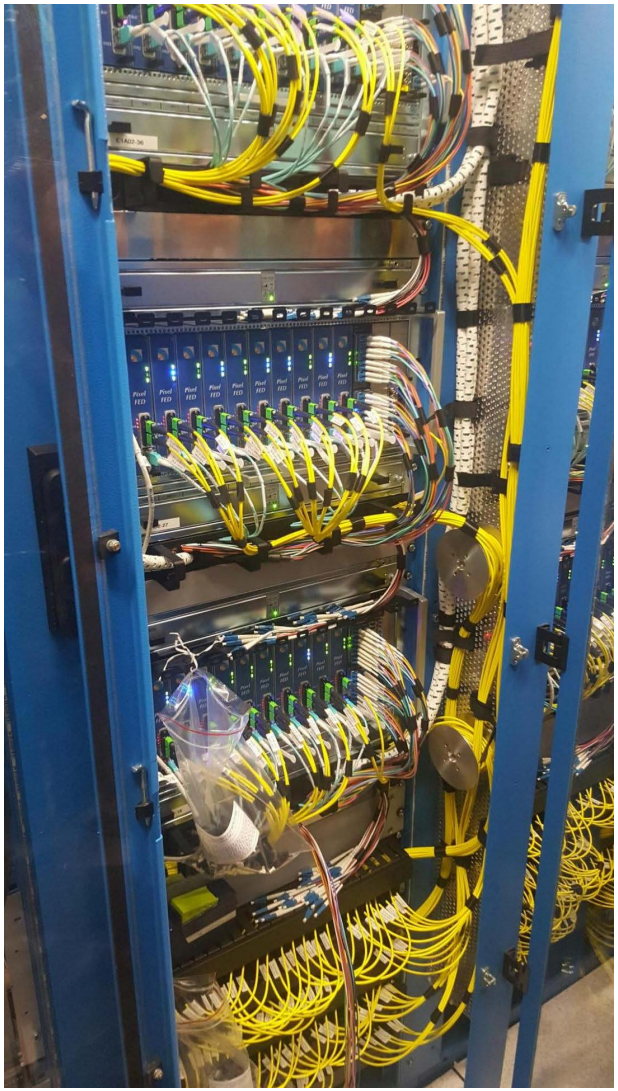
(**) M. Pesaresi et al., J. Inst. 10(03):C03036, 2015.

DAQ system implementation

- **12 µTCA crates** in 3 racks to hold all components of the DAQ backend
  - 108 FEDs
  - 16 PxFECs + 3 TkFECs

  → 2368 optical links

  + spares
- Separated into 1 rack for FPIX and 2 racks for BPIX
- 1Gb/s Ethernet network access to all cards in one crate through **MCH** (MicroTCA Carrier Hub)
- Powered by AC/DC converters
  - **2 redundant power modules** per crate
- Patch panels for 12-fibre optical cables coming from the detector (MPO connectors)



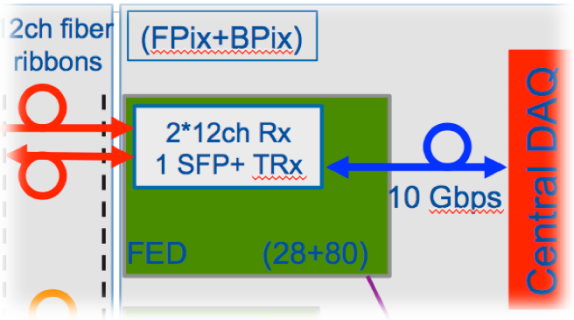
Critical Path for the Upgrade of the DAQ Back-End

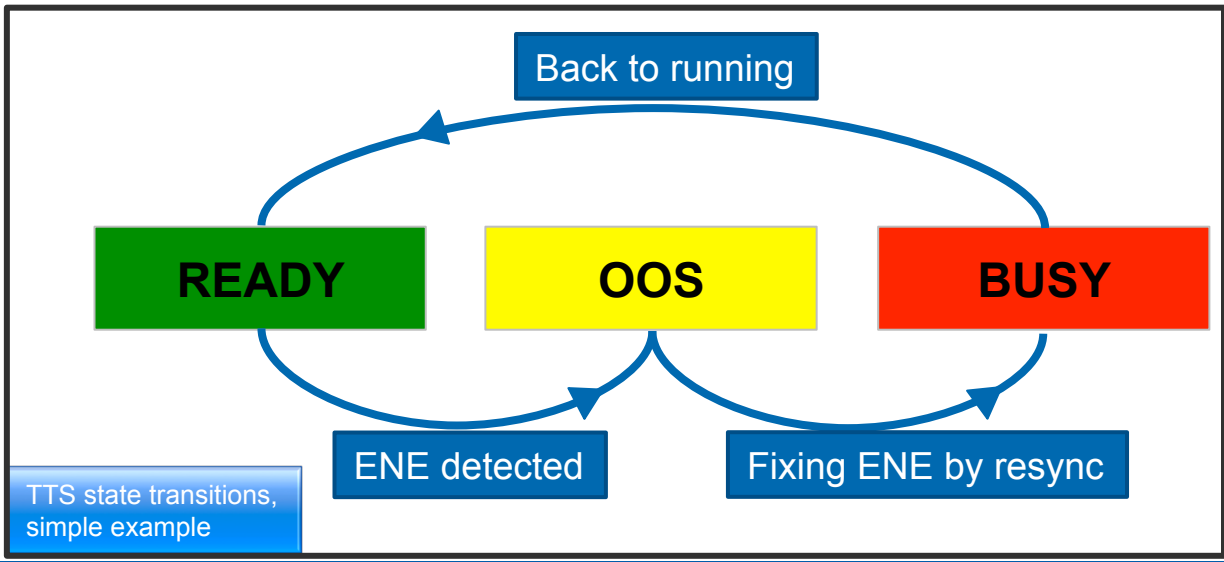
First Prototype FED & FEC	• **Prototype FED and FEC** hardware and first firmware versions that program and read-out a single module
FED&FEC in lab test stand	• Firmware advanced enough **to test front-end production modules**
Pilot Blade on µTCA back-end	• FED firmware **data throughput** fast enough for multiple channels with data from **demonstrator detector** installed in CMS • FED can **handle erroneous data from front-end**, 'real world' application
Start large scale production of cards	**DAQ soak test** • Produce and test enough good hardware for the full DAQ back-end
Installation	
Detector commissioning	• System ready **to test the full front-end detector** installed in CMS • All DAQ back-end **hardware installed**
First beam	• Firmware and software ready to run and process full Pixel detector data load at max. trigger rates and high inst. luminosity

Pixel Phase 1 DAQ – The FED

- Fully functional FED delivered at time of DAQ system installation, yet **development is ongoing!**
- The **FED receives and decodes data** coming from the front-end and **builds events** that are send to central DAQ of CMS
- FED needs to be able to handle all kind of errors
  - Event Number Error (ENE)
  - Missing ROCs
  - Missing event trailers
  - PKAM event
  - Overflow
  - Timeouts

- Lost synchronization
- misinterpreted data
- missing data
- very large events





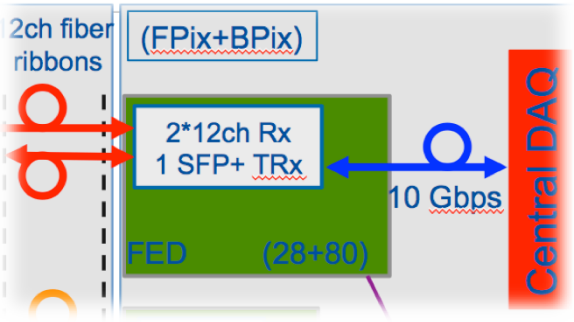
Pixel Phase 1 DAQ – FED Monitor

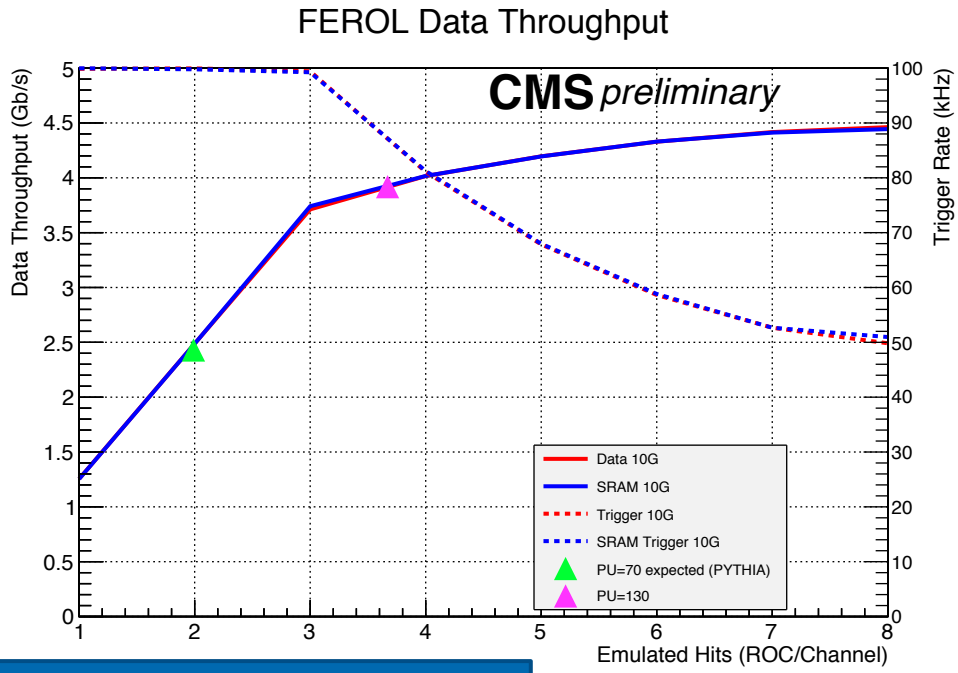
Developed a stand-alone XDAQ application to monitor Pixel FED status continuously
→Collects statistics about **TTS state** transitions
→Status of the connected modules.

- Error statistics on modules are collected by each FED and monitored by software
- Repeated offenders producing too much dead-time by requesting re-syncs or blocking triggers are eventually **masked** on module level
- Global dead-time caused by the Pixel detector has been significantly decreased since first operations

Pixel Phase 1 DAQ – FED Data Throughput

- Ongoing development!
- FED data throughput on 10Gbit/s optical Ethernet links via Slink protocol currently reaches only ~4.5 Gbit/s
  →Only becomes bottle neck if LHC running conditions change drastically
  →Good until pile-up of 130 under current conditions
- Firmware development ongoing to make full use of available link bandwidth by an **improved parallel FIFO draining scheme**





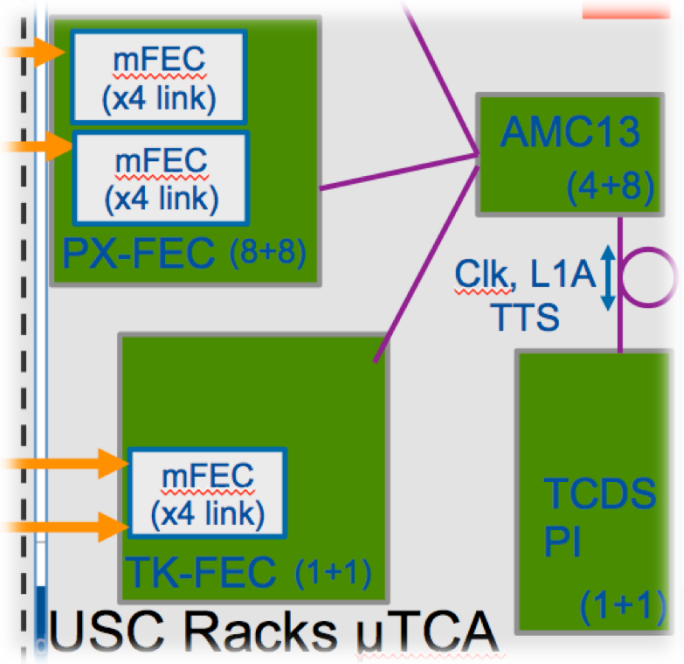
More info on Poster from Matthew Kilpatrick "FED Firmware Interface Testing with Pixel Phase 1 Emulator"

Pixel Phase 1 DAQ – The FECs and AMC13

Pixel FEC and Tracker FEC are fully functional but some desirable features are still under development

PixFEC development

- Move to **Vivado** synthesized fw version – DONE
- Storage of detector configuration in FC7 memory/SD card
  → Saves transfer time from software
  First firmware implementation under test
  → could make way for direct FED/FEC communication



TkFEC development

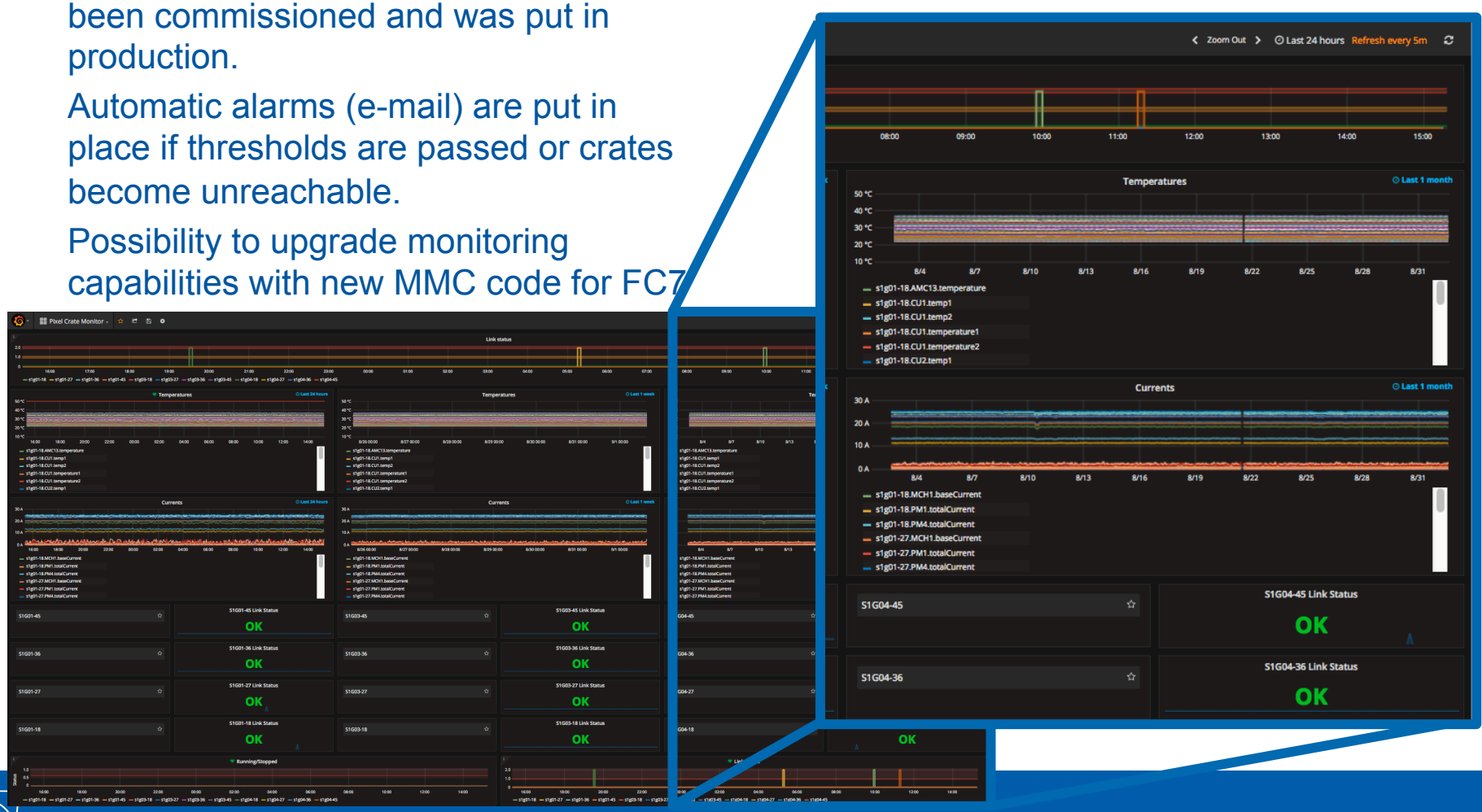
- Sometimes communication to CCU ring is lost → Needs reset
- Speed up of I^2C communication with devices might cure problem

AMC13 improvements

- Optimizations made to settings
  →Deadtime reduction on resyncs and event counter resets

System Monitoring

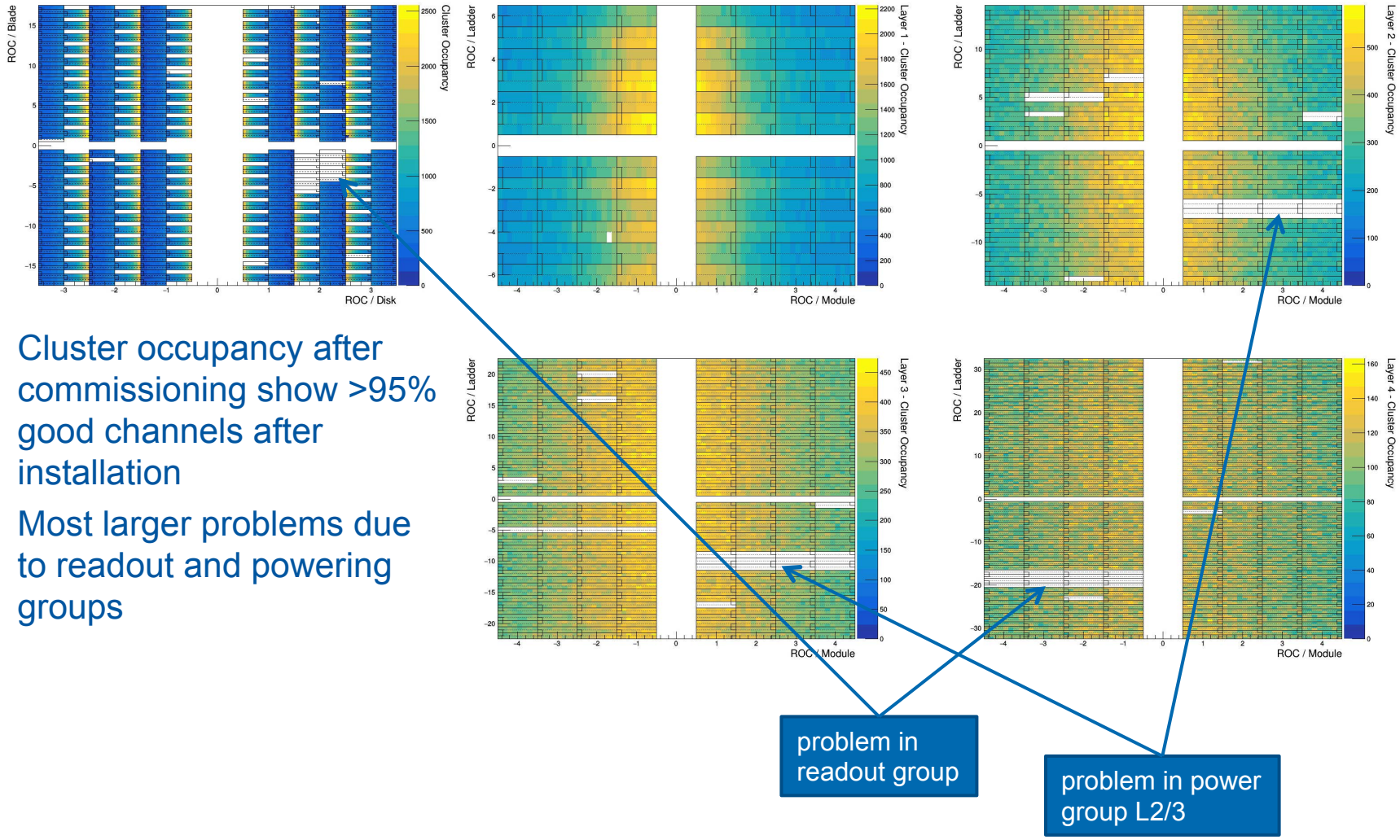
- Basic live signs like voltages, currents, temperatures, and network connection of the system are constantly monitored.
- New **Grafana** based monitoring website has been commissioned and was put in production.
- Automatic alarms (e-mail) are put in place if thresholds are passed or crates become unreachable.
- Possibility to upgrade monitoring capabilities with new MMC code for FC7



Pixel Phase 1 DAQ – Software

- Evolutionary upgrade of Pixel Online Software (POS)
- General software architecture kept, underlying hardware access libraries adapted to IPBus communication with FC7 cards
- Fully functional since beginning to operate and calibrate detector
  →Collected operational experience in 2016 with Pilot Blade demonstrator and test stands
- Software development now focusing
  - Parallelization
    Software 'supervisors' run on crate level, most noticeable during start and stop of run
    →Gain factor 12 by running processes parallel
    →Deadtime reduction at beginning/end of run
  - SEU recovery
    'Misbehaving' channels need to be reconfigured
    Software tracks of number of errors seen and fixed, and reconfigured channels in FED
    Some channels need a power cycle to recover from SEU
    → Now also automatized in software

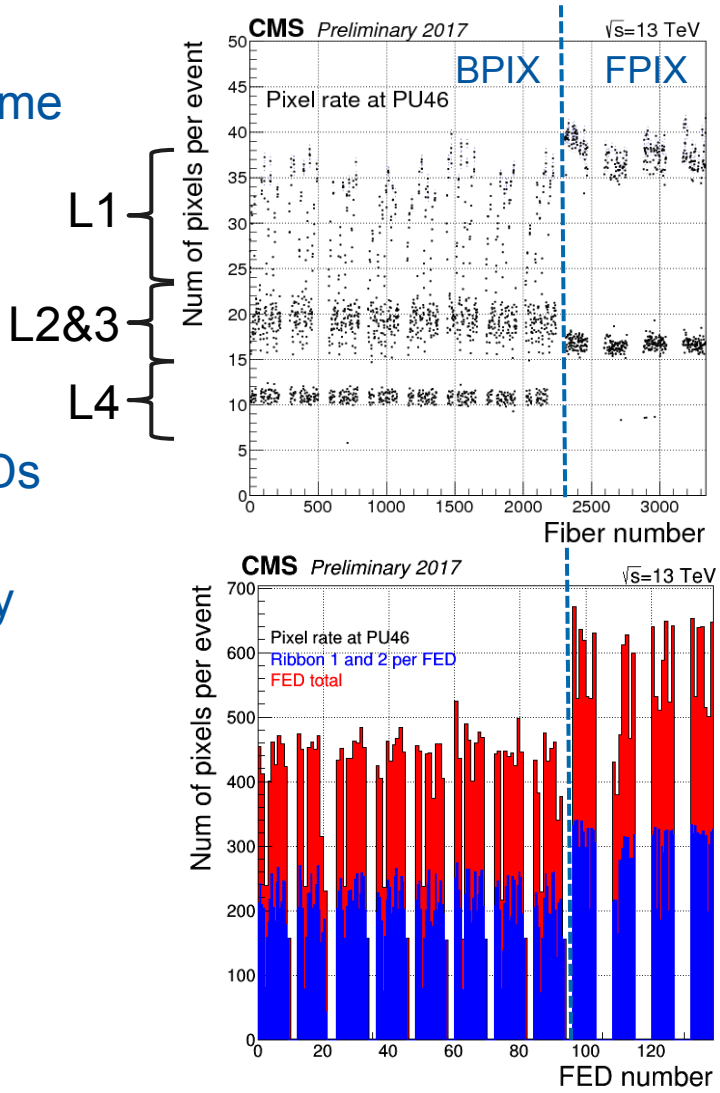
Detector Performance – Cluster occupancy



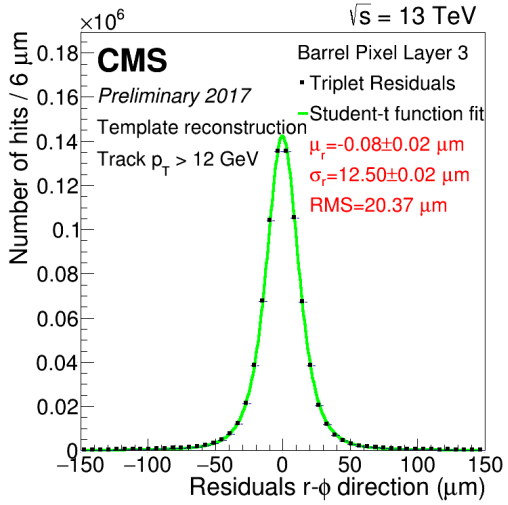
- Cluster occupancy after commissioning show >95% good channels after installation
- Most larger problems due to readout and powering groups

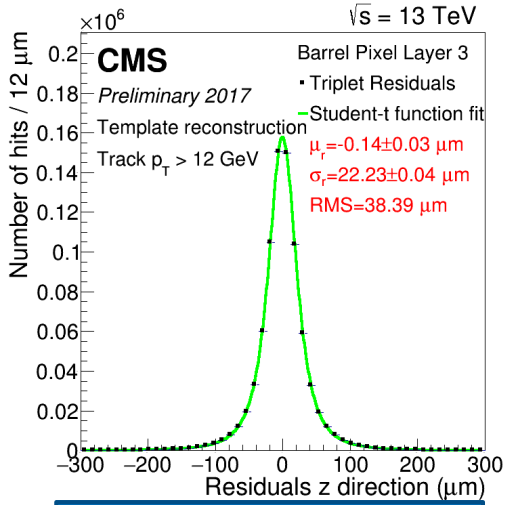
Detector Performance – Data load on DAQ system

- Data load on single optical fiber varies greatly even among channels from the same layer
- Load balancing necessary
  →Implemented on auxiliary electronics
  →Freedom of connecting fiber channels freely on detector back-end
- Uniform data rate achieved across all FEDs in the DAQ system
- Few FEDs have lower data rate since only ½ the channels are connected for them

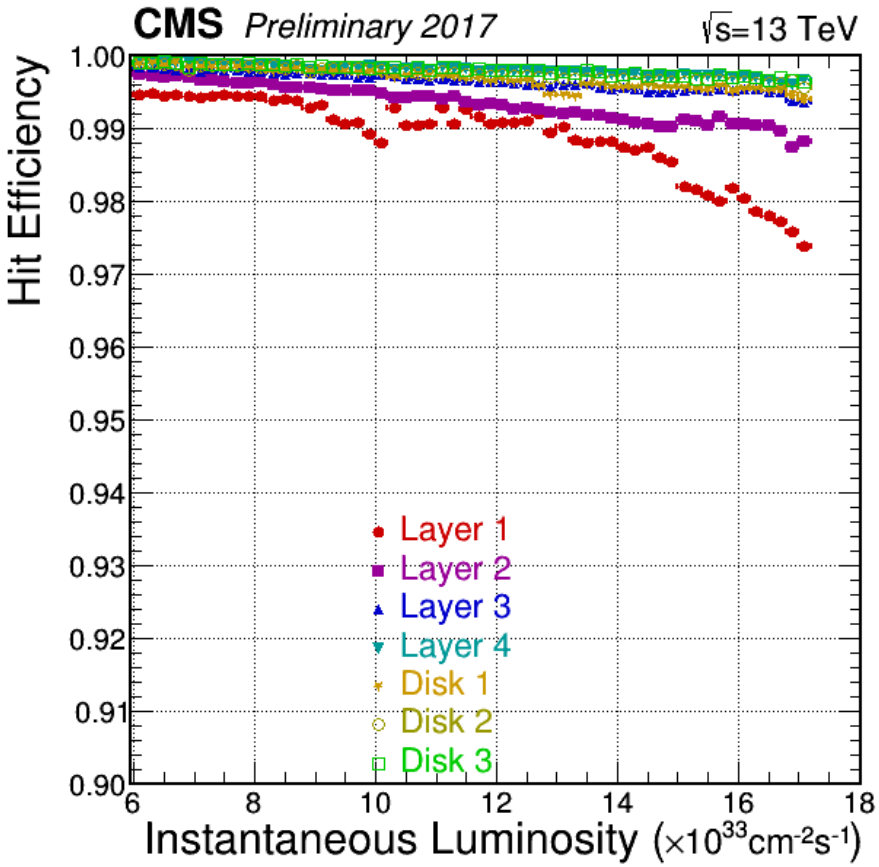


Detector Performance – Tracking & Hit Efficiency





Residuals Layer 3



Hit efficiency

Summary

- New CMS Pixel Detector and DAQ system installed in EYETS 2016/2017
- Successful evolutionary upgrade of front-end and software and complete replacement of DAQ back-end
  → New detector operational for commissioning and first collisions
- Detector shows good performance
  → Fraction of active channels >95%
  → Small residuals
  → High hit efficiency in all layer
- Further development on increasing data throughput rate in FED, faster programming of front-end by FECs and software functionalities

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