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# Integration of the CMS Phase 1 Pixel Detector

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During the extended year-end technical stop 2016/17 the CMS Pixel Detector has been replaced. The new Phase 1 Pixel Detector is designed for a luminosity that could exceed L = 2x10ˆ34 cmˆ-2 sˆ-1. With one additional layer in the barrel and the forward region of the new detector, combined with the higher hit rates as the LHC luminosity increases, these conditions called for an upgrade of the data acquisition system, which was realised based on the mircoTCA standard. This contribution focuses on the experiences with integration of the new detector readout and control system and reports on the operational performance of the CMS Pixel detector.

## Summary

During the second running period of the LHC (RUN2) it is anticipated that the instantaneous luminosity will reach and exceed L = 2x10ˆ34 cmˆ-2 sˆ-1. The Compact Muon Solenoid (CMS) Phase 0 Pixel Detector and its front-end readout chip were designed for half of this value resulting in increased dead times and random data loss at the expected hit rates.
During the extended year-end technical stop 2016/17 the entire CMS Pixel Detector has been replaced. Compared to the old detector the Phase 1 Pixel Detector has one additional layer in the barrel and the forward region. It is built from four layers in the barrel part and three disks at each end.
A new powering layout using DC/DC converters positioned at a high eta value and the switch to a CO2 based cooling system greatly reduced the material budget of the detector in its sensitive region.
The front-end readout chips (ROCs) have either undergone an evolutionary upgrade like the PSI46dig chip used in layer two to four and the forward disks, or have been completely redesigned like the PROC600 used in the first layer of the barrel part.
The switch to a 400Mb/s digital data transmission scheme coming from each of the 2368 optical front-end readout links also called for a complete redesign of the data acquisition system (DAQ). In the new microTCA based DAQ system the front-end controllers and front-end drivers are implemented on the custom made FC7 card equipped with special receiver or transceiver mezzanine cards.
This contribution will give an overview over the design of the Phase 1 CMS Pixel Detector and its new DAQ system, focusing on the integration of the readout system in the scope of the CMS experiment and report on first operational experiences and the overall performance of the new detector.

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