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A Real-Time Demonstrator for Track Reconstruction in the CMS L1 Track-Trigger System Based on Custom Associative Memories and High-Performance FPGAs

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A Real-Time demonstrator based on the ATCA Pulsar-IIB custom board and on the Pattern Recognition Mezzanine (PRM) board has been developed as a flexible platform to test and characterize low-latency algorithms for track reconstruction and L1 Trigger generation in future High Energy Physics experiments. The demonstrator has been extensively used to test and characterize the Track-Trigger algorithms and architecture based on the use of the Associative Memory ASICs and of the PRM cards. The flexibility of the demonstrator makes it suitable to explore other solutions fully based on high-performance FPGA devices.

Summary

The increase of the luminosity to 5×1034 cm−2 s−1 expected in the Large Hadron Collider after the upgrade scheduled for 2025 will bring the number of minimum bias interactions per bunch crossing to about 140. This would generate an unmanageable increase in the trigger rate. To keep the trigger rate below 1MHz, a value compatible with bandwidths in data transfers and processing power of trigger systems, we proposed the introduction of data reduction based on low-latency (<5us) track reconstruction from high-resolution Silicon Tracker information. Only data associated to high-Pt tracks (e.g.: tracks with energy >3GeV => 3% of the tracks) would be propagated to the L1 Trigger system.

Several groups studied different algorithms for track reconstruction through high-level simulations during the last years. Hardware implementations have been validated using real-time demonstrators based on "off-the-shelf"and custom components. We focused on algorithms that take advantage of a preliminary data reduction obtained filtering out "hits"that do not belong to "interesting"tracks that are associated to patterns stored in high-density Associative Memory (AM) custom devices. Algorithms are implemented in a high performance FPGA. They perform a further data reduction in the Track Candidate Builder (TCB) and they extract the Track parameters in the Track Fitter (TF).
We developed a proof-of-concept real-time demonstrator based on the Pattern Recognition Mezzanine (PRM) board, a custom board housing a set of AM ASICs (12 x AM06 in the version that produced the results that will be presented) and on a Xilinx Kintex UltraScale FPGA device where the TCB and TF are implemented. As host board we used the Pulsar-IIB board, a custom board developed at FNAL compatible with a full mesh high speed ATCA backplane. This board provides an ideal powerful building block for the development of scalable architectures requiring flexible high bandwidth board-to-board communications. Each board is equipped with two high-performance Xilinx Virtex-7 FPGA devices and four FMC connectors that allow the integration with custom or "off-the-shelf"mezzanine boards as the PRM board. The host PC uses a Gbit Ethernet link to control and monitor the demonstrator. IPBus protocol is used to access control and status registers and FIFOs. Input FIFOs are used to store patterns that will be pre-loaded into AM ASICs via JTAG and hits that will be transmitted to the PRM FPGA via high-speed (up to 10 Gbps/link) serial links (3 links/connector) to emulate Tracker data. Output FIFOs collect track parameters from the PRMs.
The final goal was to evaluate the system performance (e.g.: latency and efficiency in data filtering), to identify any necessary modifications to match bandwidth and latency constraints and to validate the component selec-

tion. System architecture, test results and figures of merit obtained with sets of data associated to physically relevant events will be presented. The entire SW/FW platform of our demonstrator is available to hardware and firmware developers interested in having a flexible and ready-to-use environment for the validation of other algorithms or hardware solutions.

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