Contribution ID: **98** Type: **Oral**

FELIX: the New Detector Readout System for the ATLAS Experiment

Tuesday 12 September 2017 14:50 (25 minutes)

Starting during the upcoming major LHC shutdown (2019-2021), the ATLAS experiment at CERN will move to the Front-End Link eXchange (FELIX) system as the interface between the data acquisition system and the trigger and detector front-end electronics. FELIX will function as a router between custom serial links and a commodity switch network, which will use industry standard technologies to communicate with data collection and processing components. This presentation will describe the FELIX system design as well as reporting on results of the ongoing development program.

Summary

The upcoming ATLAS upgrade program, to be implemented in the next major LHC shutdown (2019-2019), requires a Trigger and Data Acquisition (TDAQ) system able to trigger and record data at luminosities up to three times the original LHC design value. At the same time new on detector electronics technologies will be introduced to ATLAS readout for the new Muon Small Wheel detector, as well as the Liquid Argon (LAr) Calorimeter and Calorimeter Trigger upgrades. These new systems will make use of newer readout link technologies, including high bandwidth FPGA-to-FPGA protocols and radiation-hard Giga Bit Transceivers (GBT), providing up to 42 logical links within one fibre. In order to connect these new systems and handle the significantly increased data volumes in a detector agnostic and easily scalable way a new readout architecture, named the Front-End LInk eXchange (FELIX), has been designed.

FELIX receives and identifies different information streams on its incoming links and routes packets to client processing applications via a commercial switched network. In the opposite direction, FELIX receives packets from the network and forwards them to specific on-detector modules. Another task for FELIX is to handle input from the Time, Trigger and Control (TTC) system to recover the LHC clock and to forward synchronous trigger information to on-detector electronics over low-and-fixed-latency GBT links.

All functions described above are implemented in FPGAs hosted on PCIe interface cards, which are hosted within commodity server PCs. Feature design and subdetector interface testing is taking place using a Xilinx VC-709 development card. The VC-709 is equipped with an 8 lane PCIe Gen3 (64 Gb/s) interface and four SFP+ transceivers for optical connectivity. A custom FMC mezzanine has been designed to receive and decode the TTC clock and information stream and provide clock jitter cleaning. Drivers and software tools have been developed to test and configure these boards both for internal development purposes and use in subdetector test systems. Data routing and connectivity to a COTS (Commercial Off-The-Shelf) network is implemented in a software pipeline running on the FELIX host PC. It has been verified the packet processing performance of the design satisfies ATLAS readout requirements for 2021.

The final implementation of FELIX will make use of a custom built PCIe board with a Xilinx Kintex UltraScale FPGA, a 16 lane Gen3 PCIe interface and 48 bidirectional optical interfaces in the form of eight Mini-POD transceivers (max. link speed 14 Gb/s). The optical links, PCIe interface, and TTC decoding circuits of the prototypes of this board have been verified to function well. Integration testing with the complete FELIX firmware and software is ongoing. In this presentation the FELIX system will first be introduced, before further details are given of ongoing development and performance testing.

Primary author: STAMEN, Rainer (Ruprecht-Karls-Universitaet Heidelberg (DE))

Presenter: SCHREUDER, Frans Philip (Nikhef National institute for subatomic physics (NL))

Session Classification: Trigger

Track Classification: Trigger