AN FPGA-BASED TRACK FINDER FOR THE L1 TRIGGER OF THE CMS EXPERIMENT AT HL-LHC

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on behalf of CMS and TMTT collaborations

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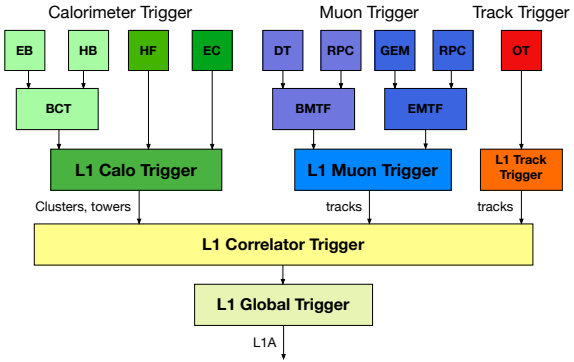
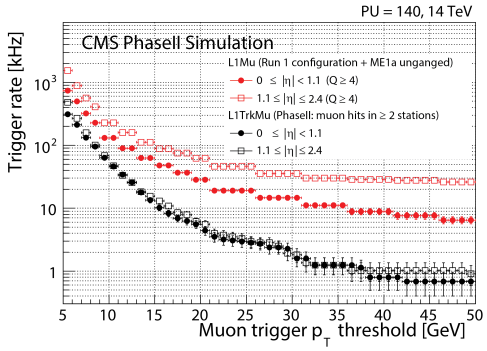
PHASE II CMS UPGRADE

- Major **upgrade** of experiment for HL-LHC (post-2025)
  - Tracker and forward calorimeter replacement (radiation damage)
- **Level-1 trigger** upgrades
  - up to 200 pileup collisions/BX (today 40)
  - output bandwidth up to 750 kHz (currently 100 kHz)
  - latency 12.5 μs (now 4 μs)
- **Tracker data** used at Level-1
  - to maintain trigger rate within limit, without affecting performance
  - on detector data rejection needed to reduce input bandwidth into Track Trigger system





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CMS PHASE II TRACKER

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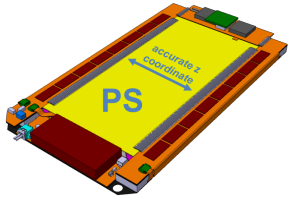
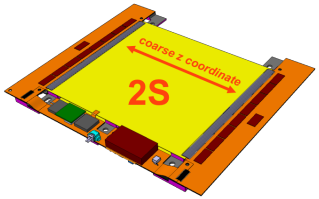
PS modules (20 < r < 60 cm)



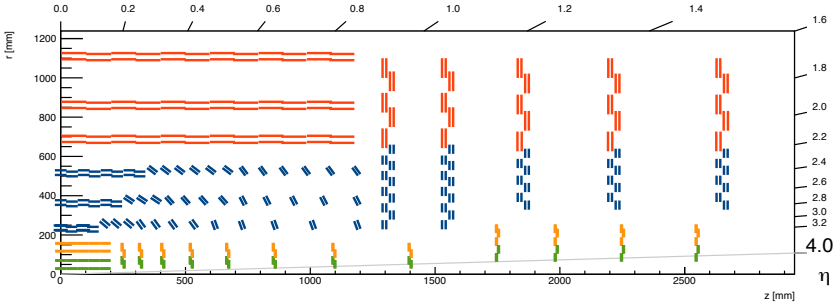
Strip Sensor x2:
2.5 cm x 100 μm
+
Pixel Sensor x32:
1.5 mm x 100 μm

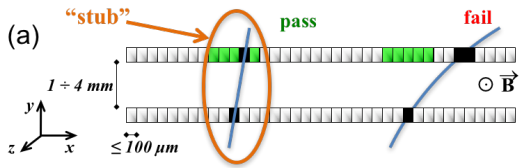
2S modules (r > 60 cm)



Strip Sensor x2:
5cm x 90 μm
+
Strip Sensor x2:
5cm x 90 μm

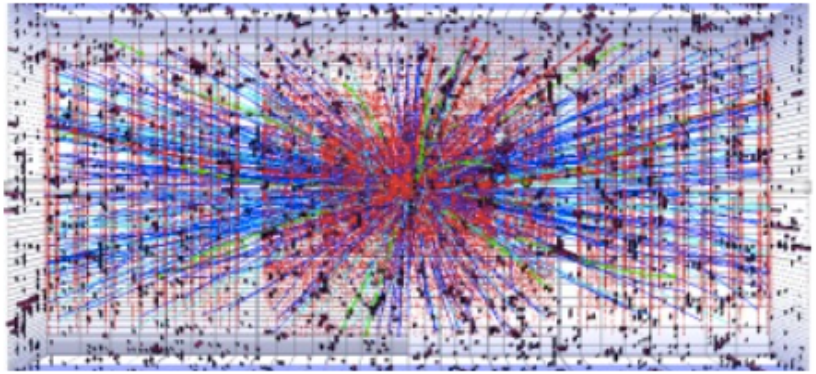
- Presence of **high-p_T tracks** is hint of an interesting physics event
- Novel tracking modules (**p_T modules**) with two separated silicon sensors to discriminate tracks with p_T > 2-3 GeV (**stubs**)
  - On detector data rate reduction O(100)





L1 TRACK TRIGGER

- Task of L1 Track Trigger is to **reconstruct tracks** from charged particles with **p_T > 2-3 GeV**
- Latency budget : **4 µs**
- Very high data-rate: 20.000 stubs per BX at PU200



- We adopt a fully **time multiplexed architecture**
  - Pioneered by the current **L1 Calo Trigger** system
  - Data from **each BX** are processed by a **single processing unit** or node

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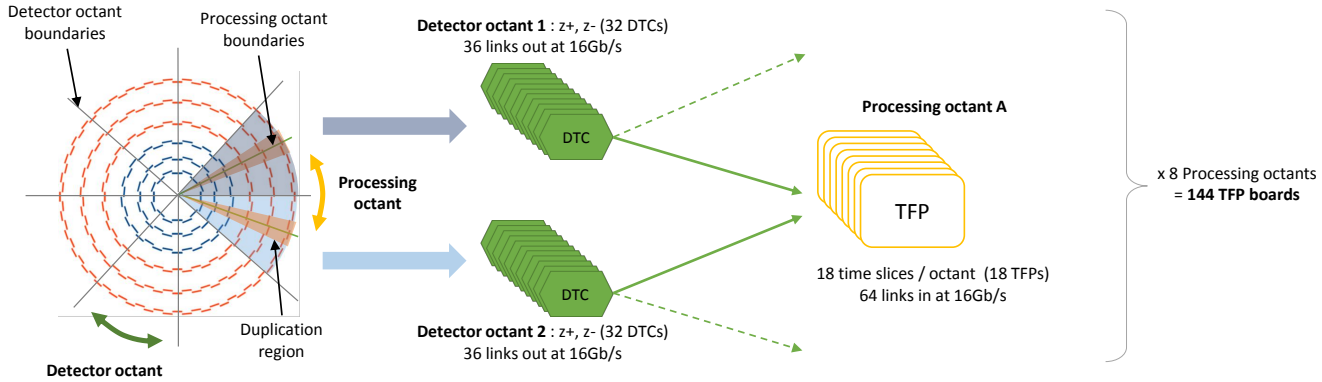
TRACK FINDING ARCHITECTURE

- No FPGA can handle the entire tracker data rate
- Tracker is divided in **octants** across Φ
  - Octant data is readout by **32 Data, Trigger and Control (DTC)** boards
  - To avoid losses at boundaries, each **Track Finder Processor (TFP)** board gets in input data from two detector octant (64 DTCs)
  - Each TFP searches tracks in a **processing octants** (rotation of half octant)
  - Each TFP handles data from **1/8 in Φ and 1/(time multiplexed period)**
  - Baseline **TMP = 18** -> total no. boards needed 18x8 = 144



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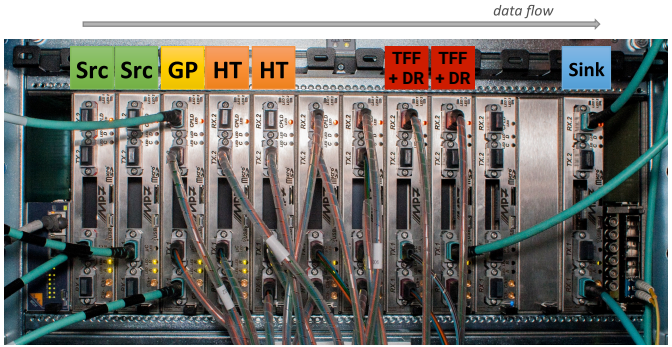
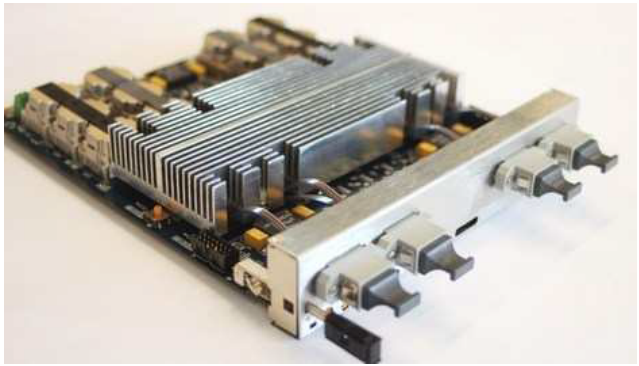
HARDWARE DEMONSTRATOR

- Track Finding capability of the system has to be **demonstrated in hardware**
- An **hardware demonstrator** has been built to prove feasibility and capability of the TFP (**demonstrator slice**)
  - TFP designed to operate independently
- Made of **several MP7 boards**, each one running a different step in the algorithm





Master Processor 7 (MP7)

- Currently used widely in CMS trigger
- Xilinx Virtex-7 690 FPGA
- 72 I/O optical links running at 10.3 Gbps
- Infrastructure fw, providing transceiver buffering, I/O formatting and external communication
  - Separated from algorithm space

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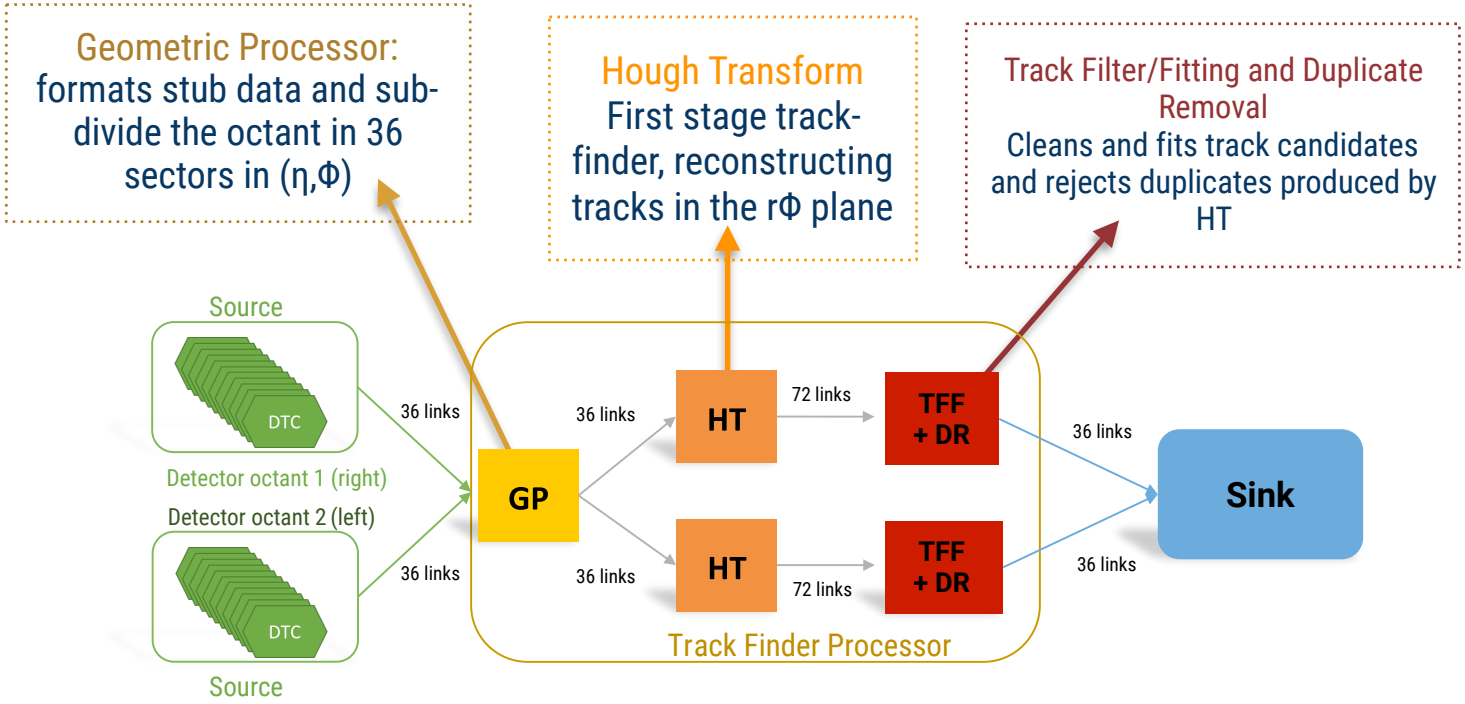
TRACK FINDER PROCESSOR



- A total of **5 boards** are needed to demonstrate track finding functionalities
- 3 boards (**2 sources and 1 sink**) are used to inject and store data from 30 LHC events into the demo chain
- **Separating** the algorithm in blocks facilitates fw development and optimise manpower utilisation

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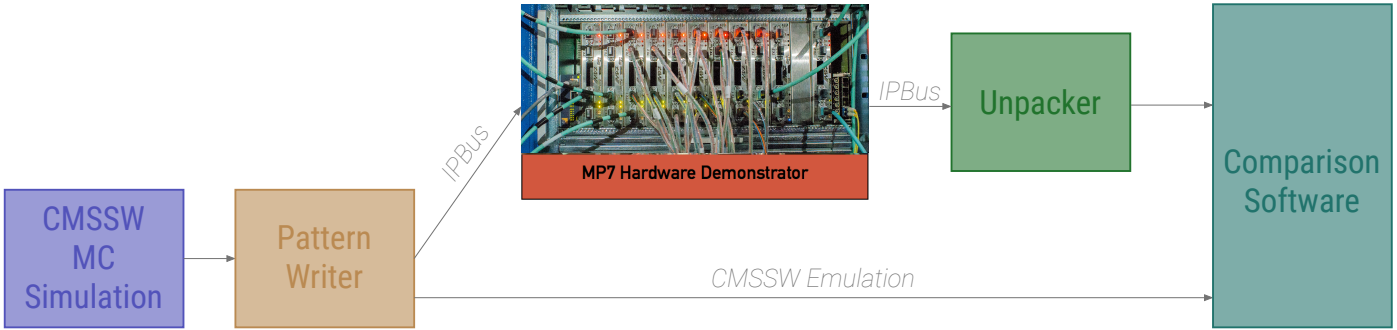
DEMONSTRATOR DATA TAKING

- A series of **software** have been developed to test the demonstrator system
- Feed the demonstrator with **Monte Carlo data from Phase II CMS simulation**
- Hardware results are compared directly with results from **Emulation**
- Up to **30 events** per injection
- Demonstrator slice is octant independent -> coverage of the **entire tracker** acceptance



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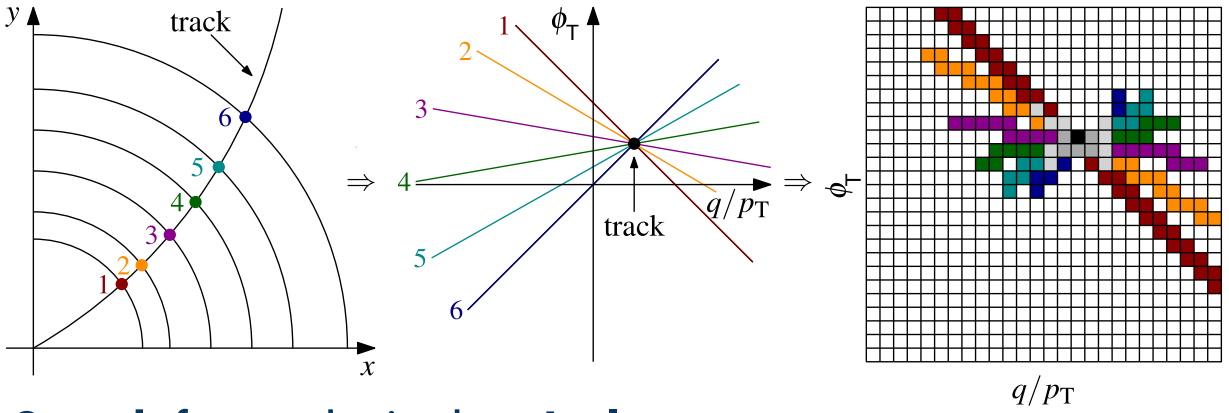
HOUGH TRANSFORM



- **Search** for tracks in the **rΦ plane**
- For tracks with $p_T > 3$ GeV

$$\phi \approx -\frac{q}{p_T} \times r + \phi_0 \quad \rightarrow \quad \phi_0 \approx \phi + \frac{q}{p_T} \times r$$

- Each stub draw a **straight line** in the **parameter space**
- **Accumulation points** correspond to track **candidates**
- **HT space discretised in a 32x64 array q/p_T x Φ_0**
- Firmware implementation described at TWEPP2016
  - M. Pesaresi, An FPGA based track finder at Level 1 for CMS at the High Luminosity LHC

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TRACK FITTING AND FILTERING

- Track candidates out of the Hough Transform contains **spurious stubs** from **pileup** interactions
- Also about **40%** of produced candidates are **fakes**
- **Track filtering stage** is needed in order to **reject fakes** and **clean** tracks
- Two algorithms have been developed

Kalman Filter

- combined fitters/filters
- default offline fit
- incorrect trajectories rejected
- can take into account scattering effects
- mathematically heavy (implemented in MaxJ, see. Summers, TWEPP2016)

Seed Filter plus Linear Regression

1. Seed Filter verifies that HT track candidates draw a **straight line** trajectory on ***rz* plane** and rejects inconsistent stubs
2. Simple Linear Regression calculate track parameters, performing independent straight line fits in ***rΦ* and *rz***

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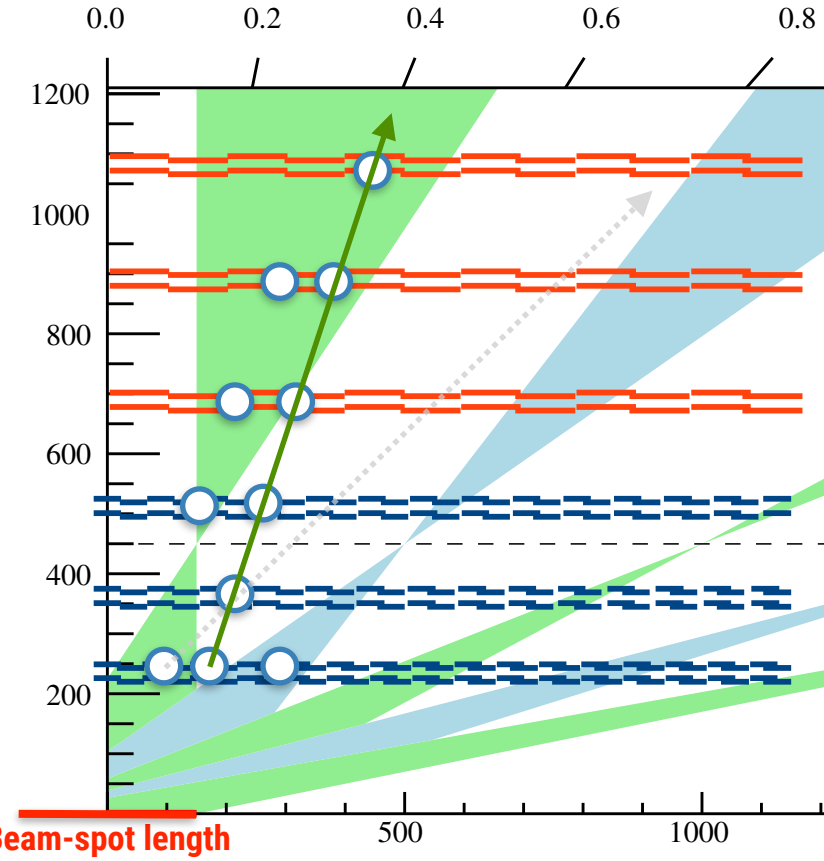
SEED FILTER ALGORITHM

1. **Seed Finder:** computes lines through stubs in PS layers
2. **Seed Checker:** Extrapolates to other tracking layers and rejects incompatible stubs
3. **Seed Comparison:** Keeps the seed with the most layers
4. **Simple Linear Regression:** calculates track parameters, fitting straight lines in *rΦ* and *rz*



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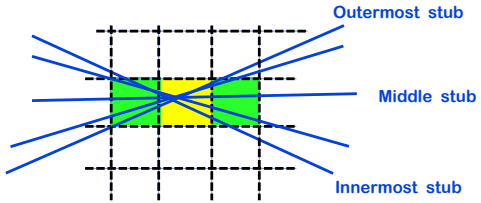
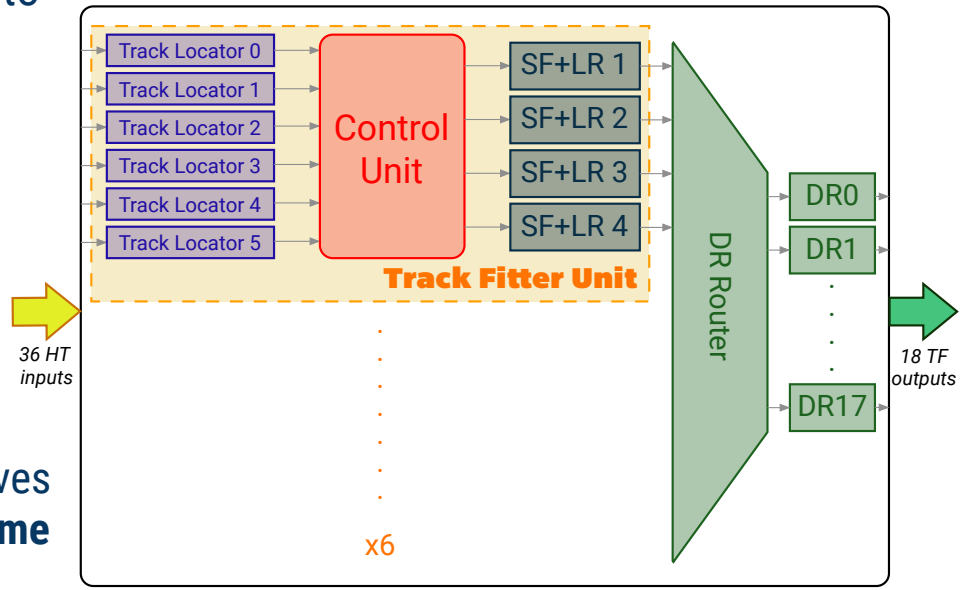
SF+LR FIRMWARE IMPLEMENTATION

- Stubs from each HT output channel are stored in a separate FIFO (**Track Locator**)
- The **Control Unit** distributes HT track candidates to **Seed Filter + Linear Regression** blocks (SF+LR) in a round-robin fashion
- Each Control Unit handles **6 Track Locator** and **4 SF+LR** blocks
- Tracks are then sent to a router block and transmitted to 18 **Duplicate Removal** modules



- Simple DR block removes HT candidates with **same helix parameters**



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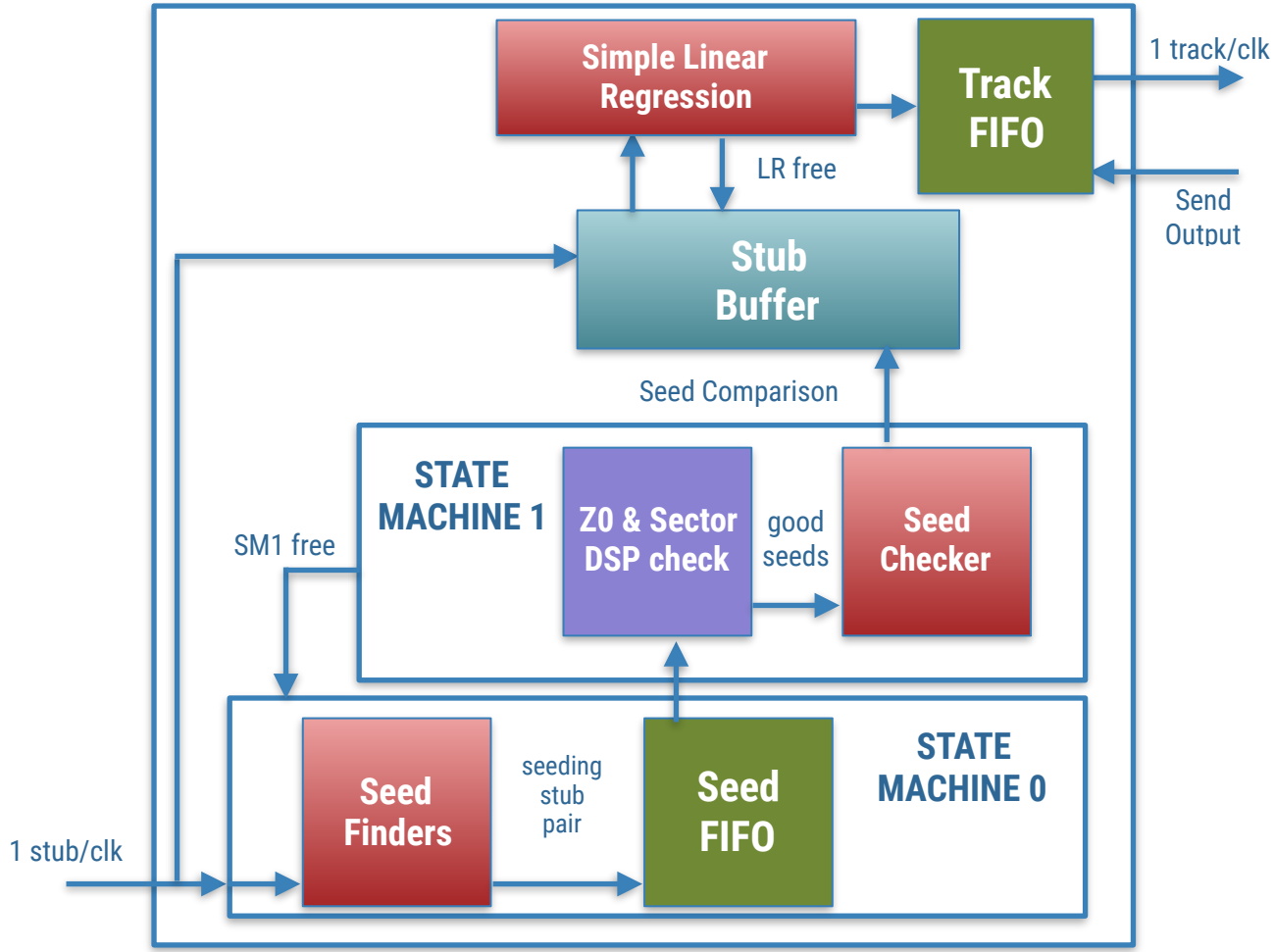
SF+LR MODULE



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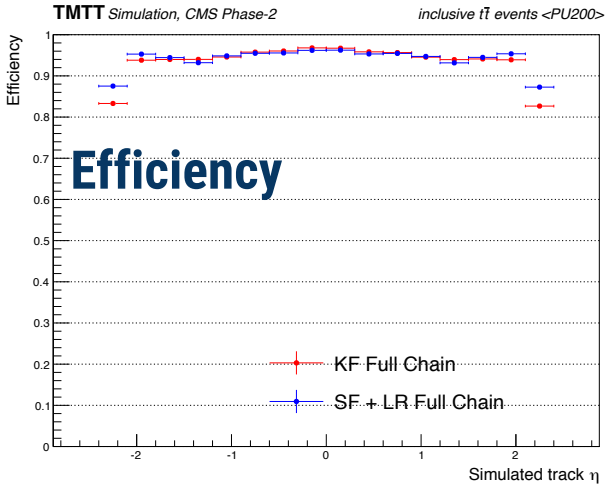
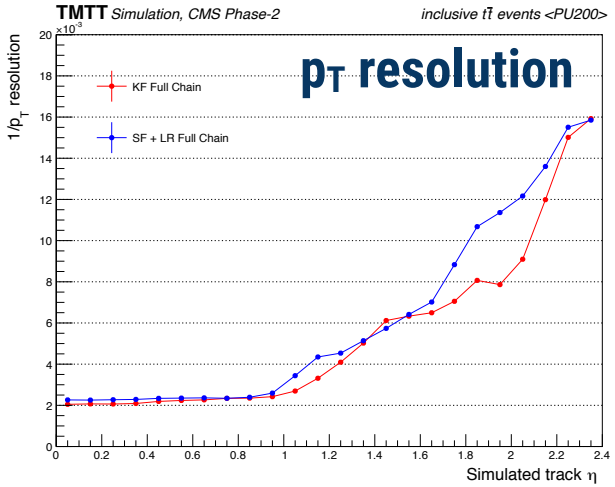
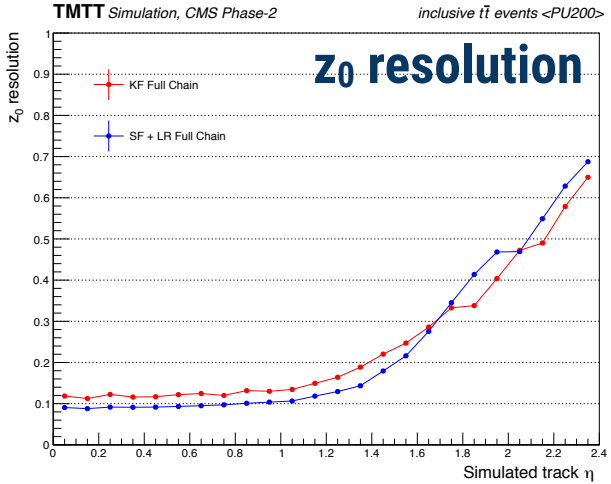
FITTERS COMPARISON







- **Similar performance** for both KF and SF+LR
  - KF: Slightly better rΦ resolution
  - SF+LR: better in rz
- **Same** track finding **efficiency** (94.7% vs. 94.6%)
- **Smaller fake rate** in SF+LR (12% vs. 18%)

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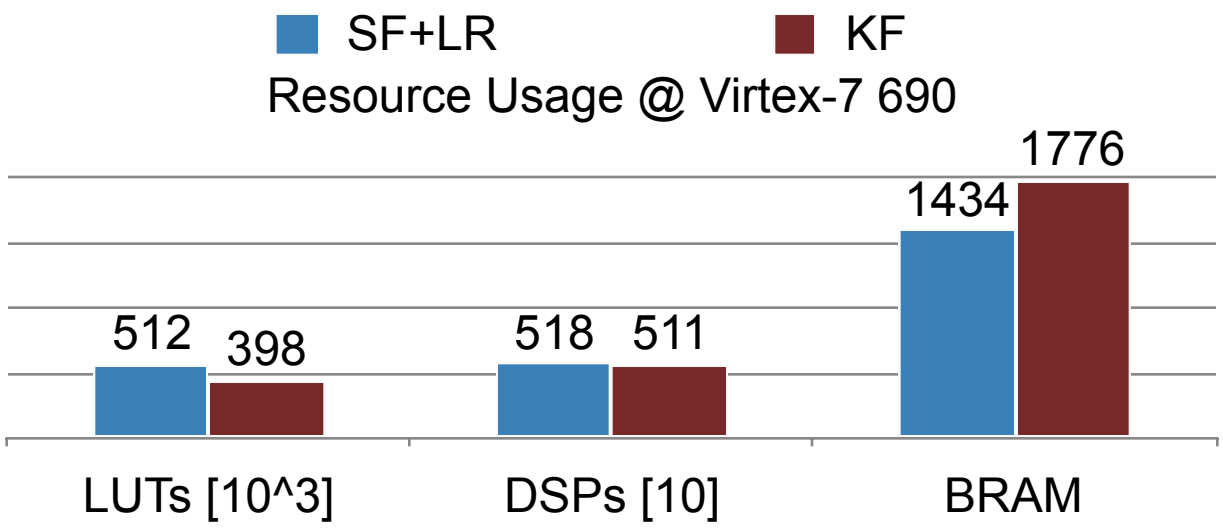
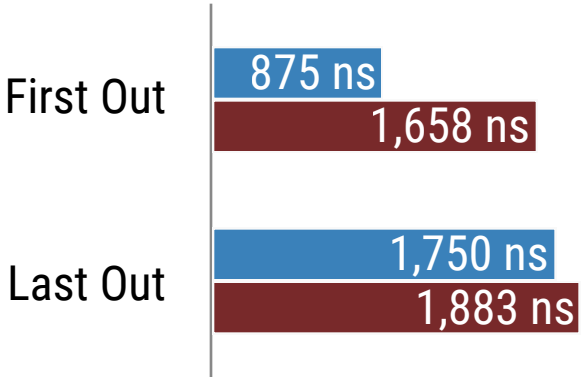
FITTERS COMPARISON





- **Similar** FPGA **utilisation**
  - SF+LR more LUTs, KF more RAMs
- **SF+LR** slightly **faster** (about 130 ns)
- Both designs implement the **same DR** modules

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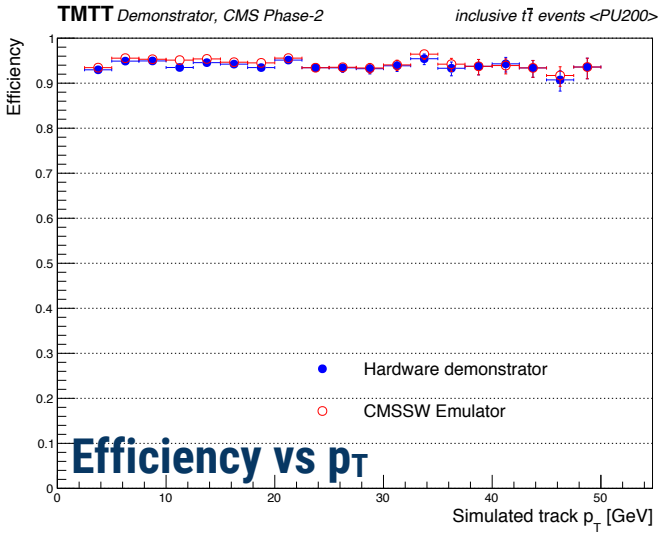
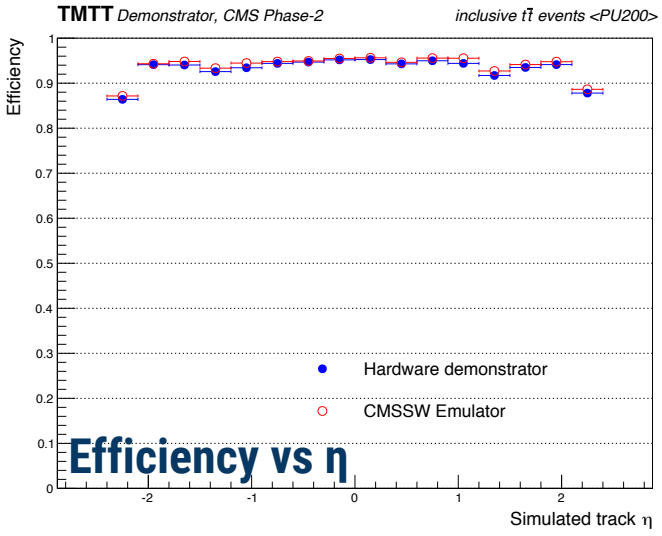
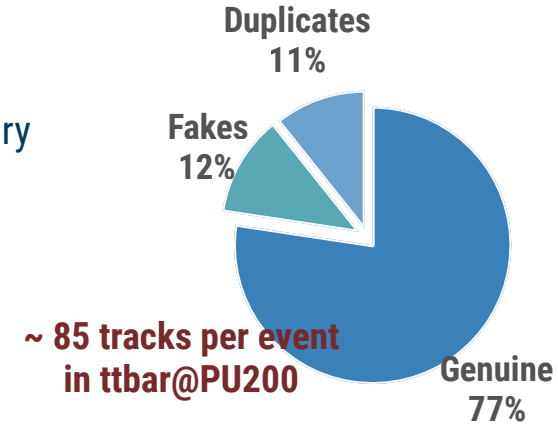
DEMONSTRATOR RESULTS: TRACK FINDING PERFORMANCE





- **Track Finding Efficiency**: no. reconstructed tracks/no. generated tracks
  - considering only generated tracks from primary interaction with **pT > 3 GeV and hits in 4+ tracking stations**
- ~95% average track finding efficiency of inclusive ttbar@PU200
  - ~97% for muons



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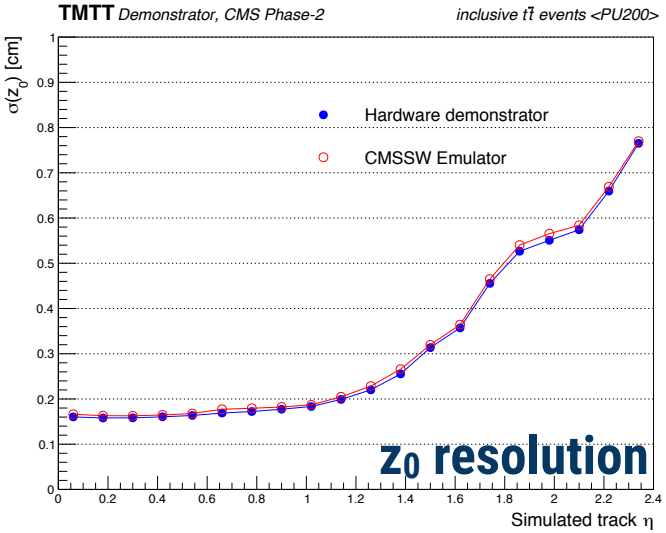
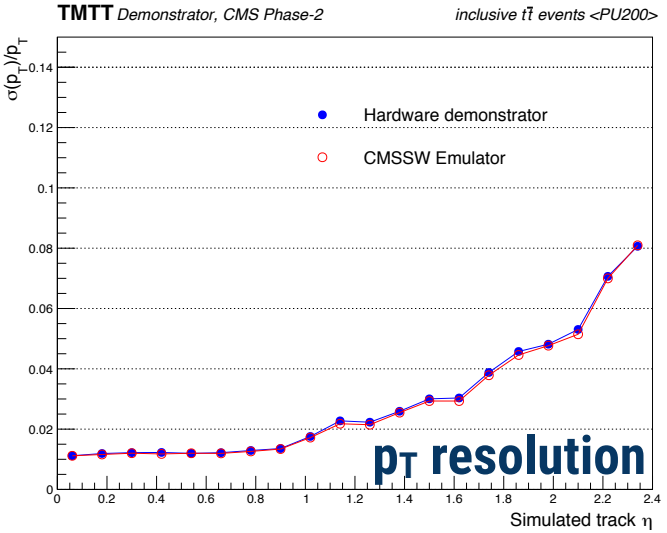
DEMONSTRATOR RESULTS: TRACK FINDING PERFORMANCE





- About 1% p_T resolution and ~2mm z_0 resolution in the barrel
  - better resolution can be achieved increasing the number of bits to encode the *r* and *z* stub coordinates (1mm resolution achievable)

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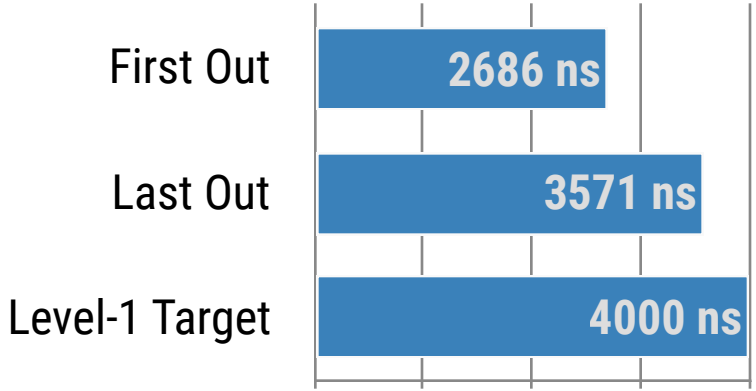
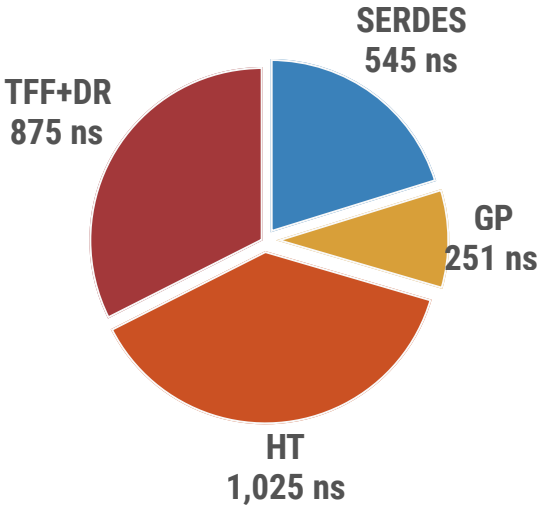
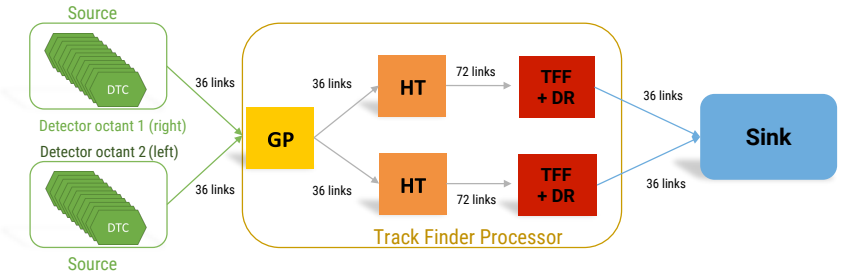
DEMONSTRATOR RESULTS: LATENCY



- **Fixed latency** - event independent
- Well below 4μs budget
- Lower latency achievable by increasing clock frequency, link speed and improving utilisation





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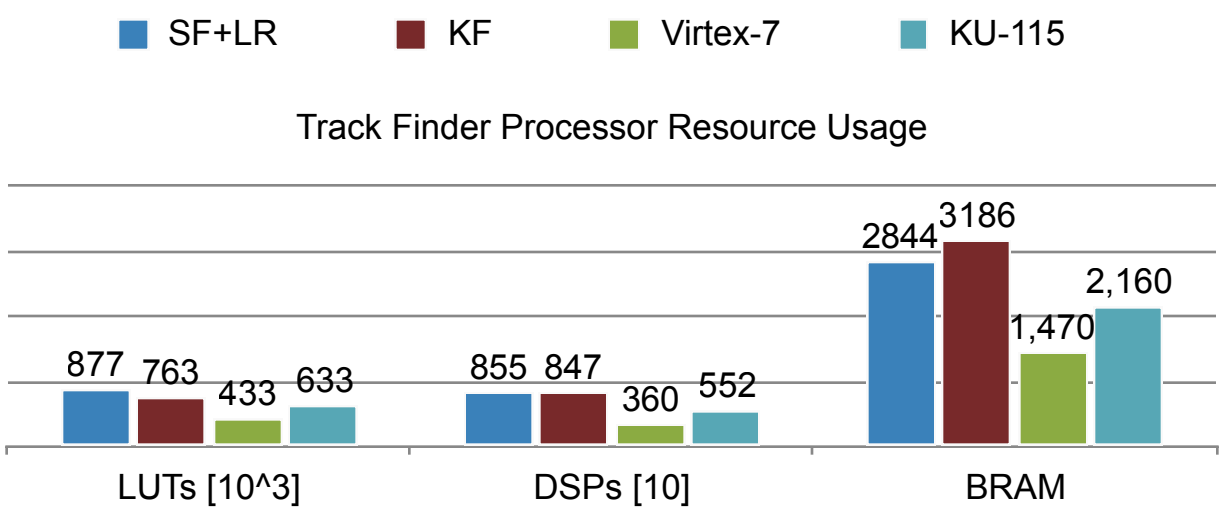
TFP RESOURCE USAGE



- Entire algorithm could potentially fit in just 3 Virtex-7 690
  - limited I/O bandwitdh
- Final system expected to be constructed with two Kintex Ultrascale-115 FPGAs
  - resource usage can be improved targeting higher clock frequency
  - optimisation of tracker geometry design (tilted barrel) will reduce input data rate

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SUMMARY

- Demonstrated in hw the concept of a **full track-finding system** at HL-LHC with **FPGA** based processing boards
  - Demonstrator reconstructs tracks with **~95% efficiency in less than 4μs**
- **Highly configurable**
  - Two independent fitters developed (similar performance)
  - Algorithm updates can be deployed in few seconds
  - Extra nodes allows testing of new fw during data taking
- **Highly scalable**
  - Adaptable segmentation to take care of larger/smaller data rates
- Plans to build another demonstrator system with **newer FPGAs and 16.3 Gbps optical links**
  - Target smaller latency O(2μs)
- Our design has been recognised as the **most promising option** (TDR) for the future CMS phase II Track Trigger system
  - System could be built even today if required ($$$)
  - Expect to be installed for CMS Phase II

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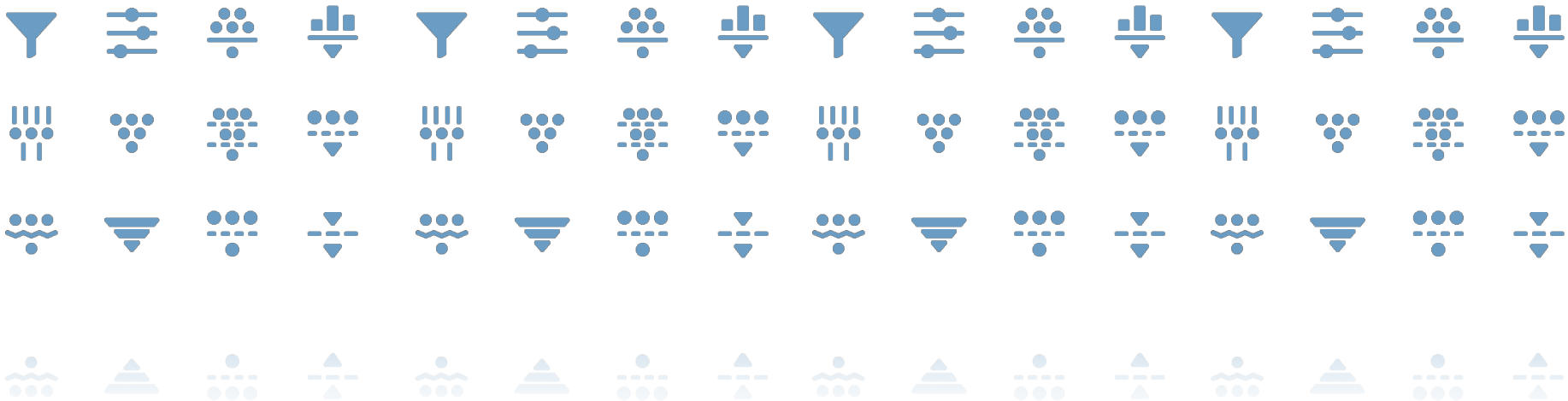


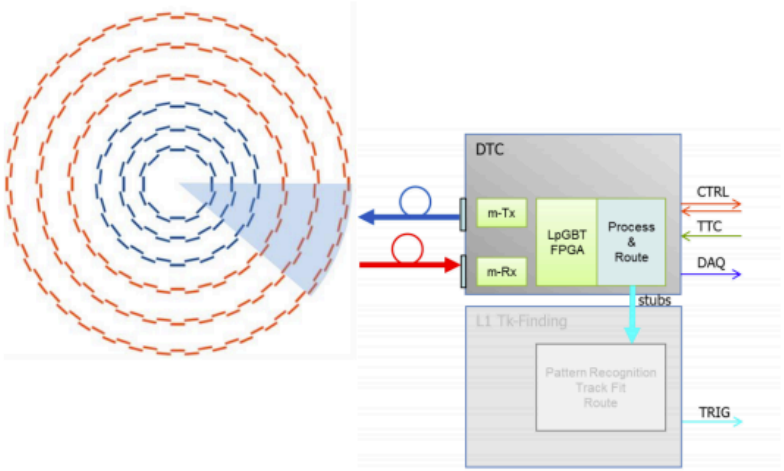
BACKUP

DATA ORGANISATION

detector to be interfaced to a first layer of off-detector hardware known as the **Data, Trigger and Control (DTC) system**

DTC to configure and read out tracker modules – including trigger data at 40MHz

total system to comprise **256 boards**



32 DTCs control ~1900 modules (in 1/8 of tracker in ϕ, or 'octants')

DTC to also implement low level stub manipulation e.g. global coordinate conversion, duplication, routing to next layer (L1 Track Finder)

FE -> DTC output latency ~1μs

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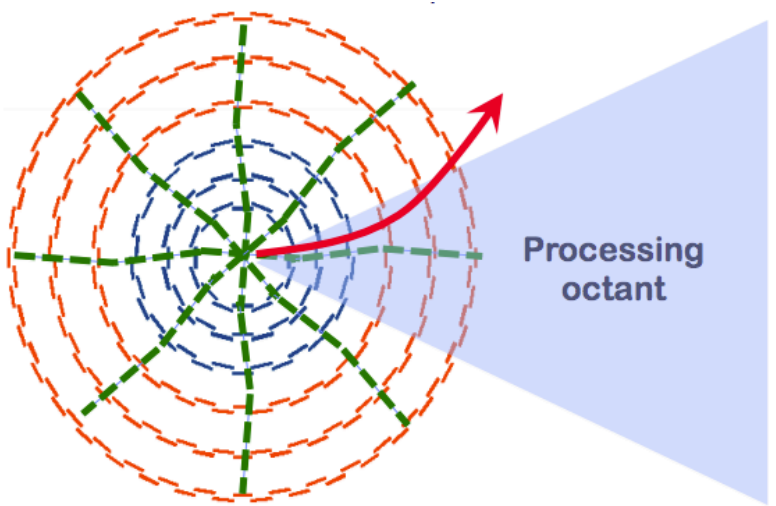
DATA ORGANISATION

- Each ”Track-Finding Processor” (TFP) is responsible for reconstructing all the tracks in one ϕ octant, known as a “processing octant”
- We rotate the “processing octant” by 1/2 octant w.r.t the “detector octant”.
  - To reconstruct particles within its processing octant, a TFP never needs stubs from > 2 detector octants, despite track curvature.



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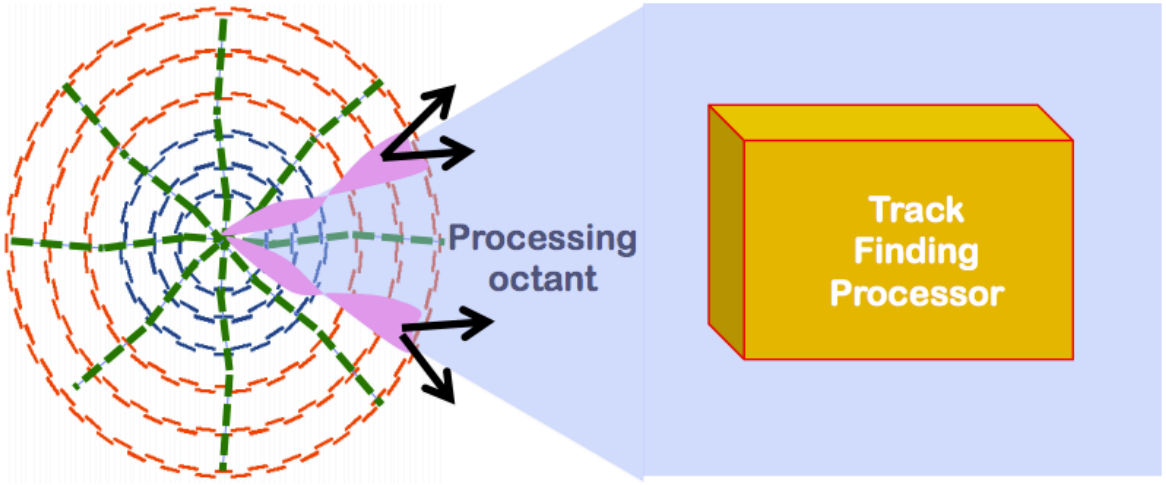
DATA ORGANISATION

- The DTC duplicates stubs in overlap region near processing octant boundaries (pink), & sends them to the two neighbouring processing octants.
  - No sideways communication is needed between Track Finding Processors from neighbouring processing octants.
  - Makes it natural to demonstrate system by building a TFP.



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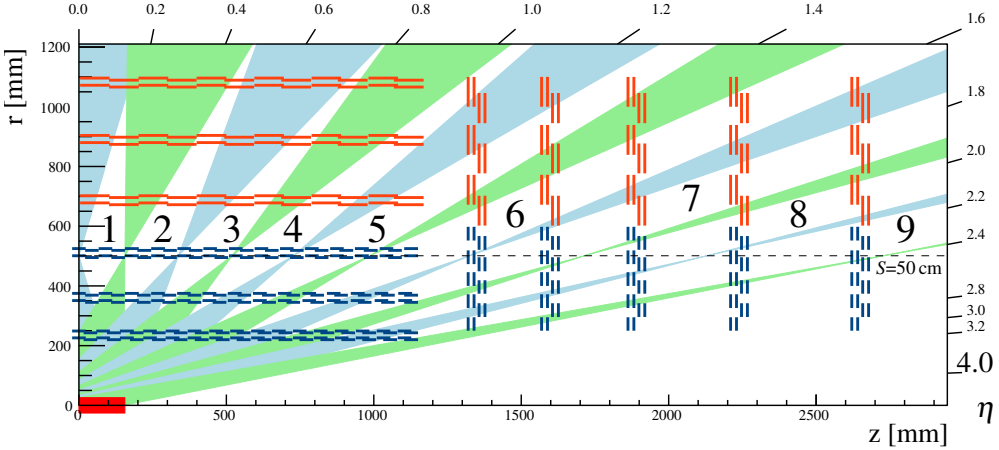
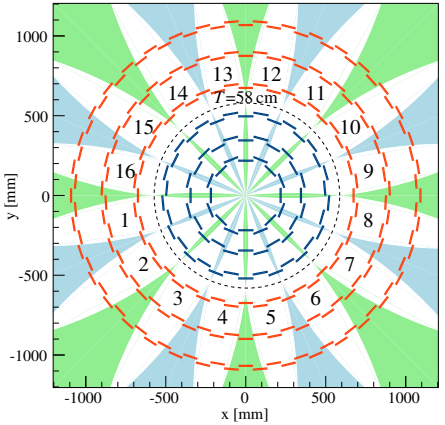
GEOMETRIC PROCESSOR





- **Converts** stub data into a more useful data format
  - **Reduced processing load** downstream
- Divide each octant into **2Φx18η sub-sectors**
  - Sector defined to reduce duplications
  - **Tracks** are found **independently** in each **sub-sector**
- **Assigns** each **stub** to the correspondent sub-sector(s)
- Average number of stubs per sector = 90

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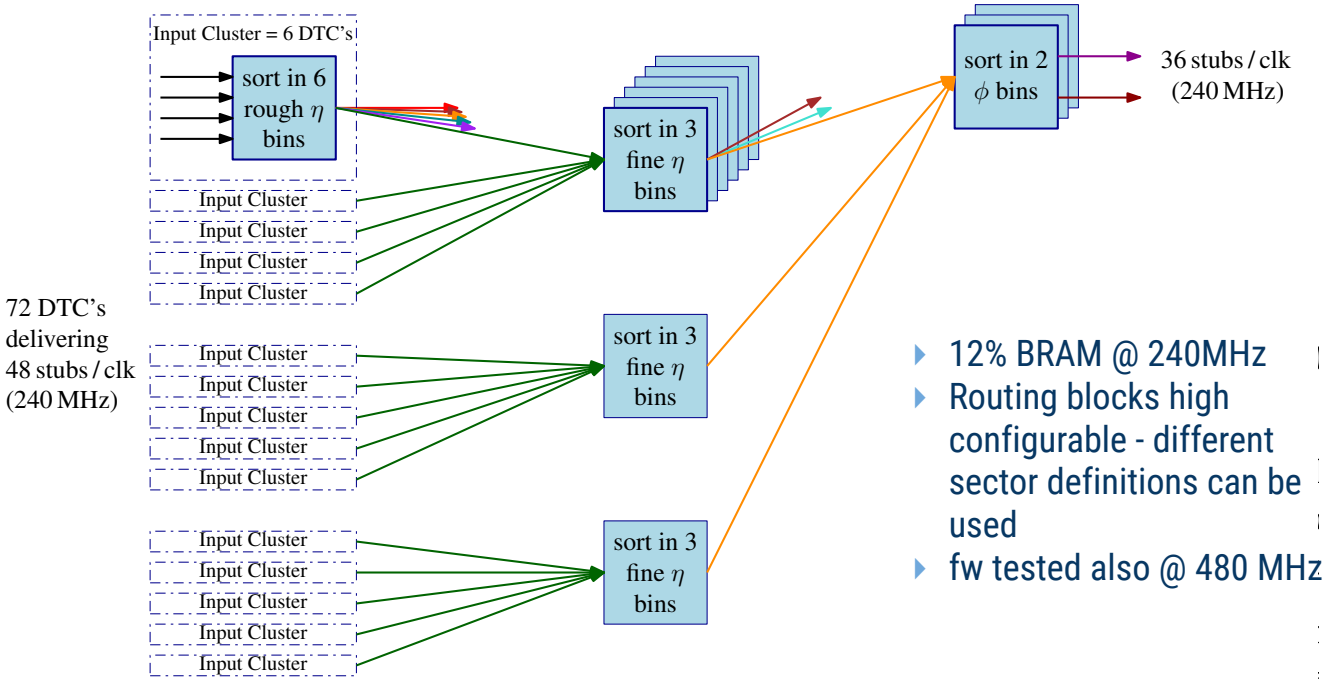
GEOMETRIC PROCESSOR FIRMWARE



- 12% BRAM @ 240MHz
- Routing blocks high configurable - different sector definitions can be used
- fw tested also @ 480 MHz

- **GP firmware** implemented on a **single** Virtex-7 FPGA
- Routes stubs from **72 input** (DTC) **to 36 output**
  - maximum number of output stubs per channel = 175
- Stubs are first formatted and then routed through a **three stage mash**

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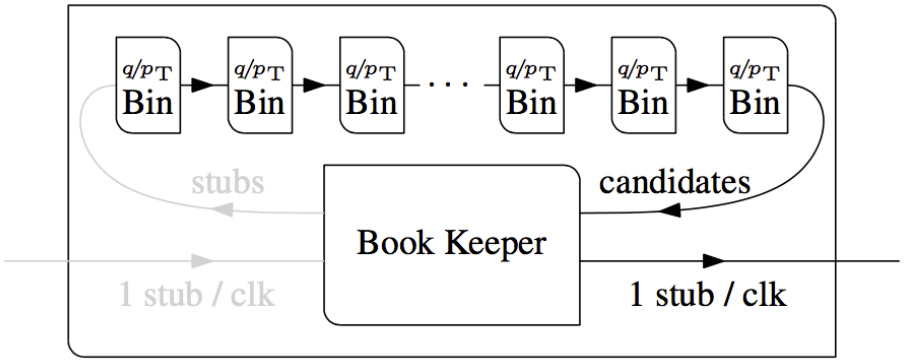
HOUGH TRANSFORM FIRMWARE

- **One HT array** per GP output **channel**
  - 18 arrays per MP7 - **two boards** needed
- **Fully pipelined design** @240 MHz, processing one stub per clock



- **Book Keeper unpacks** stub data from input link, then **propagate** them to first **bin**
  - Stubs then are transmitted **from bin to bin**, connected in daisy-chained fashion
  - **Track candidates** found by each bin are also **propagated** in the chain
- Book Keeper **transmits out stubs from track candidates** over output links

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SIMPLE LINEAR REGRESSION FITTER

- Tracks with sufficient p_T should draw a **straight line** on both **RΦ** and **RZ** planes
- The Simple Linear Regression algorithm performs **two independent fits** in the two planes

$$q/p_T = \frac{n\overline{r\phi} - \overline{r}\,\overline{\phi}}{n\overline{r^2} - \overline{r}^{-2}} \qquad \tan\lambda = \frac{n\overline{rz} - \overline{r}\,\overline{z}}{n\overline{r^2} - \overline{r}^{-2}}$$

$$\phi_T = \frac{\overline{r^2}\,\overline{\phi} - \overline{r}\,\overline{r\phi}}{n\overline{r^2} - \overline{r}^{-2}} \qquad z_T = \frac{\overline{r^2}\,\overline{z} - \overline{r}\,\overline{rz}}{n\overline{r^2} - \overline{r}^{-2}}$$

1. Compute the **helix parameters** on the **RΦ** plane
2. Calculate the **RΦ residuals** and keeps only stubs within 5σ from fit line
3. Calculate again the **helix parameter** in **RΦ** and in **RZ** (use only PS)
4. **X^2 calculation** and rejection of bad tracks

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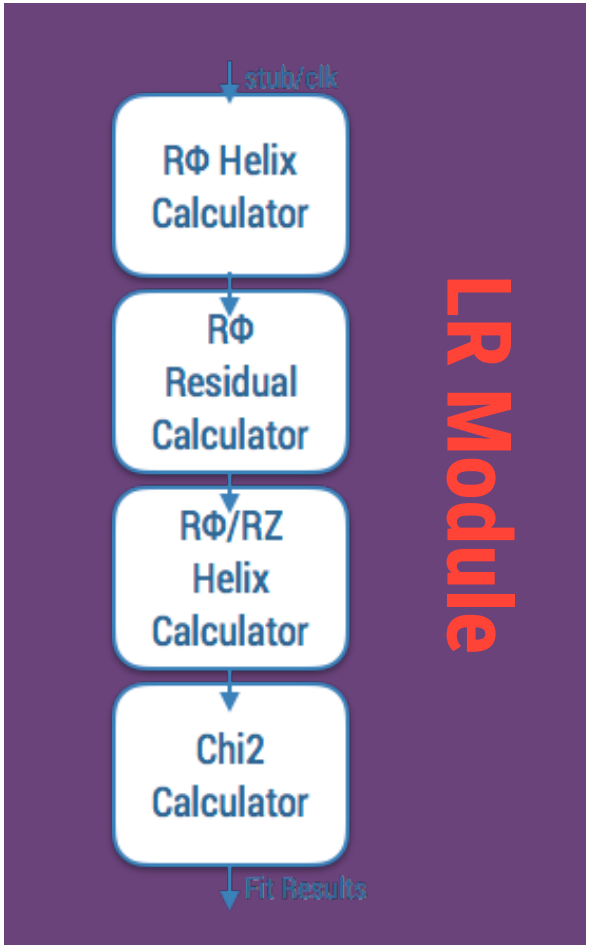
LR MODULE

- **Pipelined design** with fixed latency (~190 ns)
- Fitting steps integrated into four submodules
- Uses mainly DSPs and a LUT to implement divisions



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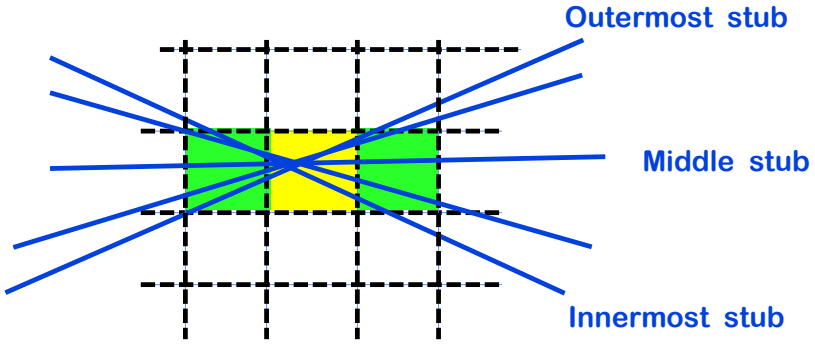
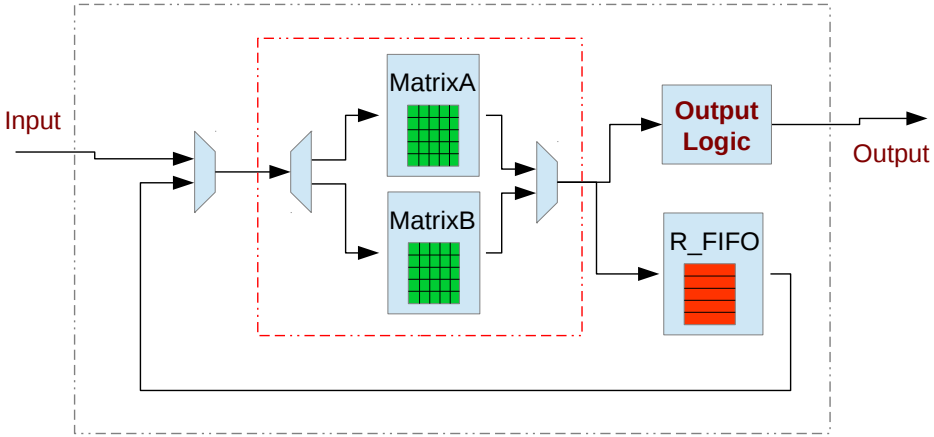
DUPLICATE REMOVAL



- Simple duplicate removal algorithm
- Keep tracks, whose **fit parameters** are **compatible** with **HT** coordinates
- **Second pass** over rejected tracks to avoid loss in efficiency

- Duplicate Removal implemented in **same chip as Track Filter** and Fitter
  - Same implementation for both KF and SF+LR
- Fast pipeline design (38ns)



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DEMONSTRATOR RESULTS: RESOURCE USAGE

	LUTs [10^3]	DSPs	FFs [10^3]	BRAM (36Kb)
GP	121	1056	205	222
HT	244	2304	299	1188
TFF+DR	512	5184	526	1434
MP7 Infra	90	0	91	291
Tot.	**877**	**8554**	**1030**	**2844**
Virtex-7 690	433	3600	866	1470
Kintex Ultrascale 115	633	5520	1266	2160

- Final TFP board can be made of two or three Kintex Ultrascale 115 FPGAs

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