The ATLAS Fast Tracker System

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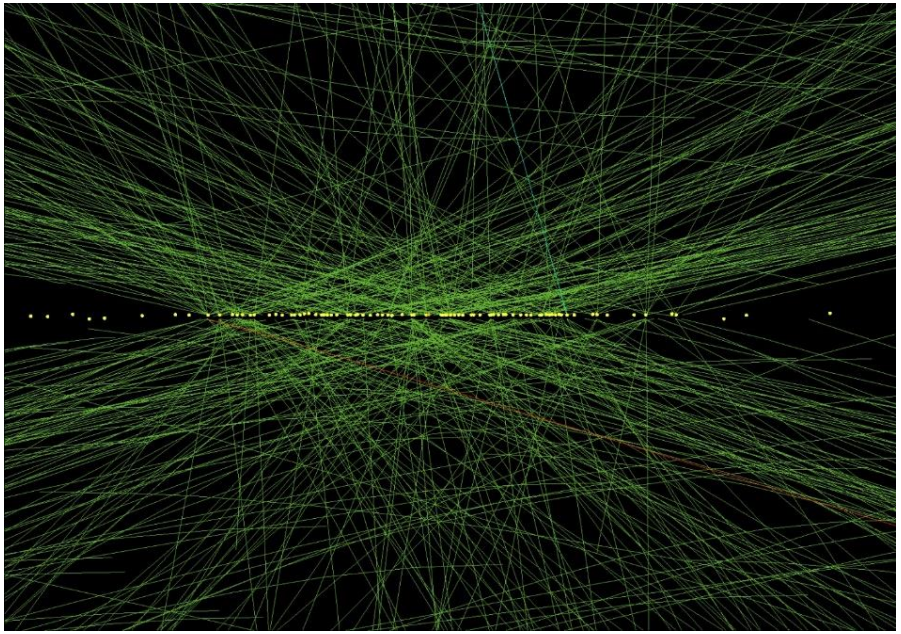
on behalf of ATLAS Collaboration
TWEPP2017 @ UC Santa Cruz

Challenge in high lumi. : Pile-up

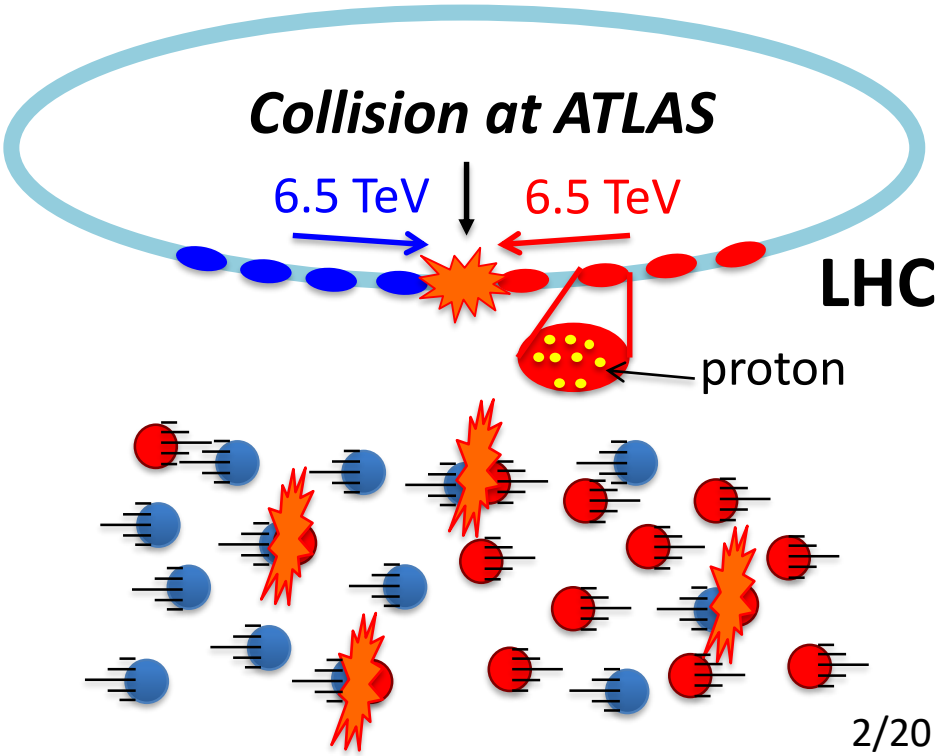
There are a large number of interactions per bunch crossing (pile-up).
→ Signal/background discrimination will become more difficult.

Track information is critical to distinguish primary vertices and pile-up.

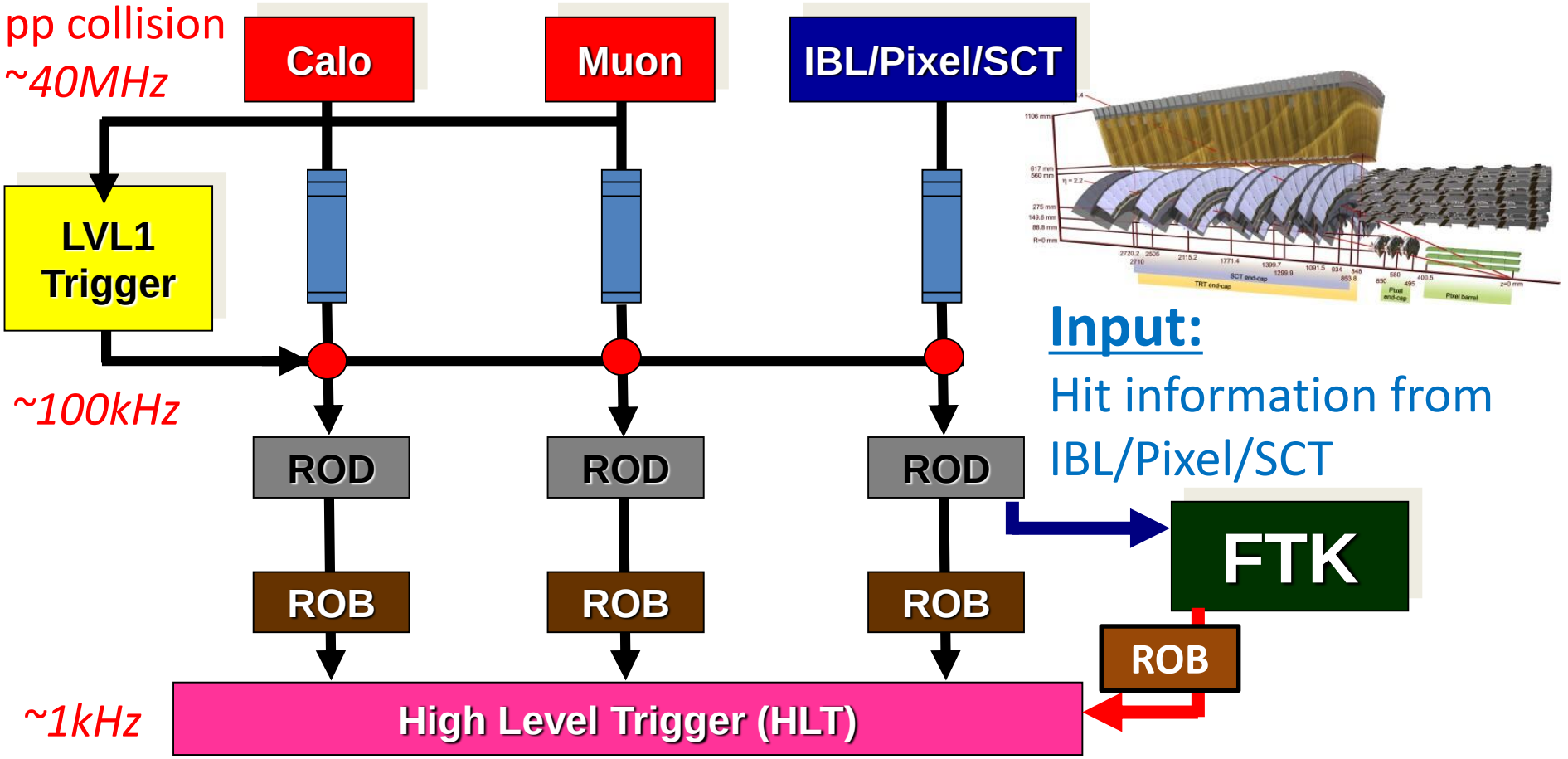
→ FTK is dedicated electronics system to reconstruct tracks, enabling a better trigger selection in high luminosity.



pile-up ~ 80 (expected in Run3)



ATLAS Trigger System with FTK

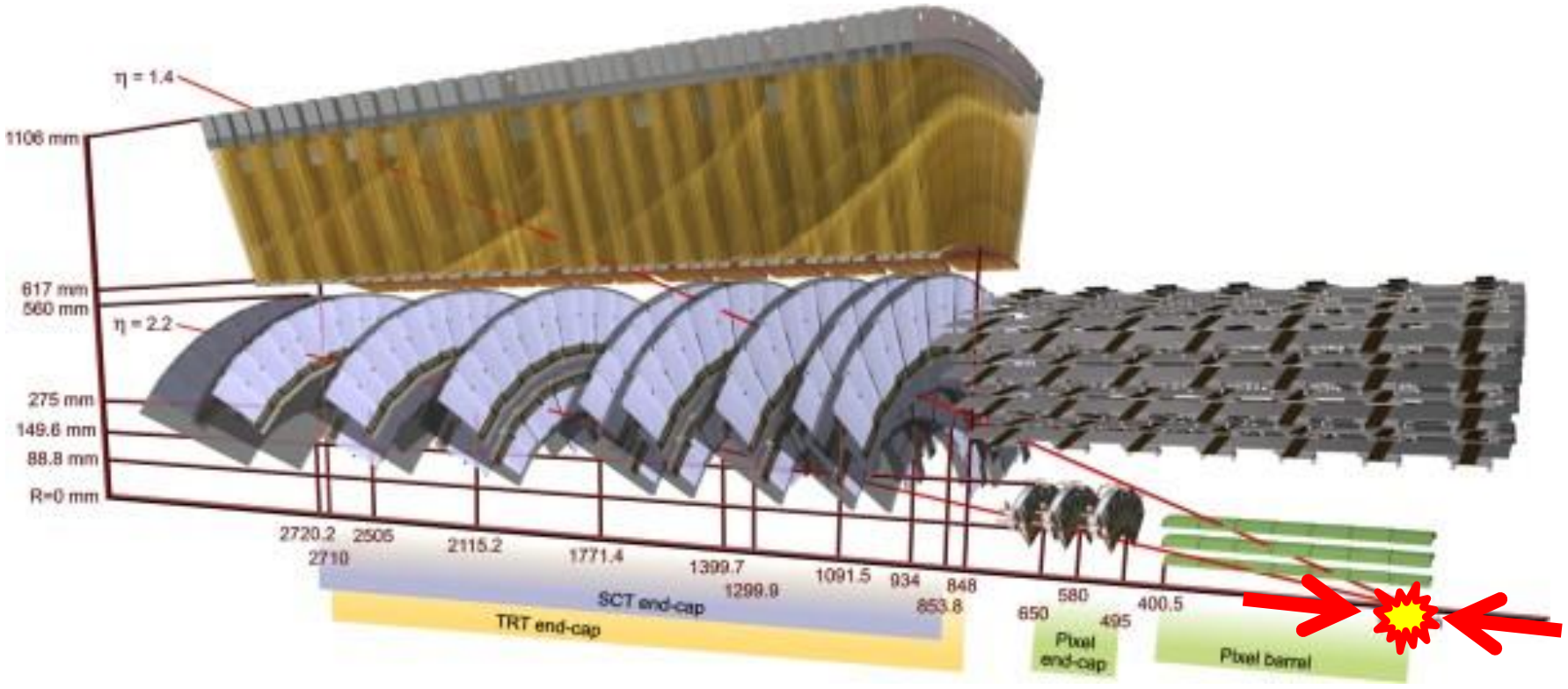


Input:
Hit information from IBL/Pixel/SCT

	w/o FTK	w/ FTK
Tracking coverage	RoI	**Full detector**
Available in	10ms/RoI	**100μs/all**

Output:
p_T, η, ϕ, d_0, z_0 for all tracks with $p_T > 1$GeV

FTK input: Inner Detector



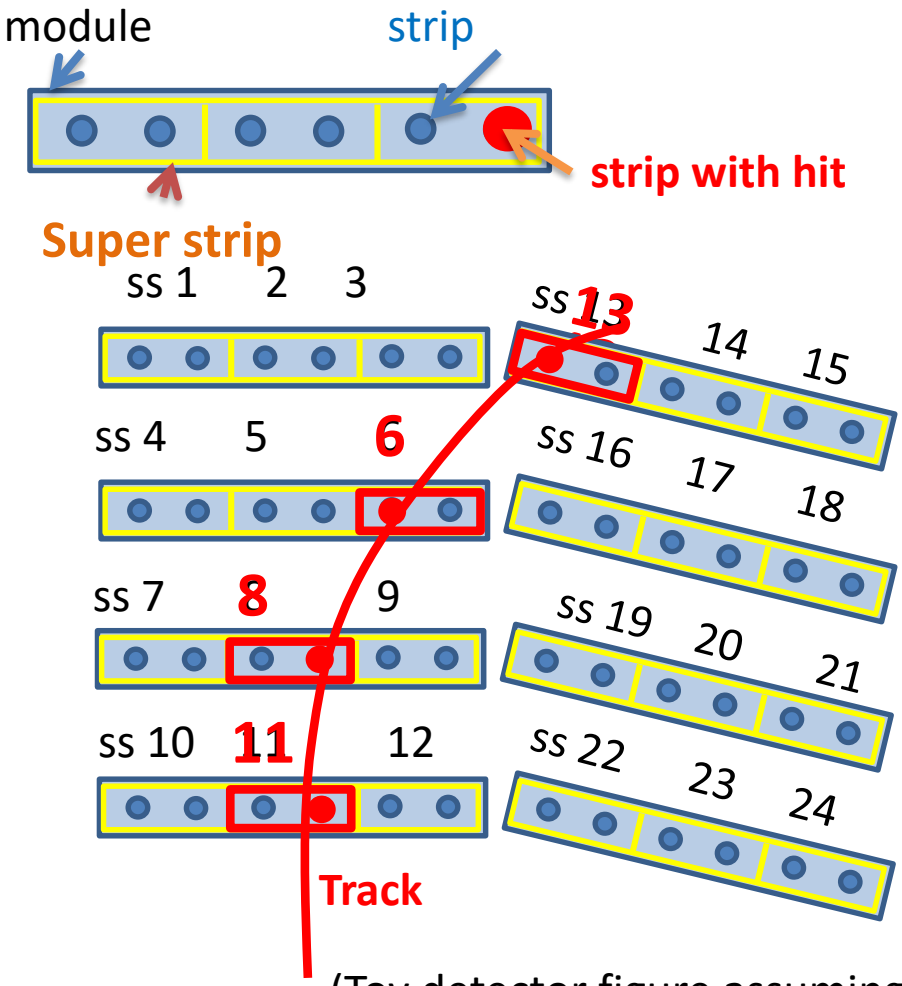
- ✓ Placed most inner part, measure position, momentum of charged particles.
- ✓ **The 12 layers of IBL/Pixel/SCT, in total ~100 million channels,** are the input of FTK.

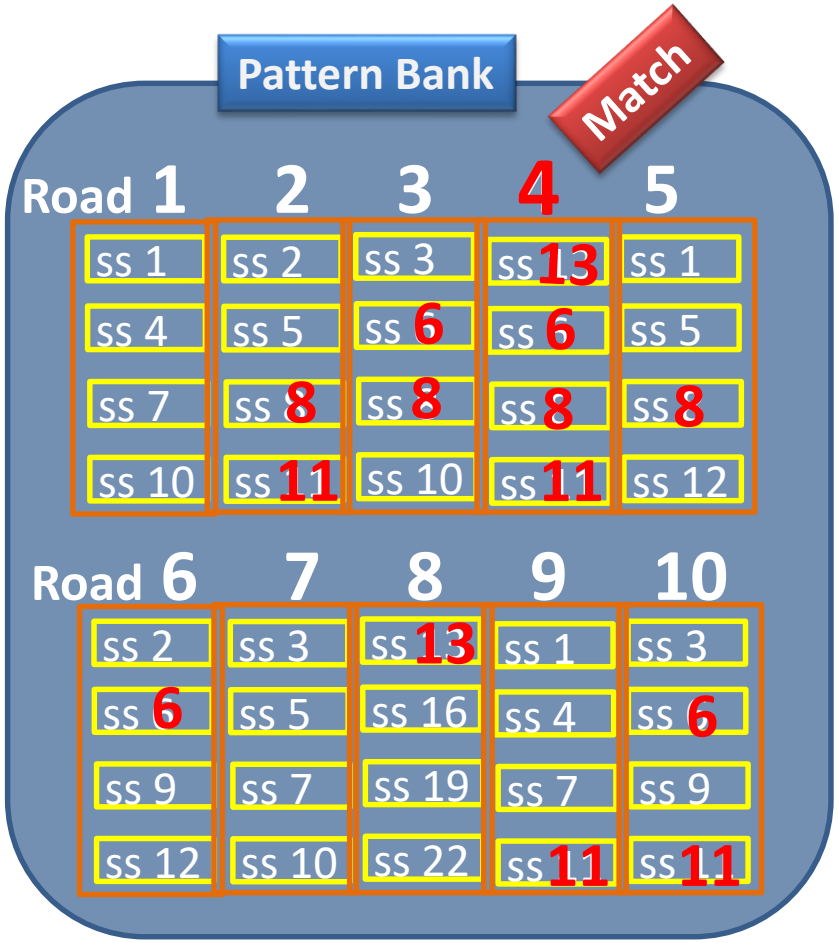
	#layers	Readout	size/unit	#channels
IBL	1	2-dim	50μm x 250μm	12M
Pixel	3	2-dim	50μm x 400μm	80.4M
SCT	8	1-dim	80μm	6.3M

Key Algorithm: Pattern Matching

To achieve fast tracking, pattern matching is performed. Hits are compared with pre-calculated patterns based on coarse resolution hits (**Super-Strip: SS**). The matched pattern is called a **Road**.

1 billion patterns are used





(Toy detector figure assuming 4 layers. In actually, 8 layers are used.)

Key Algorithm: Track Fitting

Linear approximation are performed to reconstruct track parameters with using pre-calculated constants. Here full resolution hits are used.

☐ Linear approximation

(Toy detector figure assuming 4 layers.
In actually, the output is calculated with 12 layers).

Track parameters are calculated immediately hits are coming.

Constants

Parameter

$$\tilde{p}_i = \sum_{l=1}^{N} C_{il} x_l + q_i$$

$\tilde{p}_i$: Observed Track Parameter (i=0~4)

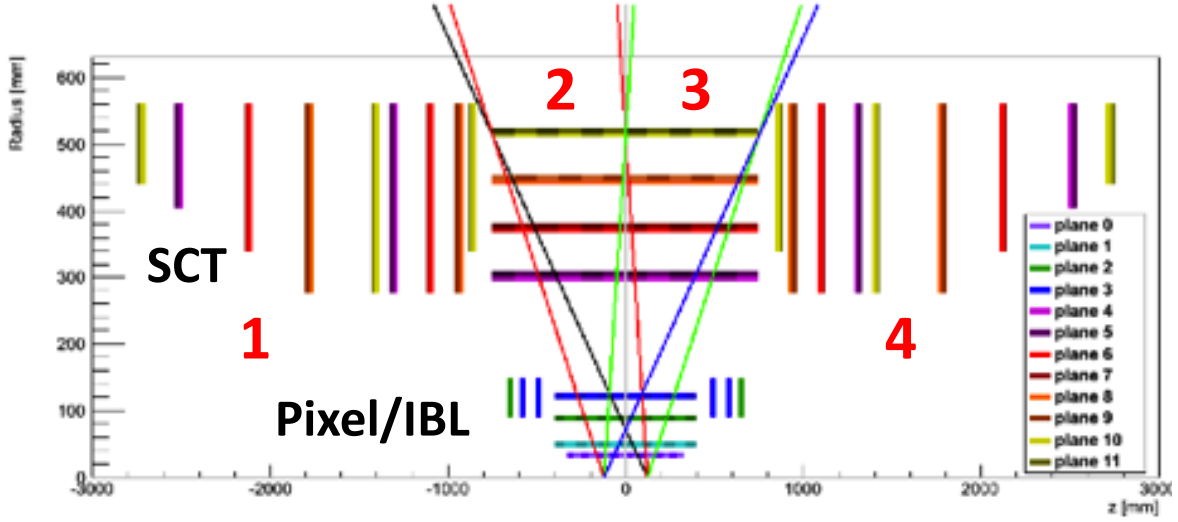
x_i : Hit Coordinate $\quad \vec{C}_i \; q_i$: Constants

5 helix parameters
d0, cotθ, ϕ, c, z0

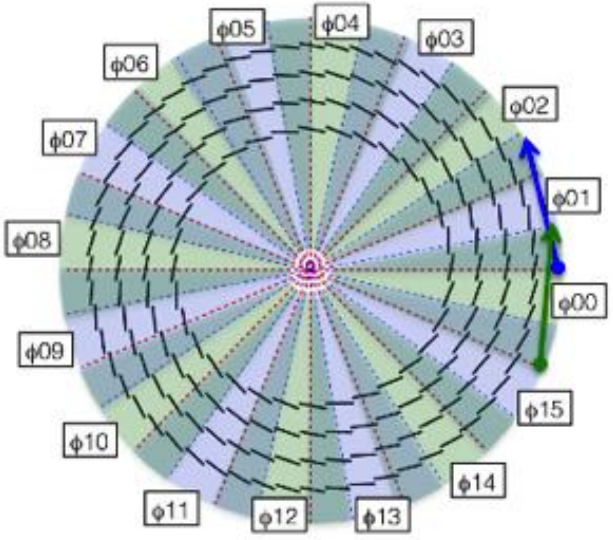
FTK patterns and constants are determined from simulation.

Parallel Processing

- ✓ Pattern matching and track fitting will run in parallel for further fast processing.
- ✓ Parallelization are performed based on detector region.
  → 4 x η, 16 x ϕ, in total 64 regions.



4 x η



16 x ϕ

Each region has overlap to avoid inefficiency at tower boundaries due to

- ✓ The finite size of the beam luminous region in the z coordinate.
- ✓ The finite curvature of charged particles in the magnetic field.

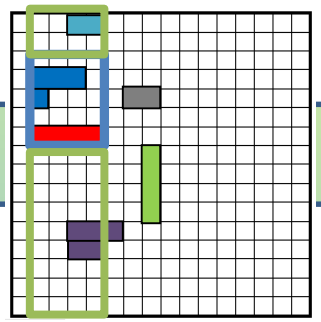
FTK Processing Schemes

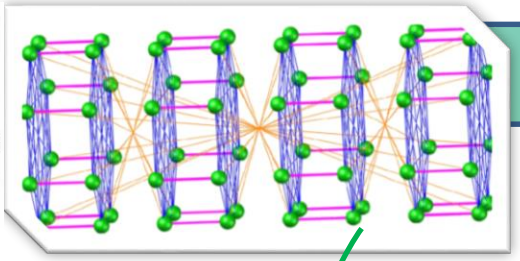
Massive parallel processing hardware

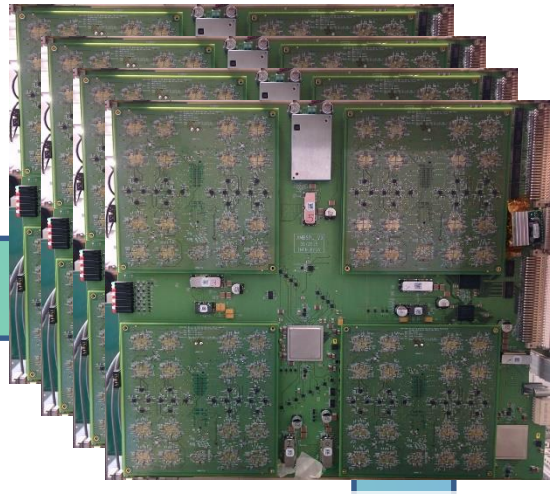
Clustering
Format data to be fit with FTK processing.

Data Switching
Distribute data to parallel processor based on the detector region.

IBL
PIX
SCT

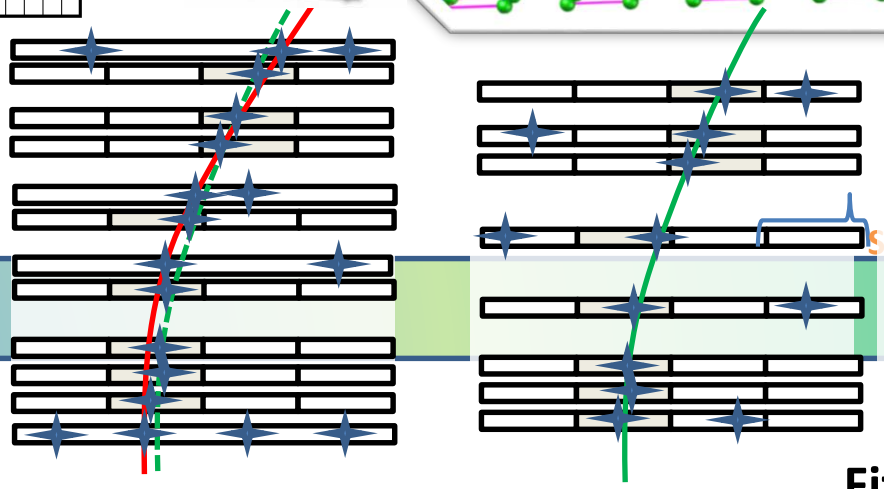






p_T, η, ϕ, d_0, z_0

HLT



Pattern Matching
8 layers: 3 pixels + 5 SCTs.
Hits are compared with pre-calculated patterns.
Track candidates are found.

Fit of 2nd stage
Tracks are refit with full 12-layer hit information.
→ Reduce fakes, improve resolution.

$$p_i = \sum_j C_{ij} \cdot x_j + q_i$$

Fit of 1st stage
Linear approximation are performed with 8-layers.
χ^2 component are calculated.

FTK System Overview

Data Formatter (DF)

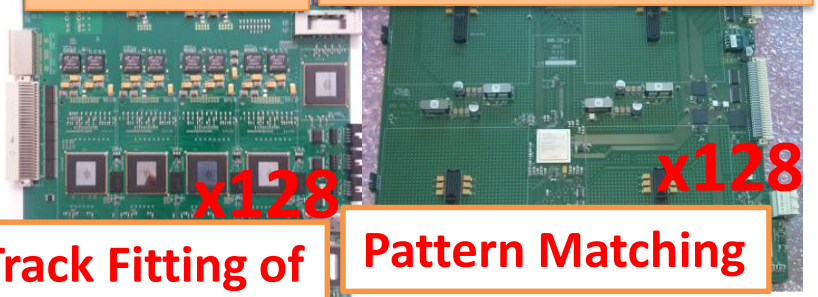
Clustering
Data sharing

Dual-output HOLA

Copy info. from ROD,
send it to FTK.

AUXiliary
Card (AUX)

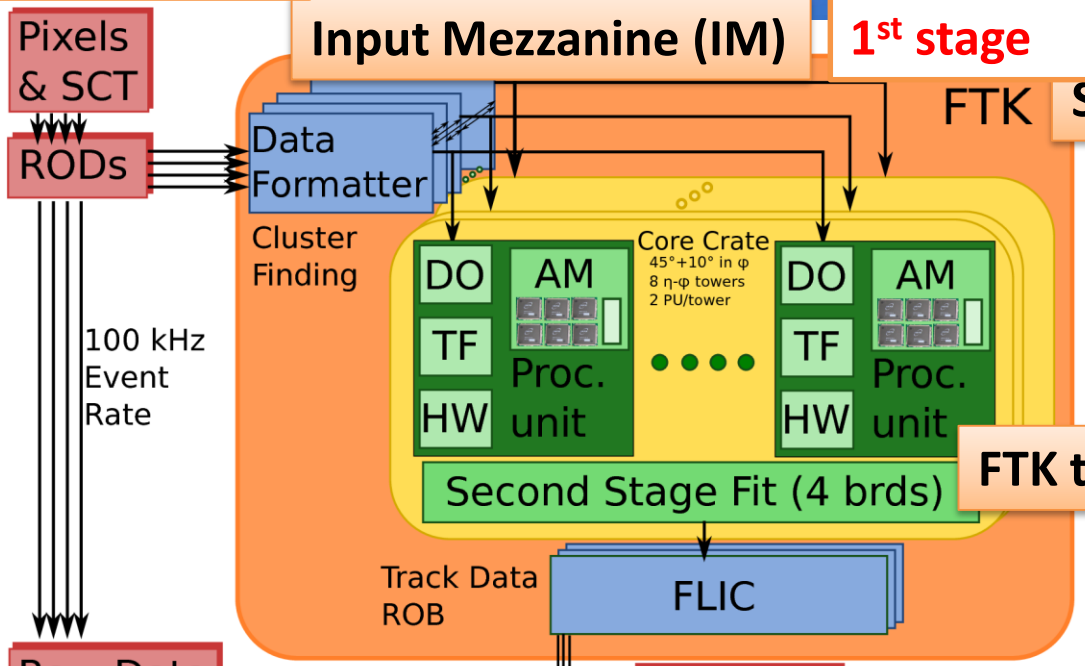
Associative Memory
(AM)



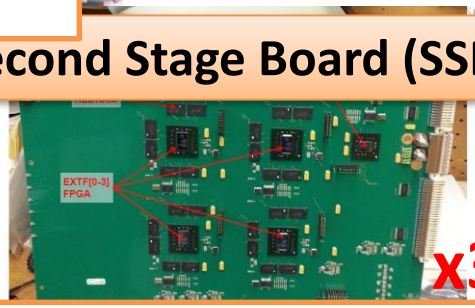
Track Fitting of
1st stage

Pattern Matching

Input Mezzanine (IM)



Second Stage Board (SSB)



Track Fitting of 2nd stage

FTK to L2 Interface Crate (FLIC)

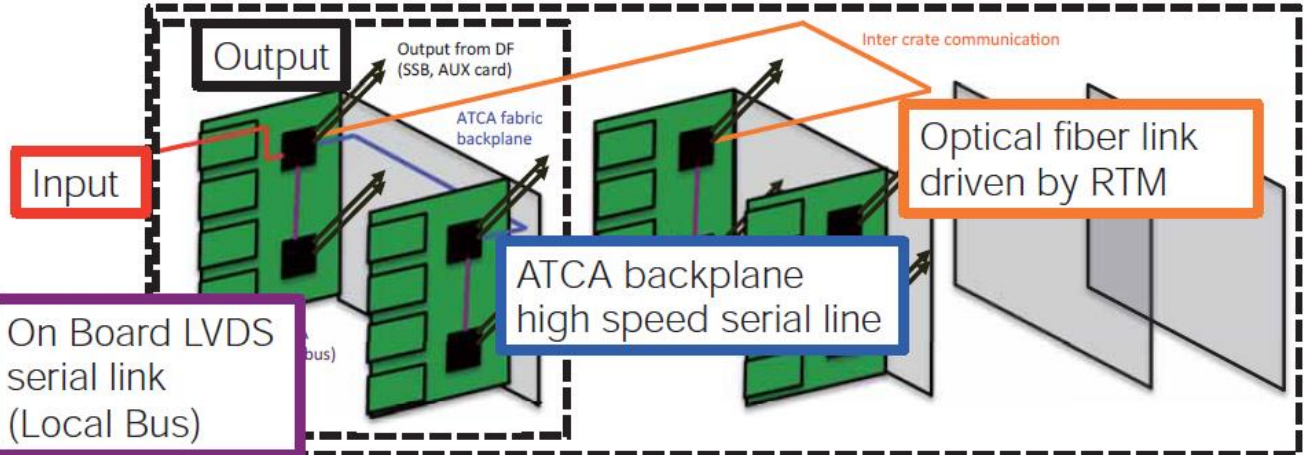
Send track info. to ROS

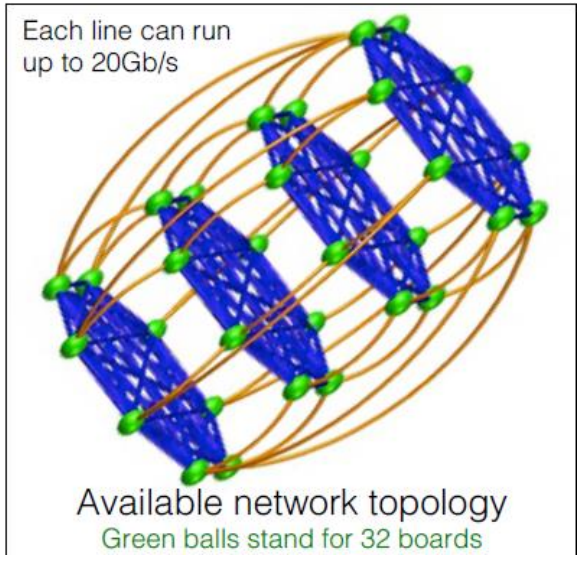
>8000 65nm ASIC chips, >2000 FPGAs

Data Sharing by ATCA

- ✓ Data Sharing for parallelization are done by Advanced Telecommunication Computing Architecture (ATCA) which can perform serial board communication on backplane.
- ✓ 1 crate holds 8 boards.
- ✓ 1 board process 2 regions.
  - → 32 boards, 4 crates are used to process 64 regions.
- ✓ Data sharing between crate is done by fibers.

AdvancedTCA®



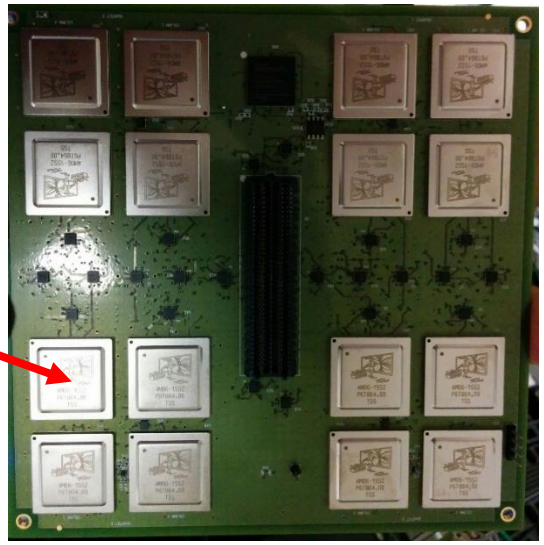


AM Chip Specification

	Technology	Area	Patterns	Pattern Density (/cm^2)	Detector Layers	Speed (MHz)	I/O	For
SVT AM			128		6 (12bits/layer)	30	parallel bus	CDS SVT (1992)
AMchip03	180nm	100mm^2	5k	5k	6 (15.5bits/layer)	40	parallel bus	CDF SVT (2005)
AMchip04	**65nm**	14mm^2	8k	57k	**8** (18bits/layer)	**100**	parallel bus	FTK R&D
AMchip06	**65nm**	**160mm^2**	**128k**	**80k**	**8** (18bits/layer)	**100**	**SERDES**	**FTK**

- ✓ Patterns are stored in special ASIC chips (AM chip).
- ✓ Great improvement for recent ten years.
  - ~16 times more pattern density than AMchip03,
    ~25 times more patterns can be stored.
  - Operating clock improves.
    - 40 MHz → 100 MHz.

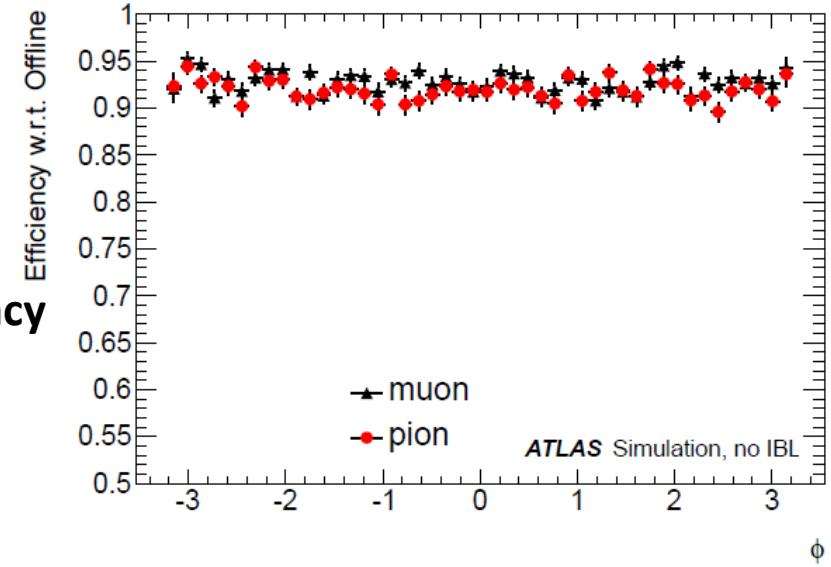
- ✓ FTK will use 8k chips.
  → 1 billion patterns can be stored.

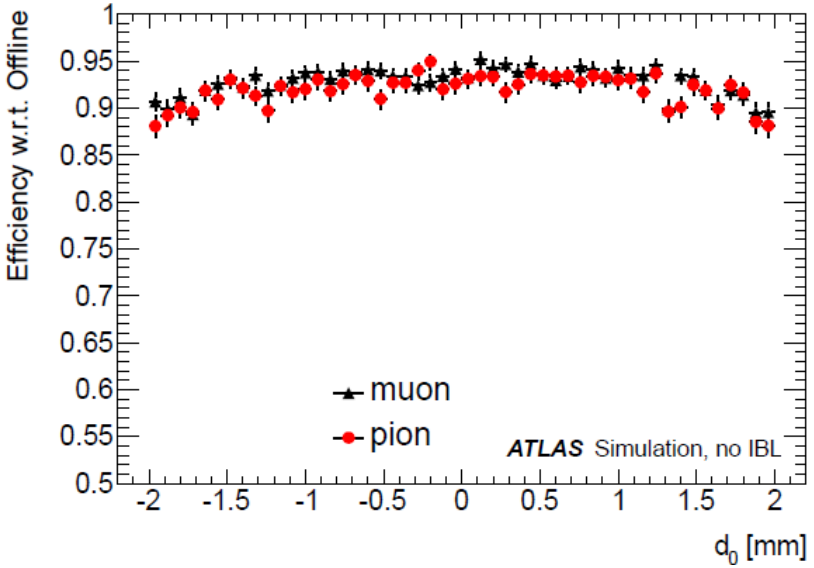


Tracking Performance

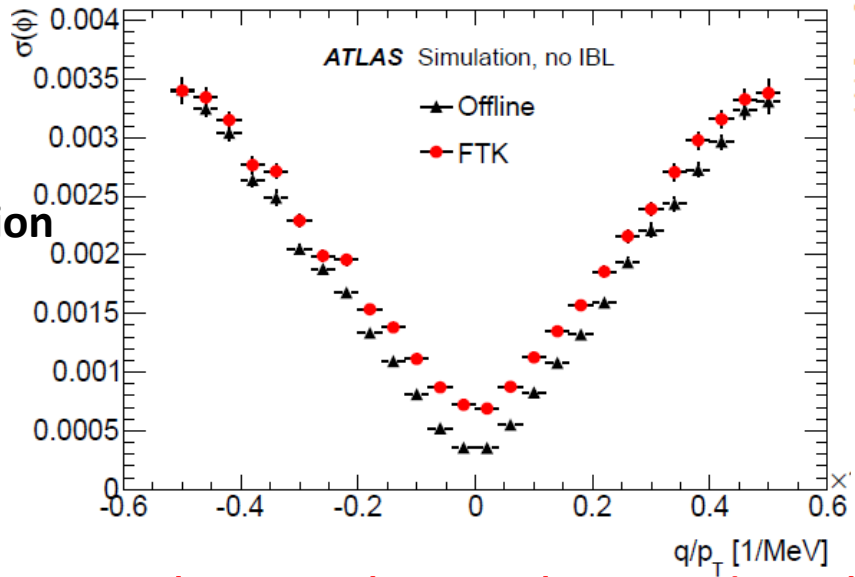
FTK TDR: http://cds.cern.ch/record/1552953/files/ATLAS-TDR-021.pdf (2013)

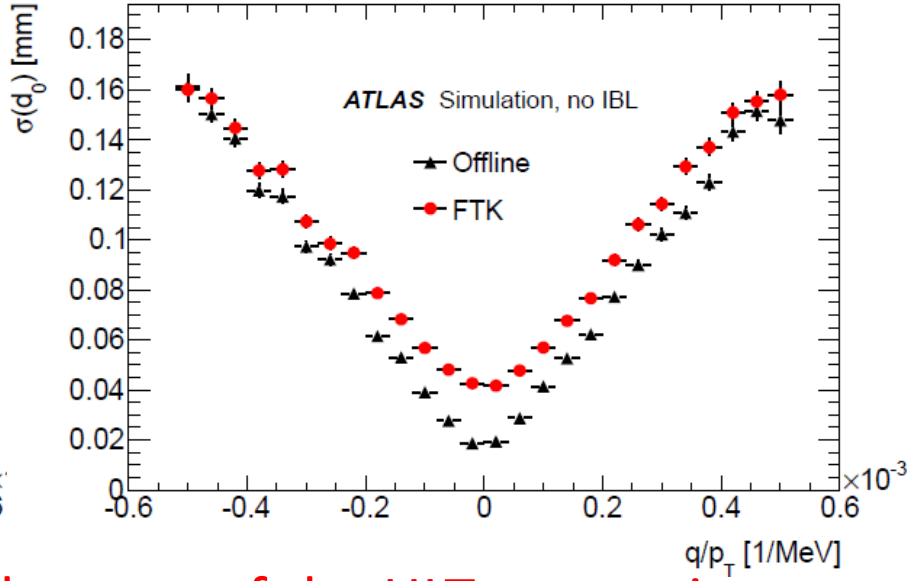
Efficiency





Resolution



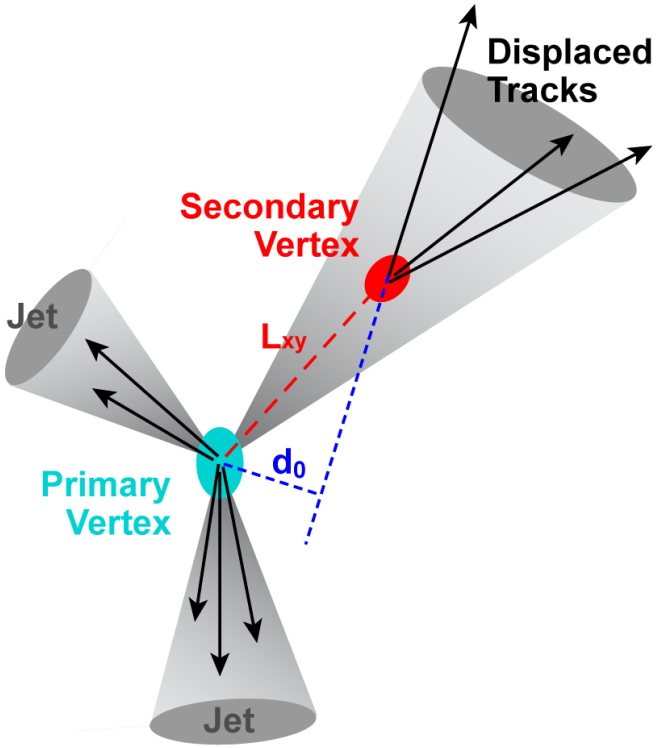


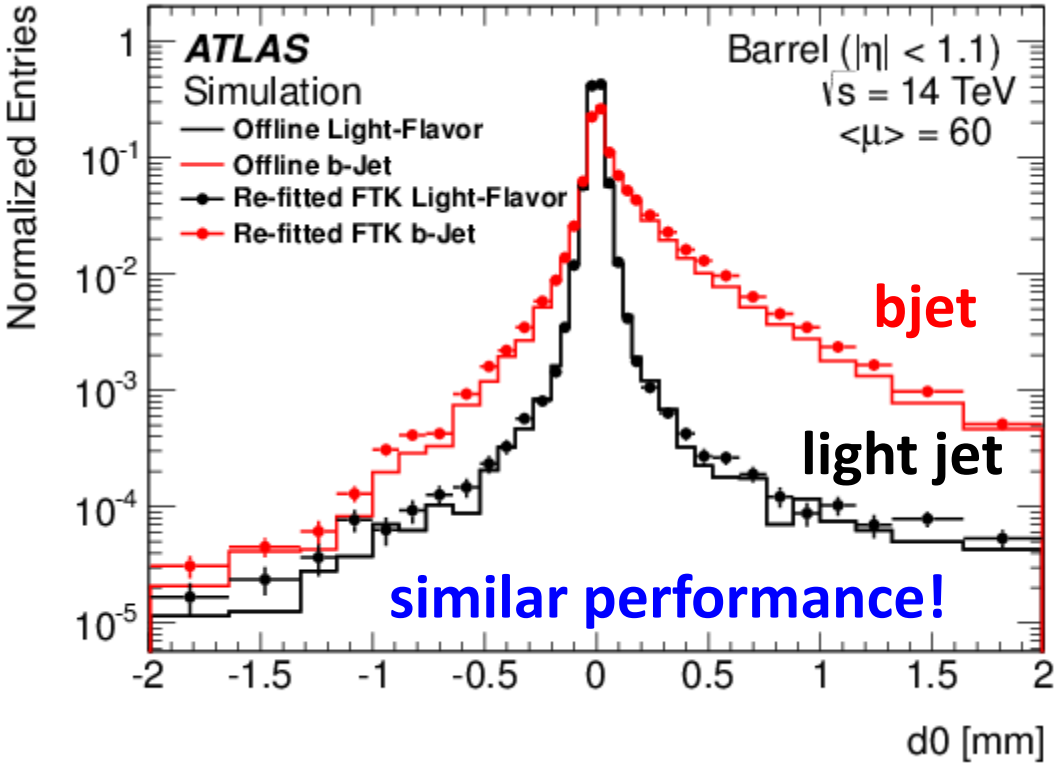
This quality tracks can be used at the start of the HLT processing.

Benefit of FTK

- ✓ HLT can use FTK tracks directly or quickly refit them.
- ✓ Better identification of the tracking objects such as b-jet, tau, track MET at the trigger level.
- ✓ It is also possible to reconstruct all the vertices in the event.

Ex.) transverse impact parameter for b-tagging



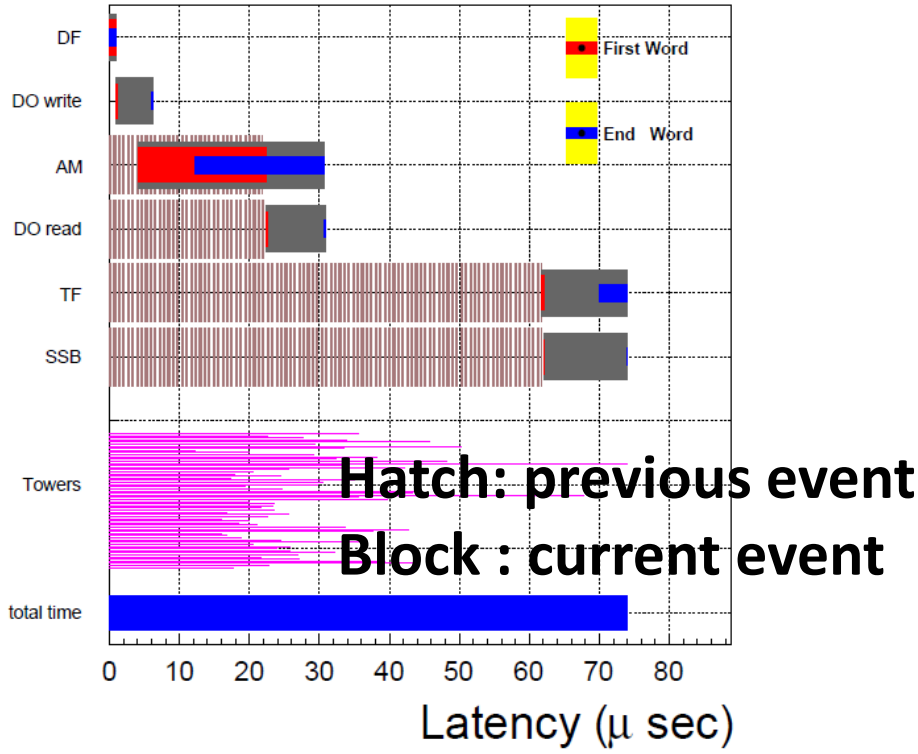


Simulation of Processing Time

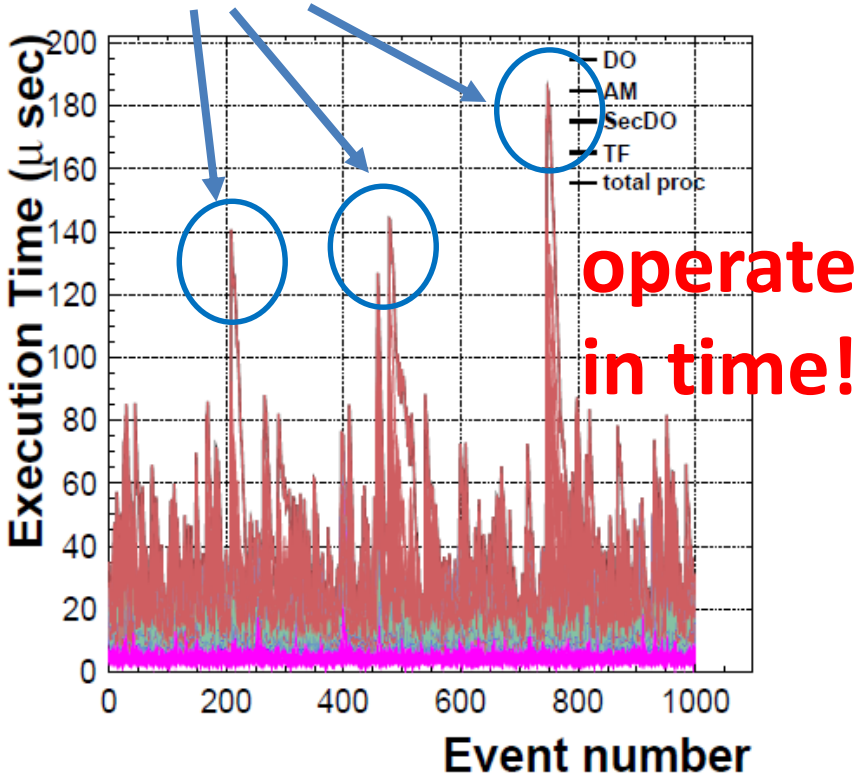
Since FTK runs in the trigger system, processing time is one of the important factors to be validated and optimized.

MC: Z → μμ, 69PU ($L = 3x10^{34}\ cm^{-2}s^{-1}$)
Input rate: 100 kHz

Some events takes much time, but it is soon recovered.



Processing time for 1 event



Processing times for 1000 events

Integration and Commissioning

Vertical Slice Test
Old prototype of IM & AM boards are tested with data from a part of SCT.

Start Global Integration
Test FTK system with production board. Build environment.

Install, Commissioning
Installation and testing with full FTK system at the real environment are ongoing.

Several series of tests were performed and FTK has been developed.

Challenges

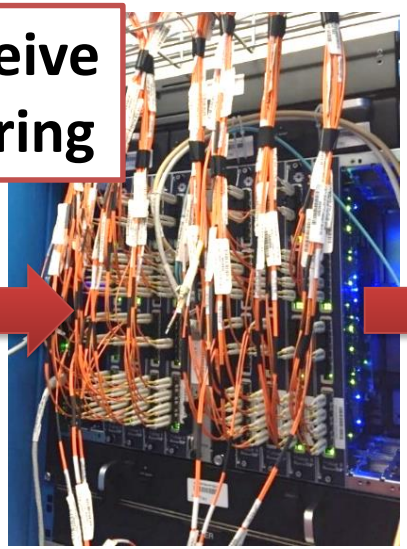
- ✓ Event synchronization at board boundary for global tracking.
- ✓ Many flow controls at board boundaries and even within an FPGA.
- ✓ Necessary to cope with various input data conditions.
- ✓ Develop complex processing performed by > 2000 FPGAs.

Accumulating many feedbacks and operating experience through these tests.

Hardware Installation Status

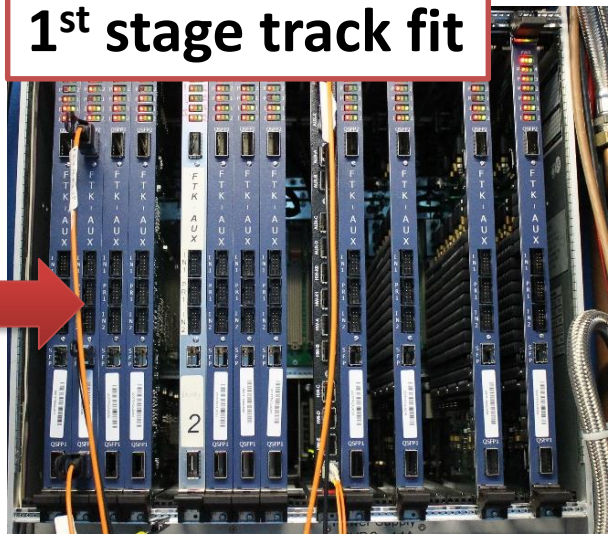
Data Receive
Data Sharing

ROD

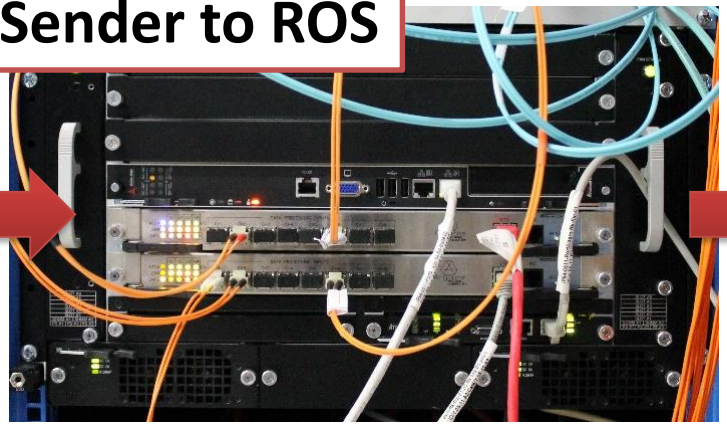


Pattern Matching
2nd stage track fit

1st stage track fit



Sender to ROS

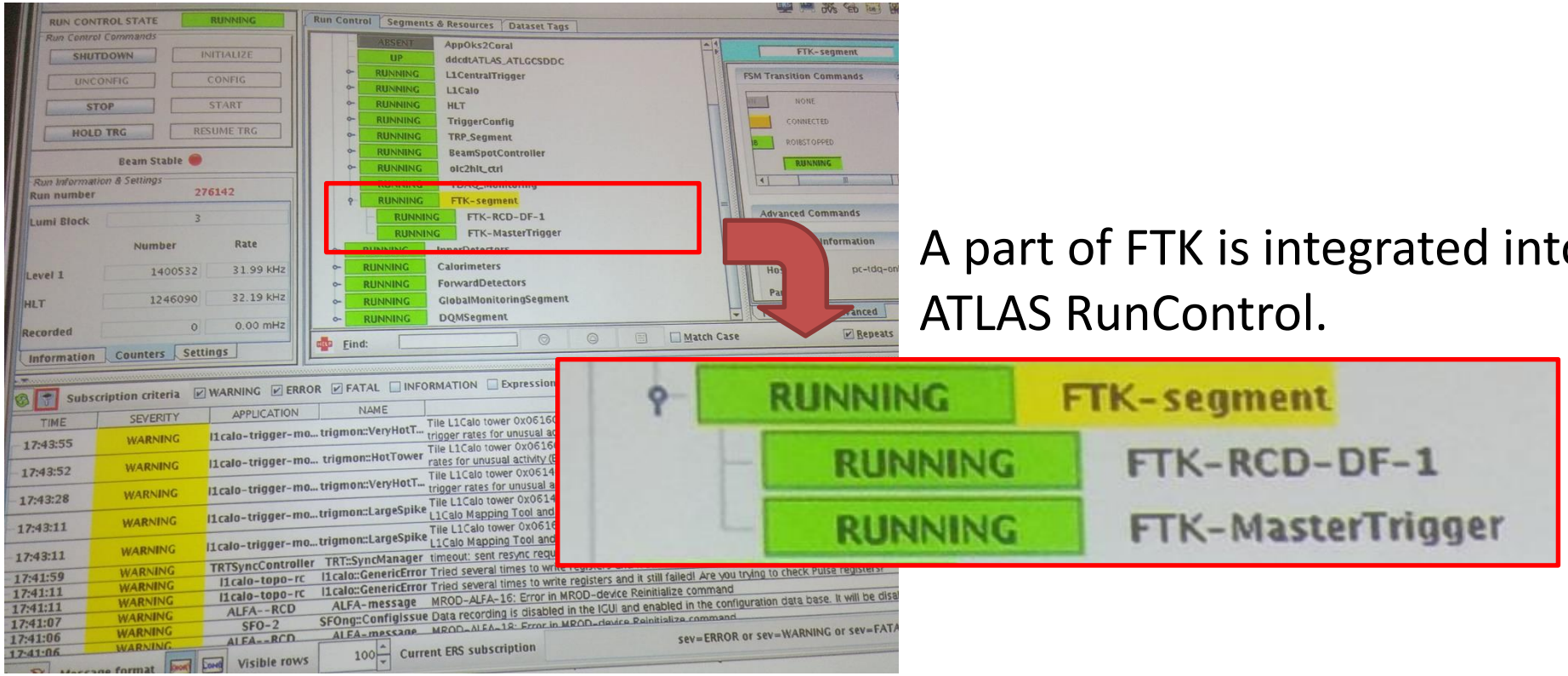


ROS

- ✓ Boards are installed when they are ready.
- ✓ Commissioning is ongoing with the installed boards.
- ✓ Development to operate under real environment ongoing.

Integration to ATLAS RunControl

RunControl to configure/monitor FTK being developed.
A part of it is integrated into ATLAS RunControl to control FTK with same way as other detectors.



A part of FTK is integrated into ATLAS RunControl.

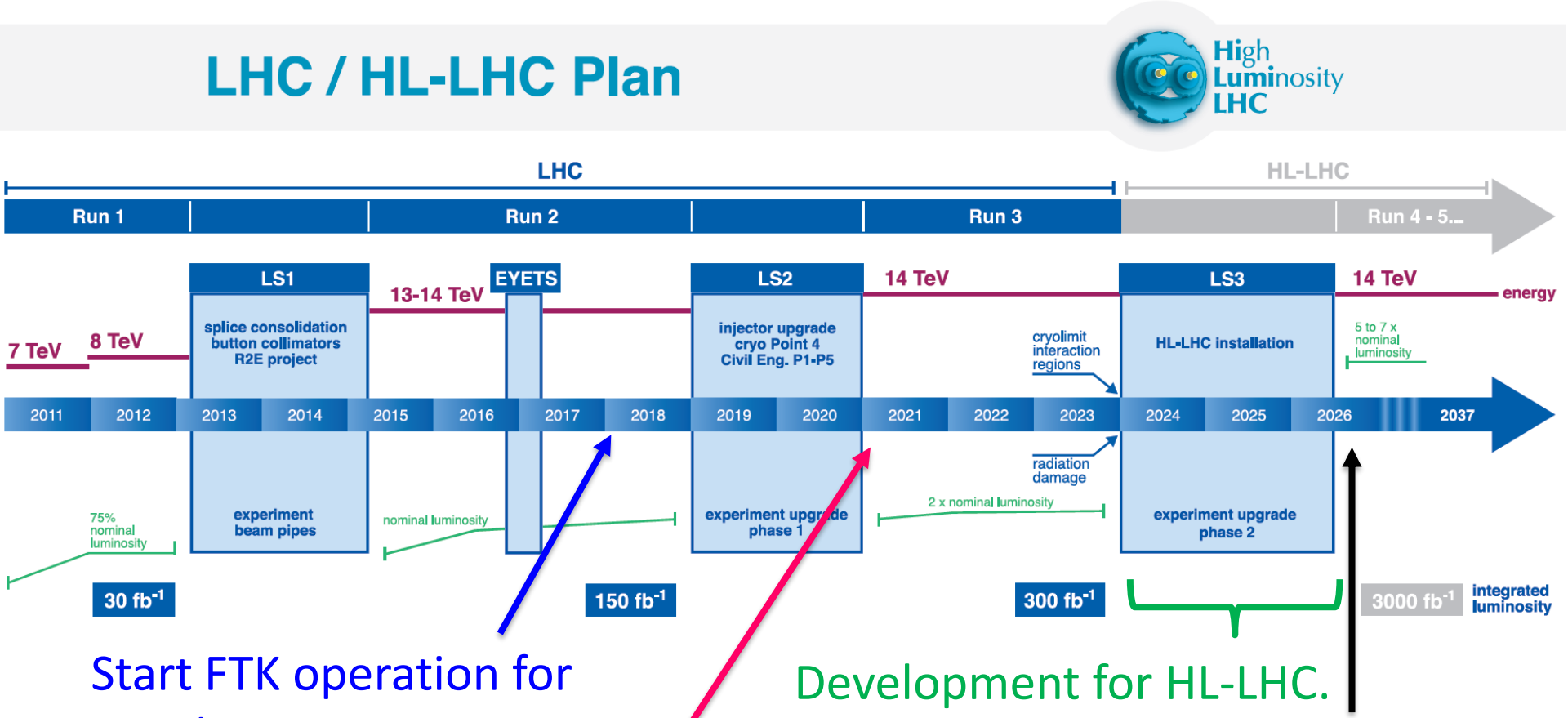
- ✓ Integration and its test are performed when there is no beam.
- ✓ FTK will be operated synchronized with other detectors.

First FTK Full Chain Output !!

Succeed to output to ROS with full FTK chain! **(1/64 region)**

Exceptional handling, improving stability to start operation is ongoing.

FTK plan (and Beyond)



Start FTK operation for 60 pile-up system.

Development for HL-LHC.

L1 Track, FTK++

Start FTK operation with 80 pile-up system.

- ✓ FTK will start operation in 2017 with system for 60 pile-up, with system for 80 pile-up in 2021, and operate entire Run3.
- ✓ FTK is demonstration of the key technology at HL-LHC as well.

Summary

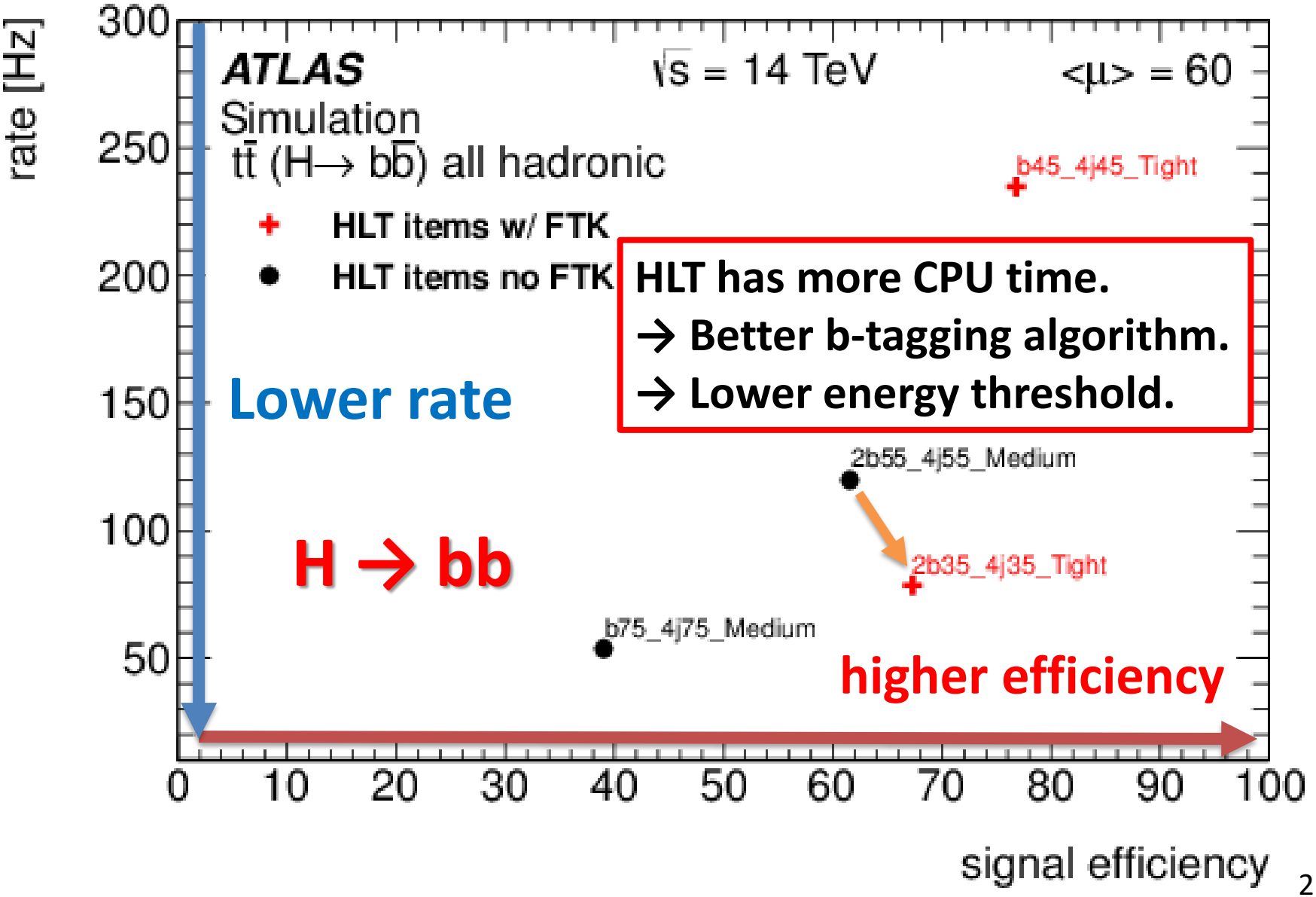
- FTK is a newly installed system of electronics with > 8000 ASICs and > 2000 FPGAs.
  - ✓ HLT can utilize track information from the full detector region and have extra time for more sophisticated trigger selection.
- The performance is evaluated by simulation.
  - ✓ Good track reconstruction performance can be achieved.
  - ✓ Realistic emulation is built and validated that FTK can operate stable at Run3 environment.
- Hardware installation and commissioning ongoing.
  - ✓ Boards are installed when the production is done.
  - ✓ Integrating to ATLAS and improving to operate stably.

It is a key development for the stable data taking at the ATLAS experiment in the future.

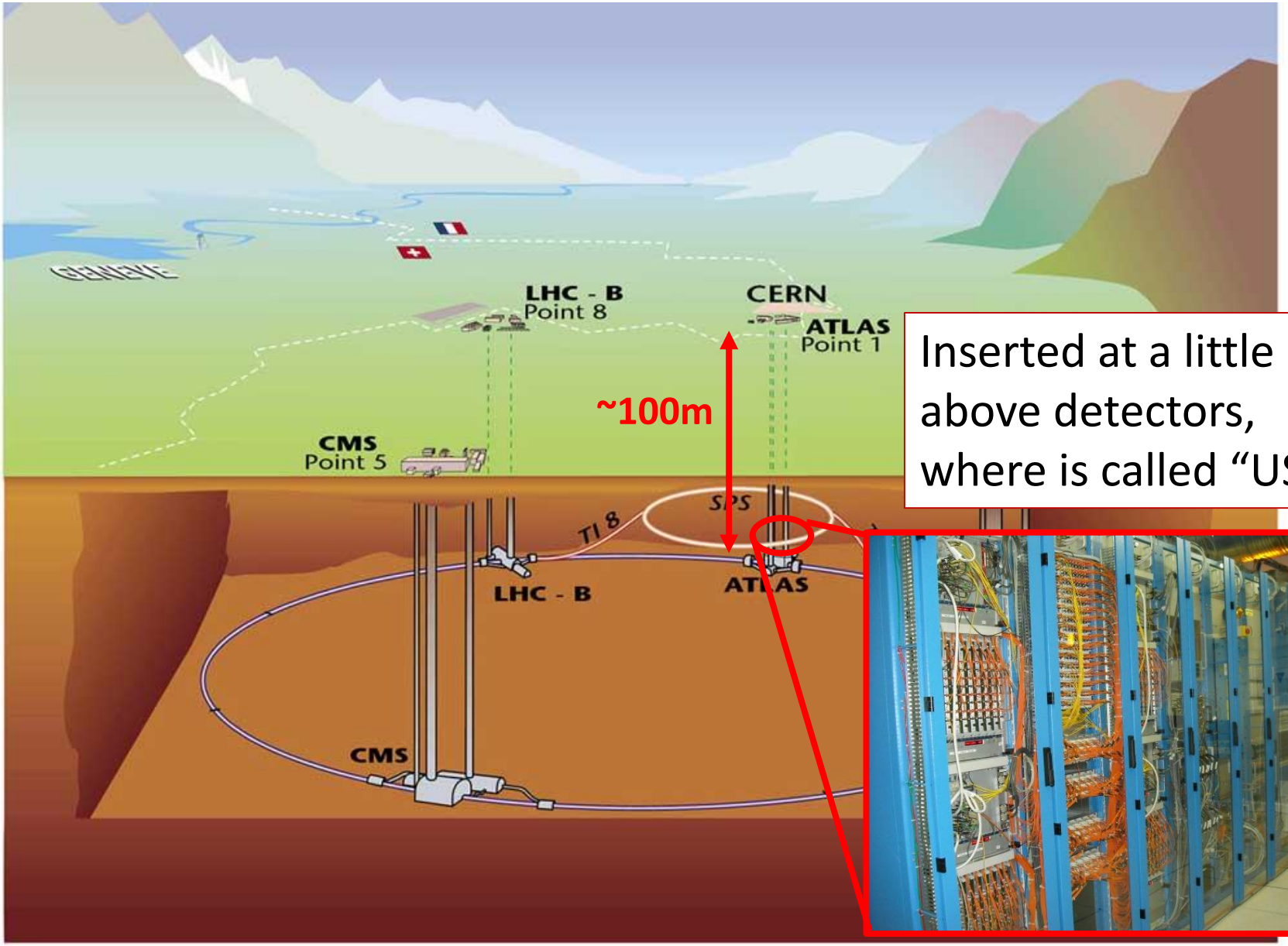
FTK TDR: http://cds.cern.ch/record/1552953/files/ATLAS-TDR-021.pdf

Backup

Expected performance: b-tagging

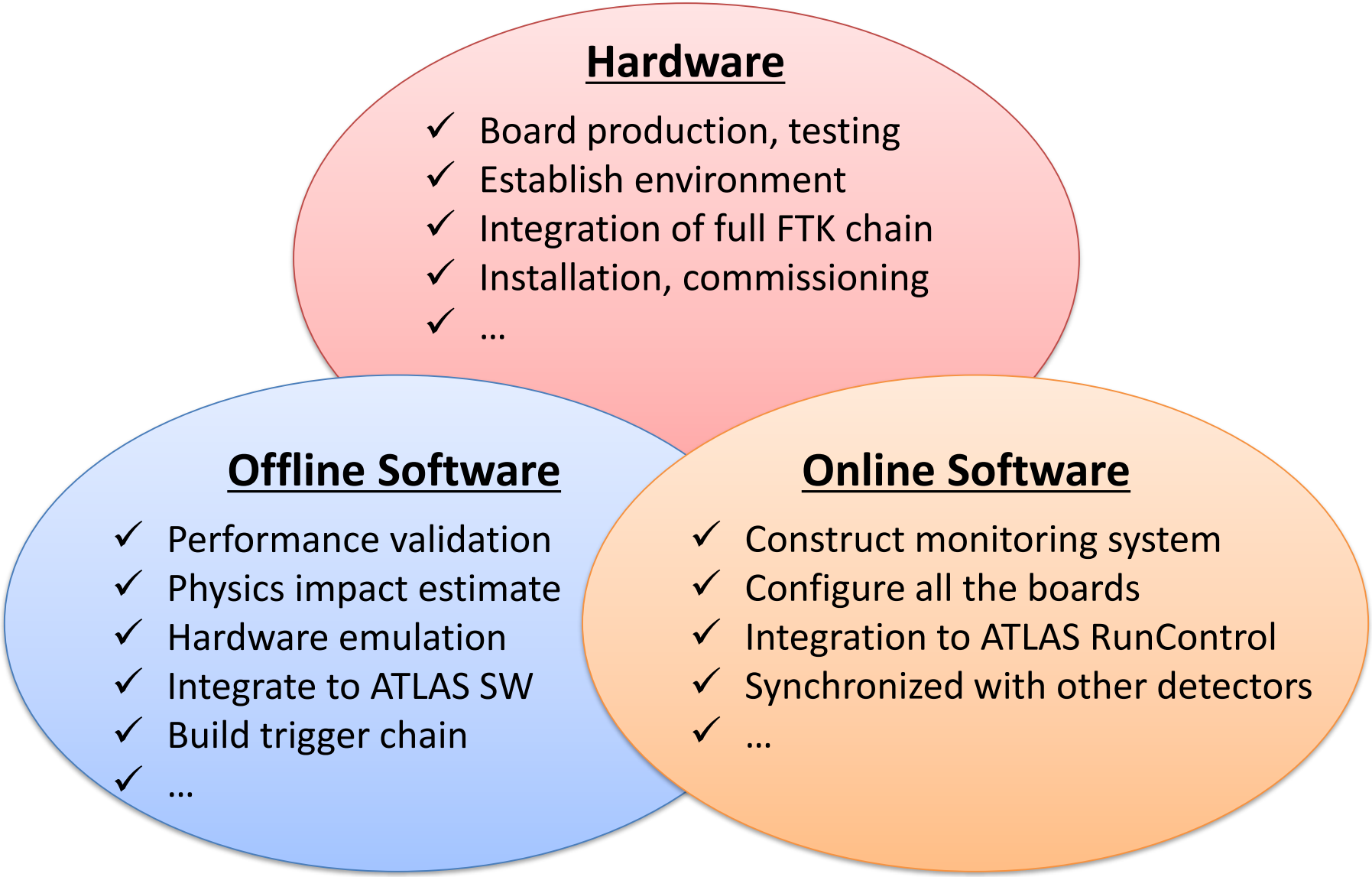


Where FTK Works?



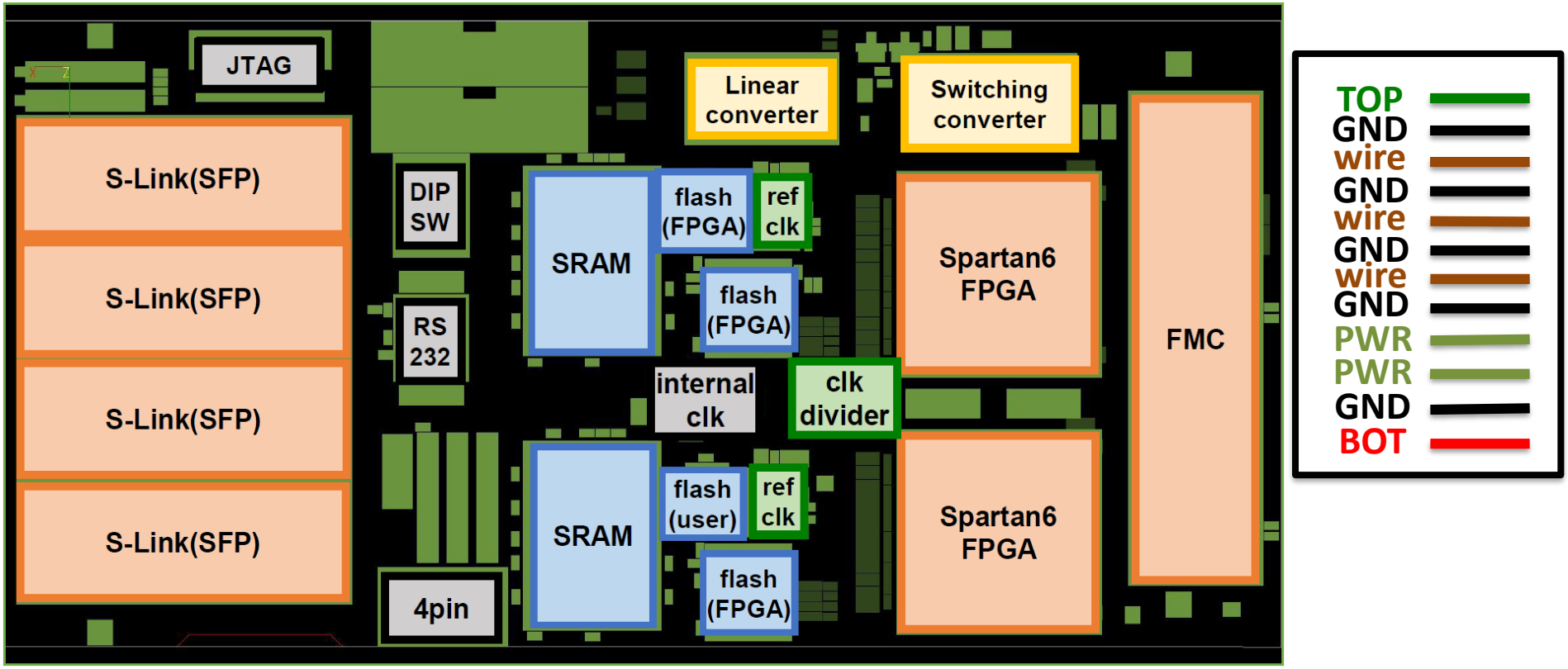
Inserted at a little above detectors, where is called “USA15”.

FTK Development Items



It is necessary to complete these to start operation!

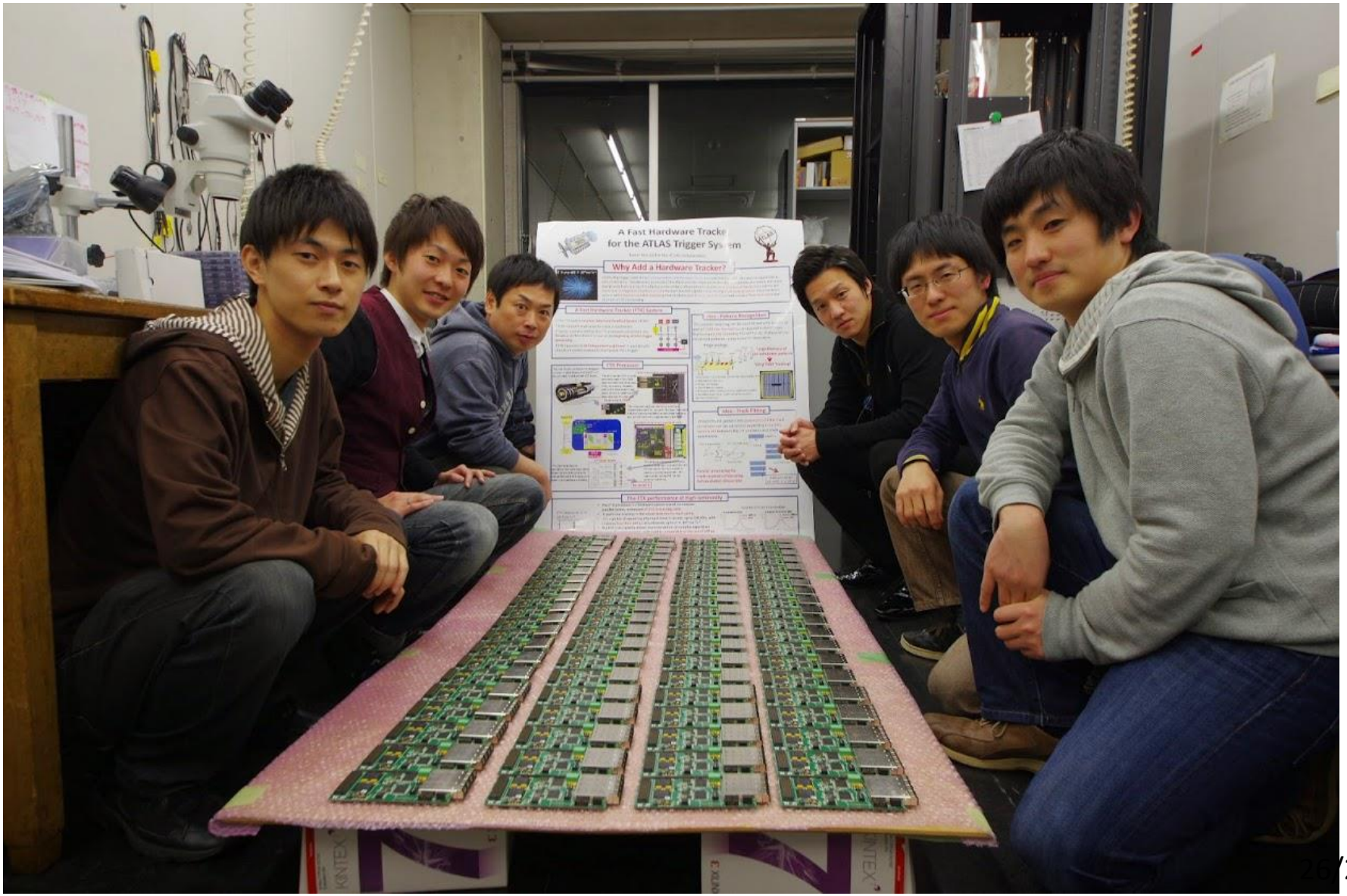
FTK_IM Board Production



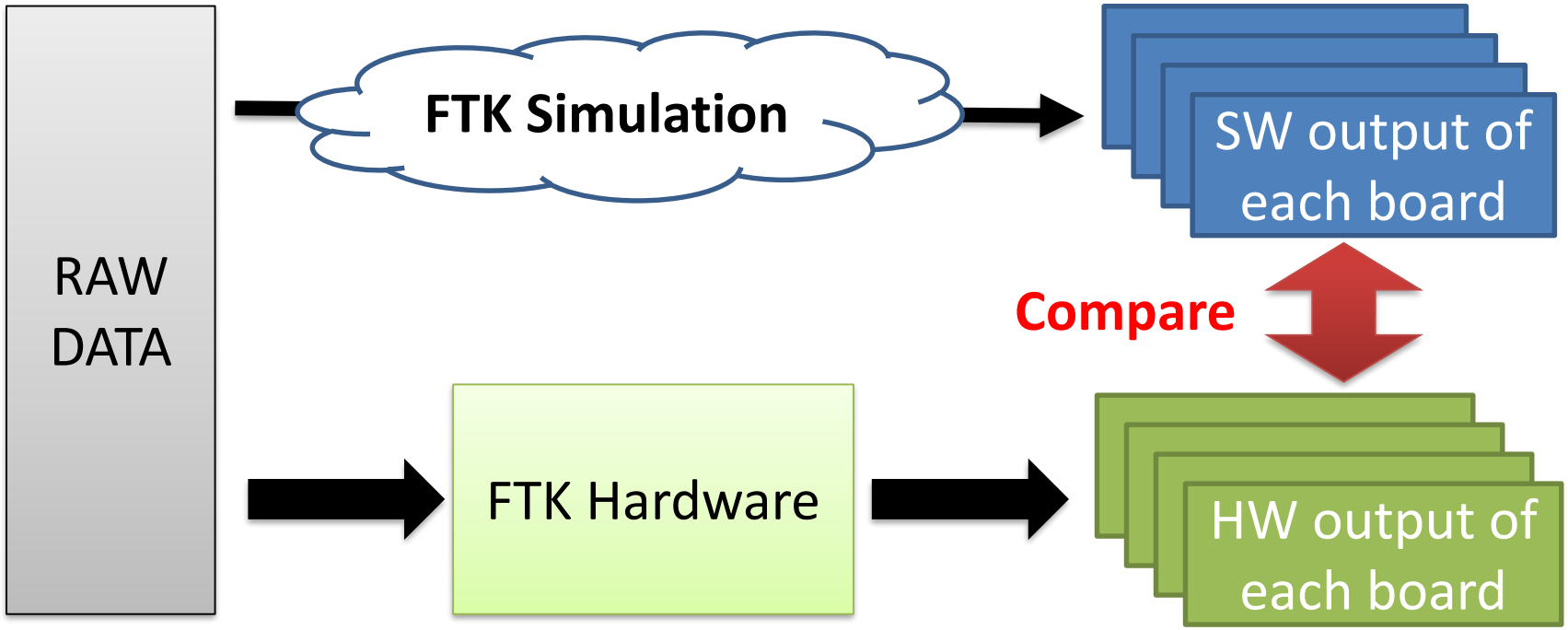
- ✓ Waseda is responsible for the design, production, testing of the FTK_IM board which is the uppermost of the entire system.
- ✓ Components are chosen to satisfy its requirements.
- ✓ It consists of 12 layers, circuit wiring was done with great care with cross-talks and the length among correlated lines.

Mass Production Completed !!

- **Version 4.0 (Feb. 2015) : Production version !**



Bit-Level Output Validation



- ✓ System to validate bit-level hardware output is established.
  - ◆ Simulation output of each FTK subsystem can be obtained.
  - ◆ HW output of each board can be obtained from spy buffers. Final output can be obtained from ATLAS ROS.
  - ◆ The output are checked when firmware is modified.

Bit-Level Output Validation

Ex.) IM/DF output

HW output	SW output
b0f00000	b0f00000
80009f98	80009f98
50170006	50170006
005a0048	005a0048
01400104	01400104
0180314d	0180314d
119b0188	119b0188
01ee21ac	01ee21ac
02280212	02280212

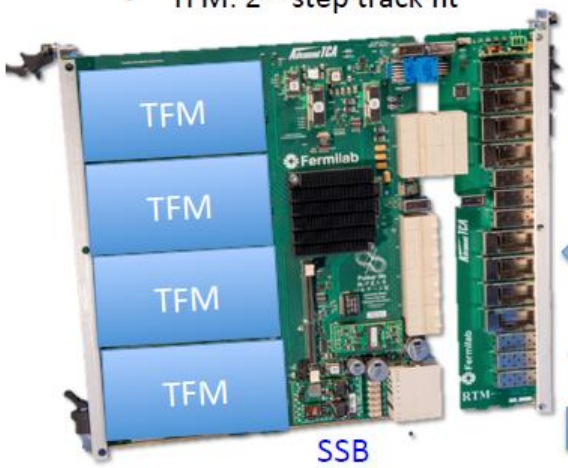
All Match!!

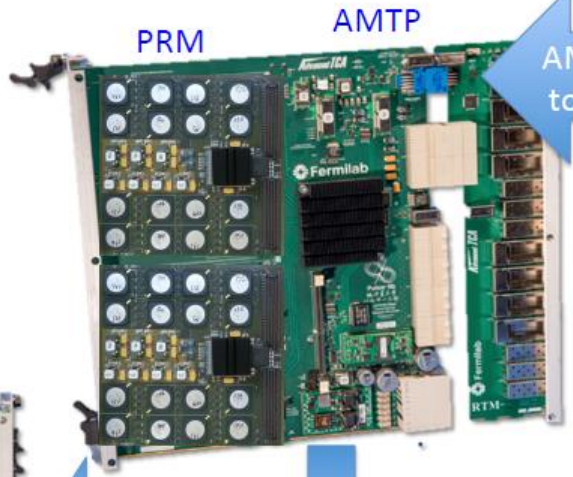
FTK++ plan

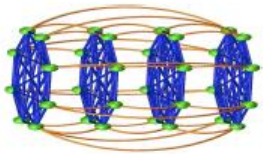
Processing model

More info: http://go.web.cern.ch/go/qjj9

- AMTP
  - Receive ITk inputs
  - Distribute ITk hits to other AMTPs and PRMs
  - PRM: AM pattern reco.
  - PRM: 1st step track fit
- SSB
  - track distribution
  - TFM: 2nd step track fit







AMTP-AMTP exchange to/from other shelves

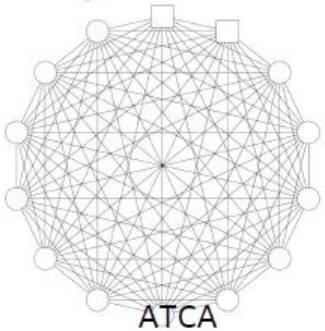
ITK inputs

1st stage trks

ITk inputs (2nd stage layers)

SSB – SSB to/from other shelves

Output tracks



ATCA
Full mesh
data exchange
AMTP-AMTP
AMTP-SSB
SSB-SSB