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Development of a High-Throughput Tracking Processor on FPGA Boards

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We present the latest results on the prototype of a tracking processor capable of reconstructing events in a silicon-strip tracker at about 40 MHz event rate with sub-microsecond latency. The processor is based on an advanced pattern-recognition algorithm, called "artificial retina", inspired to the vision system of the mammals. We design and implement this processor on a board equipped with Altera Stratix V FPGA's. Future applications of this novel approach as real-time track trigger at LHC experiments are also discussed.

Summary

Computing and storage demands of future LHC experiments at very high luminosity represent a challenge for HEP data processing, which calls for an efficient and scalable usage of the hardware. The increasing input rates and growing complexity of physics events, along with the finite bandwidth for writing to long term storage, call for sophisticated and computing intensive trigger algorithms. The available CPU time and I/O bandwidth, to and from storage, limit the amount of offline data reprocessing that can be performed. Moving part of the data processing, e.g. track reconstruction, to the online stage has multiple benefits: the stored event size can be reduced, trigger selection may be improved, and less processing has to be done offline.

While Moore's law for CPU was slowing down, FPGAs performances have increased steadily in the last few years. These devices are also particularly suited to perform repetitive tasks, such as tracking, with low power consumption, and they also allow for low and fixed latencies. Therefore an FPGA-based tracking unit could be integrated in the DAQ architecture at a moderate cost and act as a "track-detector", thus making event reconstruction primitives immediately available to event-building and high-level-trigger farms.

Our goal is to develop and implement a parallel computational methodology that allows to reconstruct events with an extremely high number (>100) of charged-particle tracks in pixel and silicon strip detectors at 40 MHz, thus matching the requirements for processing LHC events in real time. Our approach relies on a massively parallel pattern-recognition algorithm, dubbed "artificial retina", inspired by studies of the processing of visual images by the brain as it happens in nature. The artificial retina algorithm is based on two main concepts. First, for each track pattern we compute a quantity that measures how any combination of entered hits matches the pattern itself. Second, the hit sequence delivered to a pattern is an appropriate subset of all the events hits, reducing the data bandwidth involved in the process. Preliminary studies on simulation already showed that high-quality tracking in large detectors is possible with sub-microsecond latencies when this algorithm is implemented in modern FPGA devices.

After successfully developing a first prototype based on a 6-layer silicon detector and implementing that on an FPGA board with 4 Altera Stratix III chips, we port the system to a faster Stratix V FPGA chip. After additional optimization on this device, we were able to process events with low occupancy at 40 MHz rate and 0.5 us latency. We also present a feasible implementation of a larger scale system distributed over multiple commercial PCIe boards carrying Altera FPGA's. Further possible developments are also discussed, that will enable even greater performance, including 3D reconstruction, and "embedded operation", in which the reconstructed tracks are transparently incorporated with the data being read out.

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