Contribution ID: **138** Type: **Poster**

The Latency Validation of the Optical Link for the ATLAS Liquid Argon Calorimeter Phase-I Trigger Upgrade

Tuesday 12 September 2017 17:45 (15 minutes)

Two optical link data transmission ASICs have been designed for the ATLAS Liquid Argon (LAr) Calorimeter Phase-I upgrade. The latency of each ASIC and its corresponding receiver implemented in the back-end FPGA, are critically specified to be less than 150 ns. We present the latency measurements of two ASICs. The optical link latency measurement results indicate that both ASICs achieve their design goals and meet the latency specification. The consistence between the ASIC design simulation and measurements validates the ASIC characterization.

Summary

In the ATLAS Liquid Argon (LAr) Calorimeter Phase-I upgrade, the optical link is used to transmit the front-end detector data to the back-end control room. Two Application Specific Integrated Circuits (ASICs), LOCx2 and LOCx2-130, have been designed for such an upgrade. Each ASIC has two channels of serializers with custom encoders. LOCx2 is designed and fabricated in a 250-nm Silicon-on-Sapphire CMOS process and has been produced and is in packaging processing. LOCx2-130 is fabricated in a 130-nm bulk CMOS process to back up LOCx2. The latency budget is 75 ns for each ASIC itself and 150 ns for the whole link, excluding the time passing through the optical fiber. As a key specification, the latency of each ASIC and its corresponding receiver must to be validated.

We measure the ASIC latency by measuring the time difference between the input parallel data and the serial output data. The input parallel data have a special fixed pattern in an LHC clock cycle and another fixed, different pattern in all other clock cycles. For LOCx2, its scrambler functional block is turned off, so that we can locate the position of each bit in the input parallel data and in the serial output data. For LOCx2-130, since its scrambler cannot be turned off, we cannot identify the position of a specific bit in the output serial data. Instead, we determine the position of the nearest frame header and calculate the latency. Since there is a frame header in every 25 ns, the latency measurement of LOCx2-130 has an ambiguity of n * 25 ns (n = 1, 2, 3$\cdots$). Such an ambiguity is eliminated later by comparing to the ASIC simulation and the latency of the whole link.

For the whole-link latency, we generate a pulse aligned with the special input parallel pattern feeding into the ASIC and another pulse aligned with the recovered special pattern on the receiver side. The two pulses are logically OR'ed together and output via a pair of different pins of the FPGA to an oscilloscope. The latency is the time difference between these two pulses. The use of a single output pin eliminates the delay skew of output pins and reduces the measurement error.

The measurement results show that the ASIC latency is from 24.0 ns to 27.2 ns and the latency of the whole link is from 68.2 ns to 74.3 ns for LOCx2. The ASIC latency is from 34.4 ns to 40.7 ns and the latency of the whole link is from 100.2 ns to 106.2 ns for LOCx2-130. The optical link latency measurement results indicate both ASICs achieve their design goals and meet the latency specification. The ASIC latency measurement matches with the ASIC simulation. The latency of the whole link is consistent with the measurement using the Xilinx ChipScope Pro Analyzer tool. The consistence between the ASIC design simulation and measurements validates the ASIC characterization.

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Session Classification: POSTER Session

Track Classification: ASIC