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Development of a Waveform Sampling ASIC with Femtosecond Timing for a Low Occupancy Vertex Detector

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One of the crucial parts of the proposed low occupancy Timing Vertex Detector (TVD) is a waveform sampling ASIC denoted the RFpix. It is being developed to sample and digitize voltage pulses and enable measurements of their arrival times with a timing resolution of 100fs or less. To achieve this, the RFpix needs to have an analog bandwidth of 3GHz and a sampling speed of 20GS/s. In this paper, we present the architecture of the RFpix and discuss the challenges of designing and implementing the various subcircuits necessary to achieve the required performance.

Summary

Increasing luminosities of particle colliders result in ever higher hit rates of the innermost vertex detectors, thus increasing their occupancies. The TVD sensor architecture relies on using an asynchronous digital pixel matrix for detection and a high-precision timing readout technique, where the pixel position is encoded in the time of flight of voltage pulses on a micro-strip line. The arrival times of the pulses are measured by a waveform sampling ASIC called the RFpix, the architecture of which is based on differential switched capacitor (SCA) arrays. The prototype has 32 channels. Each channel has two unity gain amplifier buffers to decouple the capacitive loading of the SCA arrays from the inputs, thus providing the necessary analog bandwidth of 3GHz in a wire bonded package. The differential configuration of the SCA helps in terms of crosstalk mitigation and noise coupling. At the same time, it turns the amplitude dependent voltage error, due to charge injection, into a virtual gain of the sampling cell. The strobe signals are generated by a two-level delay locked loop (TLDLL), which ensures a worst case added jitter of 41fs. Two adjacent channels share one TLDLL, which has several advantages: avoiding loading on the strobe lines and thus providing with fast strobe rise times (app. 30ps), lowering of the power consumption, and providing with the possibility of interleaving. With the TLDLL tap delay of 50ps, the 20GS/s sampling speed is achieved. Every SCA block has a trigger logic that issues a transfer cycle, which latches the SCA block for 3.2ns (64 cells x 50ps) upon signal detection. Within this time, the SCA cell values are transferred in parallel to an analog storage array. Each storage array has a depth of 32 storage cells. Each storage cell has an integrated comparator, which is a part of a parallel slope ADC, which runs at a speed of 128MS/s/channel due to its parallel configuration. The digitized data is transmitted off-chip by a serializer logic through a dedicated LVDS driver per channel. With a 12-bit ADC, buffer depth of 5µs, and the system trigger of 30kHz, the overall data throughput is around 2Mbits/s/channel. The average power consumption without the input buffers is estimated at 25mW per channel. The input buffers are not planned in the final detector version (flip-chip mounting directly on the sensor). The prototype is being designed in the TSMC 130nm technology node, which has proved to have good performance in radiation-hard environments. In addition, working in this technology provides the necessary transistor speeds, dynamic range, and level of integration. The RFpix is to be the first low-power, multi-channel waveform digitizer with timing resolution in the range of 100fs.

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