Characterization of SLVS driver and receiver in a 65 nm CMOS technology for High Energy Physics applications

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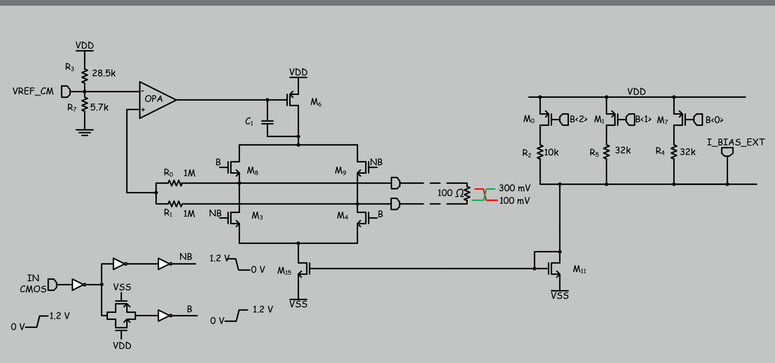
Introduction

This work presents the design and characterization of an SLVS transmitter/receiver pair, to be used for I/O links in High Energy Physics applications. The prototype chip was designed, and was completely characterized in the first quarter of 2016. The chip has been also irradiated with X-rays in order to evaluate the effect of the ionizing radiation on the signal integrity. This activity has been developed in the framework of the CERN RD53 collaboration, whose aim is the design of the next generation of hybrid pixel readout chips for the ATLAS and CMS Phase 2 pixel upgrades. The ultimate goal of this three year project is the development of an innovative chip for pixel detectors, using a 65nm CMOS technology for the first time in the High Energy Physics (HEP) community.

Differential I/O link for Harsh Radiation Environments

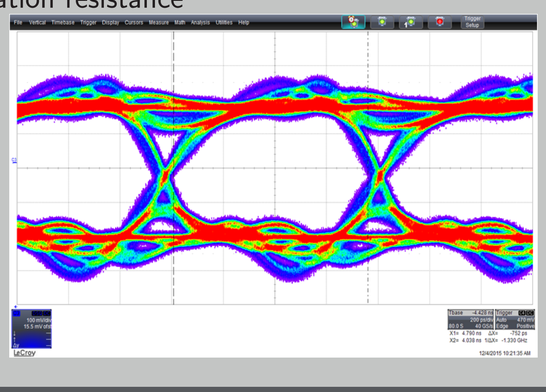
- A transmitter/receiver pair IP block for integration in the RD53A ASICs, complying with SLVS protocol, was designed in a 65 nm CMOS technology.
- The SLVS standard describes a differential current-steering protocol with a voltage swing of ± 200 mV on a 100 Ω termination resistance and a common mode of 200 mV [1]. The driver architecture is based on a Bridged-Switch Current Source (BSCS) scheme. The 2 mA biasing current is switched through a 100 Ω termination resistance, according to the input data stream. The output current of the transmitter can be trimmed, by means of three configuration bits, in a range from 500 μA to 2.5 mA. In order to achieve insensitivity to PVT variations, a simple low power common-mode feedback has also been included. The common mode voltage is sensed by two resistors, which are connected to the output node and compared with a reference voltage, which is generated by a resistor voltage divider. The CMFB amplifier is based on a two stage Miller OTA [2].
- The receiver is a rail-to-rail stage, in order to detect differential signals with a common mode from 100 mV to 1 V. It is based on three different stages: the first one is a fully differential amplifier with a cross-coupled load and with a bandwidth close to 1.2 GHz; the second stage is a differential-to-single ended amplifier with a full swing CMOS output chip voltage and the last one is a chain of three inverter.

Characterization results - Transmitter

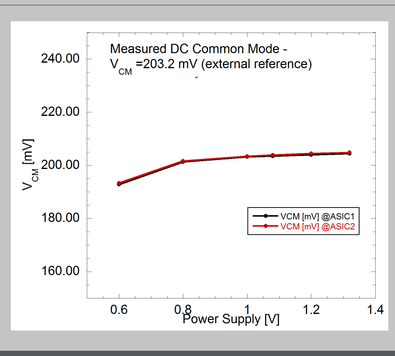


- Programmable TX output current (0.5 mA, 1.0 mA, 1.5 mA, 2.0 mA, 2.5 mA)
- Phase margin: ≥ 70 °
- Power dissipation: 2.8 mW
- Area: 150 μm *x* 200 μm

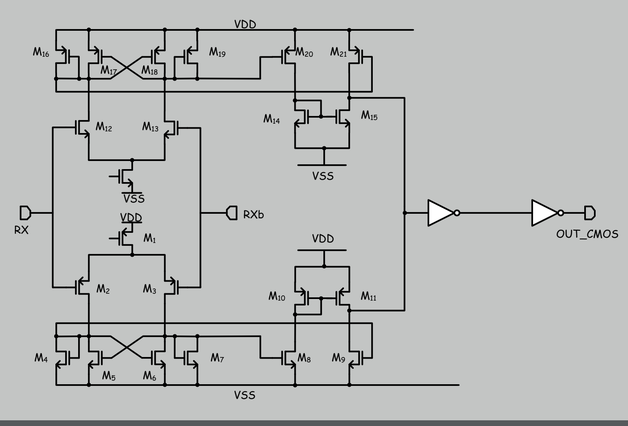
- Two ASICs are bonded directly on the PCB
- The termination resistance (RT) is connected to the driver through a 5.5 cm microstrip differential pair
- 1.2 Gbit/s CMOS PRBS signal applied to the driver input
- Transmitter output signal via Differential Probe on termination resistance



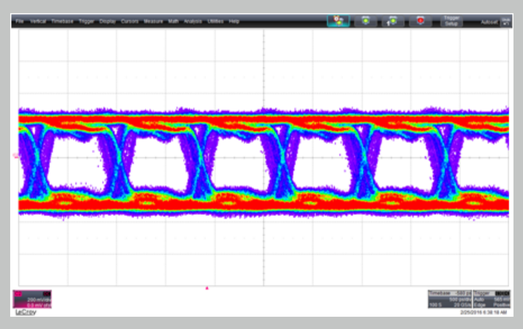
Eye Amplitude	376.7 $\pm$ 11.7 mV
Eye Height	365 mV
Eye Width	752 ps (0.9 UI)
rms Jitter	11 ps
Eye Rise Time	309 ps
Eye Fall Time	220 ps



Characterization results - Receiver



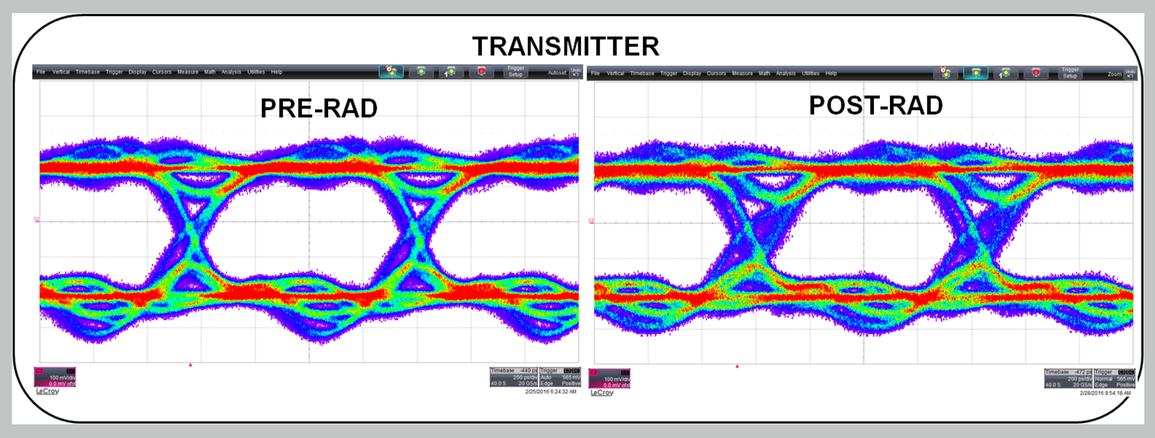
- The receiver is AC coupled to the driver for possible use in serial powering
- The receiver has been stimulated with a 1.2 Gbit/s differential PRBS signal
- Internal termination resistance ($R_T = 100\ \Omega$)
- Power dissipation: 2.5 mW
- Area: 90 μm *x* 115 μm



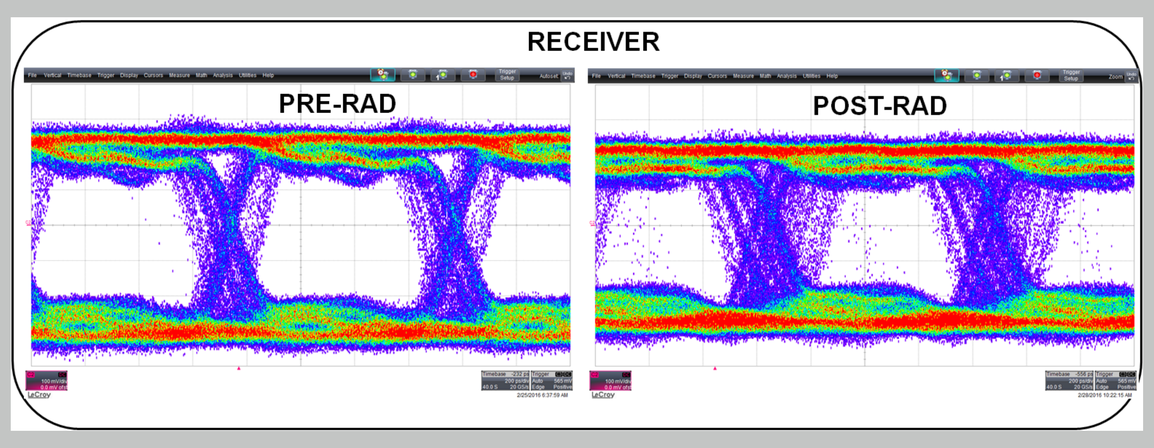
- The receiver is followed by CML driver provided by the microelectronics group of CERN
- The minimum detectable signal at 1.2 Gbit/s is an input differential voltage of 150 mV
- The eye diagram is measured at CML output at 1.2 Gbit/s, when at the input $V_{ID} = 200$ mV - $V_{CM} = 200$ mV is applied

Irradiation Results

- The chip was irradiated up to 550 Mrad TID with the X-ray facility at CERN.The dose rate was 9 Mrad/h.
- During irradiation the chip was biased and stimulated by an input signal.



- Limited degradation of the crossing point
- Jitter degraded from 11 to 25 ps
- Eye amplitude from 378 mV to 359 mV



- Degradation of the crossing point
- Degradation of the eye opening

Conclusion and future activity

- A differential link for the RD53 collaboration has been designed, fabricated and characterized. In order to prove its capability to operate in harsh radiation environment, differential driver and receiver were irradiated with X-rays up to 550 Mrad TID.
- This IP has been integrated in the RD53A chip

Reference

[1] JEDEC, Scalable Low-Voltage Signaling for 400 mV (SLVS-400), JESD8-13

[2] G. Traversi et al., Design of low-power, low-voltage, differential I/O links for high energy physics applications, JINST 2015

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